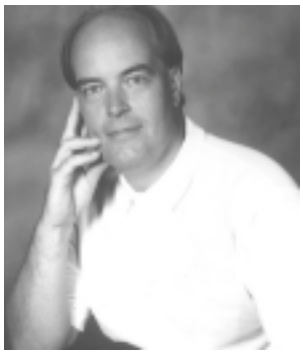
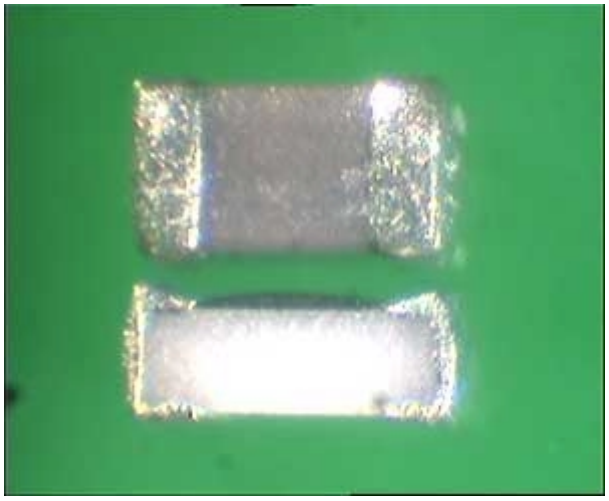
0201 Printed Board Design And Assembly Issues



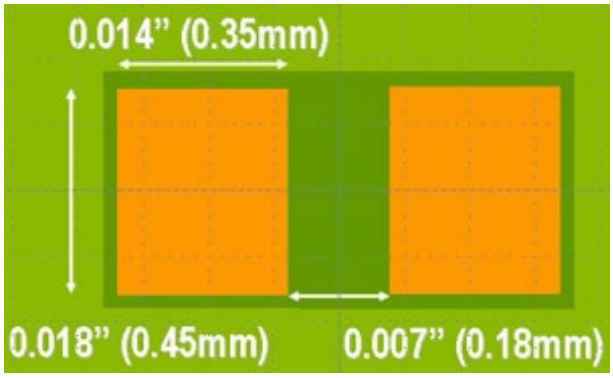
Probably the biggest issue with 0201 chip components are the tolerances when using what is currently the smallest chip component available. The tolerances involved are board laminate, solder mask and etching of copper foil which all make printed circuit board inconsistency a problem during assembly. The chip components are 0.020" long by 0.010" wide, solder resist may have a error of 0.002" and a laminate error can be 0.001" per inch, how can we ever make a circuit board or assemble components on to it?

Component Pads

There are a number of recommendations on pad design from numerous evaluation projects around the world. Some of the papers are listed in the SMART Group Charity Report "Design and Assembly of 0201 Components which is available from all SMART Group offices. Based on results of trials on projects with Harting Connectors, Speedline Technologies and The Cookson Electronics Hands-On Workshops the following are recommended for inclusion in future designs.



Example of 0201 chip capacitor and resistor



The copper pad size above may be 0.018" wide and 0.014" long with a pad to pad separation of 0.007".

Bob Willis Process Guides

An alternative way of sizing the pads, which has been reported, is to use solder mask to define the mounting area. Effectively the pads are slightly larger with the solder mask overlapping the edges of the copper to provide the defined solderable area. The disadvantage of this design technique is that the copper must be larger than the pad would normally be. The copper pad must be larger than the maximum tolerance of the solder mask. For example, if we wanted a resist defined pad of 0.018" x 0.014" the copper land area would have to be a minimum of 0.024" x 0.022". The larger the copper pad the larger the surface area taken up with circuitry.

Pad to Pad/Component to Component Spacing

Inevitably to take full advantage of 0201 size reduction the components must be placed as close as possible to each other and adjacent parts. Considerations to be taken into account during the layout or during production trials are:

*** Placement machine accuracy and repeatability**
*** Print accuracy and repeatability**
*** Component movement during reflow**
*** Size of the placement tool overhanging the component**
*** Air release from the pick up tool**
*** Tolerance of the printed board**

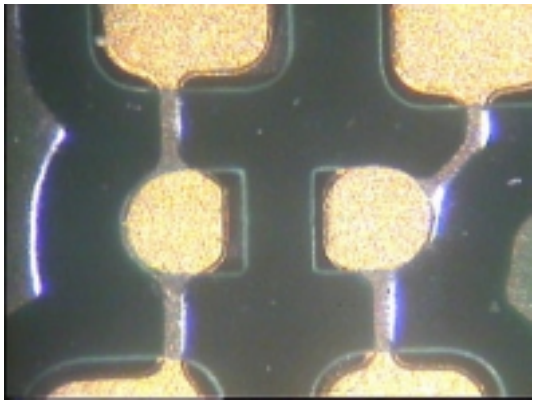
Typically the part to part separation which is currently being used is 0.008" but most companies will want to achieve a better separation of 0.006" which will impact on many other processes other than placement.

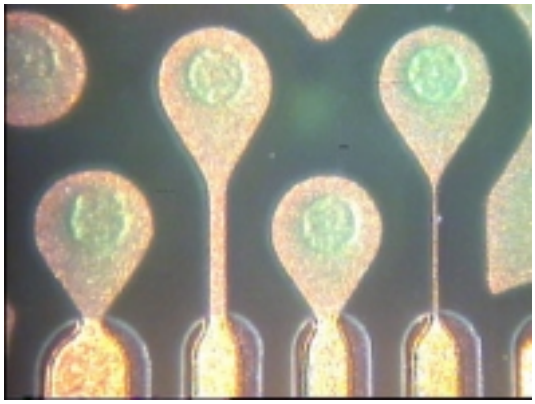
Interconnection

There are only two methods to make a connection to the component termination, one being a track to one of three sides of the pad. Alternatively, a via hole is directly placed in the pad stack, this has been used successfully on many 0402 chip designs on mobile products for the past few years.

Tracks

The track width would normally be the same as the minimum track size on the outer surface of the board. It is also perfectly feasible to use a wider track width and reduce the track size locally necked to the pad to reduce the possibility of damage and process yield in circuit manufacture. Typically the track size would be between 0.006-0.008" and the track would link to the pad with a teardrop/snowman pad. The benefit of a slightly wider section is that as it joins the pad it is more robust on small track sizes. It is stronger on thin boards and reduces the risk of etch problems on 90o connections.

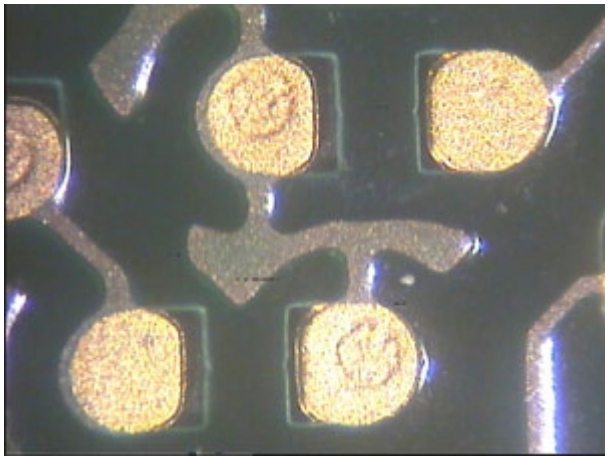




Example of track to pad and track to via interconnection with teardrops, this technique is commonplace in flexible circuit and rigid paper based board designs.

Via Holes

The minimum economical via should be used in each case on the surface interconnection after first tracking out from the pad. The pad of the via hole does of course take up more room than the via. Consideration could be given to landless vias which have been used successfully in the past. Typically vias would be between 0.012" - 0.003" using traditional drilling at the high end and laser vias at the lower end. The use of via in pad is of course another option and making the via part of the stack, which is also a benefit as it reduces the outer layer tracking.



Example above shows a via in pad. The pad is 0.018" and the via is 0.008"

Solder Resist Mask

There are very few applications today where solder mask is not used on circuit boards to isolate surface interconnection. In the case of 0201 chip components the solder mask would normally follow standard design rules. The solder mask would have a border of 0.002" - 0.003" around the copper pads. This would be normal practice for surface mount pads in the industry.

When the chip component size drops down from 0805 to 0201 the possibility of running tracks between the pads and under the chip parts becomes unreasonable. This provides the possibility of using a single solder mask window around both surface mount pads. The dimensions of the resist remain the same 0.002" - 0.003" larger with the gap between the pads left open. This can make life easier for the printed board supplier in terms of tolerance issues if a 0.003" border is used.

One additional consideration covered in 0201 technical papers is the use of resist defined pads. The solder mask is designed to form the pad sizes for soldering based on the tolerances of the mask. As an example, to use resist defined pads the copper pad could be 0.004" larger than the optimum for assembly. It should be considered that if resist defined pads are used then resist defined fiducial pads should also use the same technique.

The reasoning behind the use of resist defined pads for passive components like 0201 is not clear, but here are some possible suggestions:

*** Better accuracy between resist defined fiducial/mounting pads**
*** Better vision alignment from a camera on resist defined pads**
*** The tolerance on the resist image is better than the copper to copper image**
*** Elimination of pad lift during rework**

(There is no evidence to support any of the above)

We know that laminate moves in manufacture, that is why we have board fiducials and local alignment marks for fine pitch parts. Solder mask also has errors, so is the solder mask positionally more accurate, aperture to aperture than copper to copper? There may be other reasons with the laminate material becoming thinner/more transparent and the potential for error during optical alignment; a resist to copper edge may offer a better image to interrogate, I wonder if this is true?

PCB Laminate

There are a number of different laminate options in the industry but the bottom line is any alternatives to standard FR4 glass epoxy laminate will cost more. The laminate choices may include:

FR4 Glass Epoxy
FR4 (Multifunctional)
Polyimide
BT/Epoxy
PTFE
Thermount (Dupont)

All the options are a higher price than standard materials and hence the reluctance to change but there are limits to the material's capability. Every circuit is getting smaller and tolerances make things more difficult if not impossible to produce so if an alternative material were available people would use it, but only if the cost were not significantly different.

Solder Finishes

To provide the best assembly option tin/lead is not practical for miniature products. There are a wide selection of solder finishes which can be used for 0201 based products. The alternative surface mount finish options have been surveyed in the past by SMART Group with results on the Group's web site www.smartgroup.org. The most recent industry survey was conducted by the IPC with the following results:

PCB Solder Finish Survey Conducted by IPC

Solder Finish Type (%)	2000	2001
Copper OSP	10	7.9
Selected Solder Level (HASL)	66.9	65.7
Tin-Lead Plate and Reflow	4.2	4.2
Tin	0.1	0.2
Nickel/Gold	4.8	5.1
Immersion Gold	12.2	15.3
Palladium	0.6	0.5
Tin-nickel	0.2	0.1
Silver	0.8	0.6
Other	0.3	0.2

(The total does not actually add up to 100 due to some rounding of the figures)

Each of the alternative tin/lead finishes are possible with 0201 and it will depend on your preference to solder levelled finishes. To date gold, silver, tin and OSP have been used.

Fiducial Marks

The use of fiducial marks is standard practice in surface mount assembly so that placement systems can check the position of the board and relate the placement position of components to the board pattern. The use of mechanical tooling to the non-plated drilled hole is not suitable for SMT. However, hole to hole alignment can be more accurate when considering odd form through hole assembly for intrusive reflow.

In the case of fine pitch parts below 0.020" pitch, both board fiducials and device fiducials should be used. First the board alignment is undertaken, then local alignment of the fine pitch part to the board pattern is conducted where necessary. In the case of a multiple board, a large panel with sub panels, each of the boards should have their own alignment marks. It is also not uncommon for engineers to notice a trend of poor placement due to sub panel movement in the larger panel. This can be caused by PCB machining, routing or scoring and can move the pattern by 0.003 - 0.004".

Standard fiducial marks are diamonds, squares or circles in the copper pattern with relief around the pad. The marks are normally positioned on the opposite corners of a board and the opposite corners of fine pitch devices. In the case of thin and fine pitch boards a third mark is also requested on the outer edge of the panel. In the case of each of the standard optical marks a resist window is placed around the pad normally leaving a 0.050-0.060" window. The stencil printing process will also use optical alignment to position the stencil and the board pattern.

Some companies in their evaluation of 0201 assembly have suggested the use of resist defined fiducial marks; it will be interesting to hear in the future the reasoning behind this option. To date there has not been a need to change traditional practices.

Legend

Legend must be considered a thing of the past on small portable products, there is simply no surface area available for markings. Legend was provided in the past to aid assembly, inspection, test or rework recognition. Legend is the most inaccurate process when using screen printing; direct imaging or jetting will reduce the errors but the size of characters and the ink slump is an issue on small products.

Fundamentally you cannot reduce the size of the printed image as the print quality deteriorates and boards are rejected for poor prints or contaminated pads. There is also a limit to what can be manually read so what is the point. Remove legend, it makes sense and should saves money on your board price.

Solder Paste Stencil

Solder paste stencil apertures are often defined by design and assembly engineers during initial prototype phase. Based on the component pitch likely to be used on a board with a mixture of 0201, CSP and fine pitch it is likely that a 0.005" stencil will be used. However, a 0.006" thick stencil has been used successfully with lead free paste on production trials. This was necessary to accommodate both 0201 and through hole intrusive reflow of connectors.

It is recommended that the aperture used be size for size with the 0.005" stencil and a reduction of the aperture areas under the component termination only when using a 0.006" foil. The majority of people have highlighted that an electroless nickel stencil has provided the best results in trials but success has also be achieved with laser cut foils. The variable is probably the quality of stencil manufacturer or the paste stencil combination.

Bob Willis is a process engineer providing engineering support in conventional and surface mount assembly processes. He runs production lines for suppliers at exhibitions and also provides seminar and workshops world wide. Bob has one of the largest collection of training videos, interactive CD-ROMs and training material in the industry. Bob will be presenting four Master Classes at APEX in California, he will also be presenting classes at SMT Nuremberg in Germany for those engineers visiting the show. For further information on how Bob may be able to support your staff contact him via his web site **www.bobwillis.co.uk**