Device Features

- Fully qualified Bluetooth system
- Bluetooth v1.1 and v1.2 specification compliant
- Low power 1.8V operation
- Minimum external components
- Integrated 1.8V regulator
- UART Bypass mode
- Available in VFBGA and CSP packages
- Available in 'RF Plug and Go' package (see separate data sheet)
- RoHS Compliant

BlueCore™2-ROM

Single Chip Bluetooth® System

Production Information Data Book for

BC213143A

October 2004

General Description

BlueCore2-ROM is a single chip radio and baseband chip for Bluetooth wireless technology 2.4GHz systems.
It is implemented in 0.18μm CMOS technology.

BlueCore2-ROM has the same pinout and electrical characteristics as available in BlueCore2-Flash to enable development of custom code before committing to ROM.

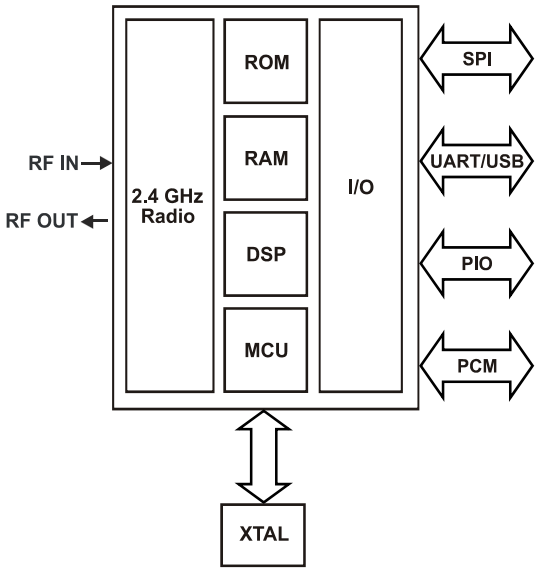
The 4Mbit ROM is metal programmable, which enables an eight week turn-around from approval of firmware to production samples.

Applications

- Cellular Handsets
- Personal Digital Assistants
- Mice
- Keyboards
- High volume, cost sensitive production

BlueCore2-ROM has been designed to reduce the number of external components required which ensures production costs are minimised.

The device incorporates auto-calibration and built-in-self-test (BIST) routines to simplify development, type approval and production test. All hardware and device firmware is fully compliant with the Bluetooth specification v1.1 and v1.2.



BlueCore2-ROM System Architecture

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Status Information

The status of this Data Sheet is **Production Information.**

CSR Product Data Sheets progress according to the following format:

Advance Information:

Information for designers on the target specification for a CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.

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Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

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1 Key Features

Radio

- Operation with common TX/RX terminals simplifies external matching circuitry and eliminates external antenna switch
- Extensive built-in-self-test minimises production test time
- No external trimming is required in production
- Full RF reference designs are available

Transmitter

- Up to +6dBm RF transmit power with level control from the on-chip 6-bit DAC over a dynamic range greater than 30dB
- Supports Class 2 and Class 3 radios without the need for an external power amplifier or TX/RX switch
- Supports Class 1 radios with an external power amplifier, provided by a power control terminal controlled by an internal 8-bit voltage DAC and an external RF TX/RX switch

Receiver

- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Digitised RSSI available in real time over the HCI interface
- Fast AGC for enhanced dynamic range

Synthesiser

- Fully integrated synthesizer; no external VCO varactor diode, resonator or loop filter
- Compatible with crystals between 8 and 32MHz (in multiples of 250kHz) or an external clock
- Accepts 7.68, 14.4, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz TCXO frequencies for GSM and CDMA devices with either sinusoidal or logic level signals

Auxiliary Features

- Crystal oscillator with built-in digital trimming
- Power management includes digital shut down and wake up commands and an integrated low power oscillator for ultra low Park/Sniff/Hold mode power consumption
- Device can be used with an external master oscillator and provides a ‘clock request signal’ to control external clock source

Auxiliary Features

- On-chip linear regulator, producing 1.8V output from 2.2 – 4.2V input
- Power on reset cell detects low supply voltage
- Arbitrary sequencing of power supplies is permitted
- Uncommitted 8-bit ADC and 8-bit DAC are available to application programs

Baseband and Software

- Internal programmed 4Mbit ROM for complete system solution
- 32Kbyte on-chip RAM allows full speed Bluetooth data transfer, mixed voice and data, plus full seven Slave piconet operation
- Dedicated logic for forward error correction, header error control, access code correlation, demodulation, cyclic redundancy check, encryption bitstream generation, whitening and transmit pulse shaping
- Transcoders for A-law, μ-law and linear voice from host and A-law, μ-law and CVSD voice over air

Physical Interfaces

- Synchronous serial interface up to 4M baud for system debugging
- UART interface with programmable baud rate up to 1.5M baud with an optional bypass mode
- Full speed USB interface supports OHCI and UHCI host interfaces. Compliant with USB v2.0
- Synchronous bi-directional serial programmable audio interface
- Optional I^2C™ compatible interface

Bluetooth Stack

CSR’s Bluetooth Protocol Stack runs on-chip in a variety of configurations:

- Standard HCI (UART or USB)
- Fully embedded to RFCOMM
- Customer specific builds with embedded application code

Package Options

- 84-ball VFBGA 6 x 6 x 1.0mm 0.5mm pitch
- 49-ball CSP 4 x 4 x 0.7mm 0.5mm pitch

2 6 x 6 VFBGA Package Information

2.1 BC213143AXX-EK and BC213143AXX-RK Pinout Diagram

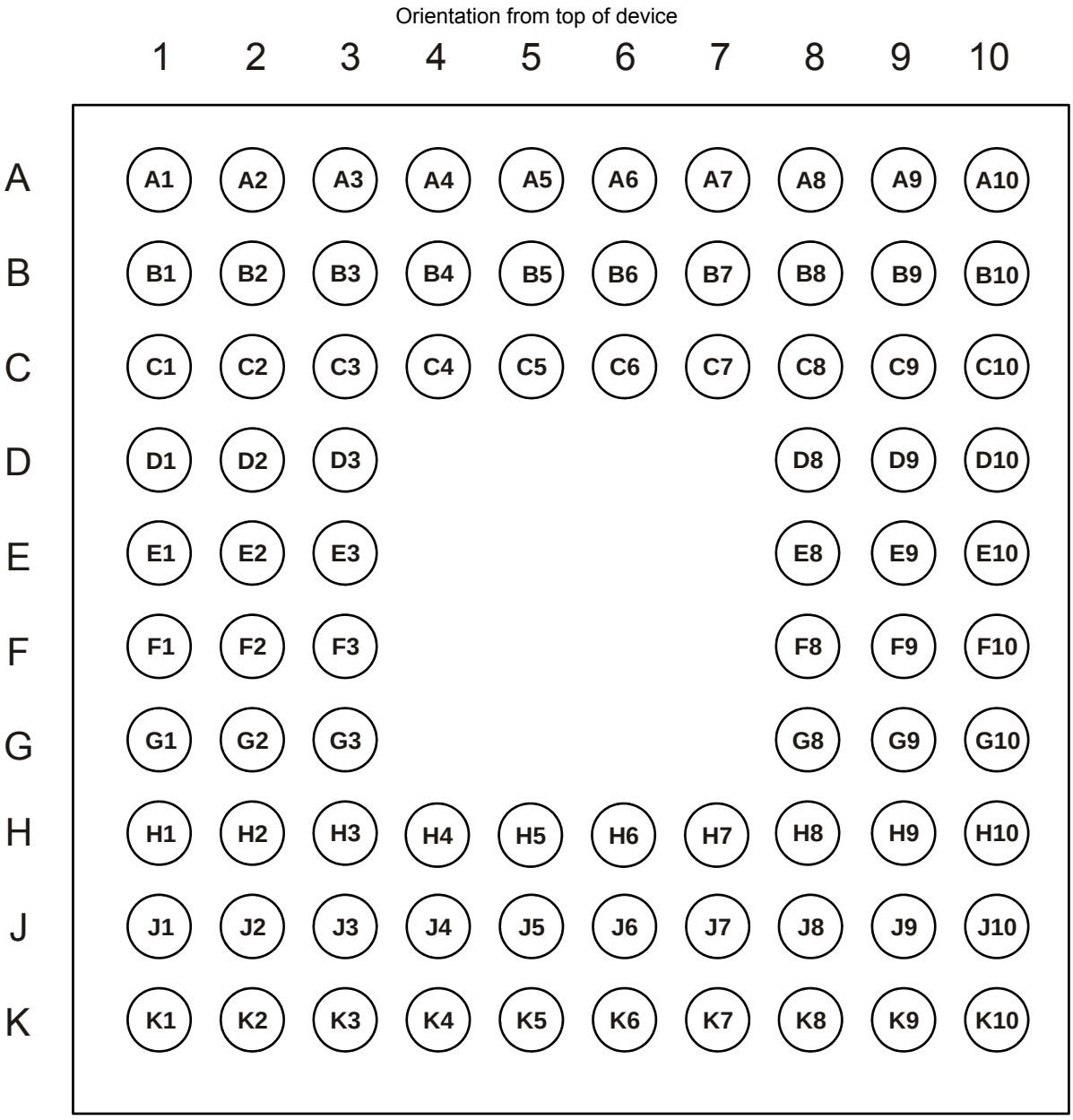


Figure 2.1: BlueCore2-ROM 6 x 6mm Packages (BC213143AXX-EK and BC213143AXX-RK)

2.2 Device Terminal Functions

Radio	Ball	Pad Type	Description
RF_IN	D1	Analogue	Single ended receiver input
PIO[0]/RXEN	B1	Bi-directional with programmable strength internal pull-up/down	Control output for external LNA (if fitted)
PIO[1]/TXEN	B2	Bi-directional with programmable strength internal pull-up/down	Control output for external PA (if fitted for Class 1)
TX_A	F1	Analogue	Transmitter output/switched receiver input
TX_B	E1	Analogue	Complement of TX_A
AUX_DAC	D3	Analogue	Voltage DAC output

Synthesiser and Oscillator	Ball	Pad Type	Description
XTAL_IN	K3	Analogue	For crystal or external clock input
XTAL_OUT	J3	Analogue	Drive for crystal
LOOP_FILTER	H2	Analogue	Connection to external PLL loop filter (Do not connect)

PCM Interface	Ball	Pad Type	Description
PCM_OUT	G8	CMOS output, tristatable with weak internal pull-down	Synchronous data output
PCM_IN	G9	CMOS input, with weak internal pull-down	Synchronous data input
PCM_SYNC	G10	Bi-directional with weak internal pull-down	Synchronous data sync
PCM_CLK	H10	Bi-directional with weak internal pull-down	Synchronous data clock

USB and UART	Ball	Pad Type	Description
UART_TX	J10	CMOS output, tristatable with weak internal pull-up	UART data output active low
UART_RX	H9	CMOS input with weak internal pull-down	UART data input active low (idle status high)
UART_RTS	H7	CMOS output, tristatable with weak internal pull-up	UART request to send active low
UART_CTS	H8	CMOS input with weak internal pull-down	UART clear to send active low
USB_DP	J8	Bi-directional	USB data plus with selectable internal 1.5kΩ pull-up resistor
USB_DN	K8	Bi-directional	USB data minus

Test and Debug	Ball	Pad Type	Description
RESET	C7	CMOS input with weak internal pull-down	Reset if high. Input debounced so must be high for >5ms to cause a reset
RESET_B	D8	CMOS input with weak internal pull-up	Reset if low. Input debounced so must be low for >5ms to cause a reset
SPI_CSB	C9	CMOS input with weak internal pull-up	Chip select for Serial Peripheral Interface, active low
SPI_CLK	C10	CMOS input with weak internal pull-down	Serial Peripheral Interface clock
SPI_MOSI	C8	CMOS input with weak internal pull-down	Serial Peripheral Interface data input
SPI_MISO	B9	CMOS output, tristatable with weak internal pull-down	Serial Peripheral Interface data output
TEST_EN	C6	CMOS input with strong internal pull-down	For test purposes only (leave unconnected)
FLASH_EN	B8	No pad	Pull high to VDD_MEM for compatibility with flash parts

PIO Port	Ball	Pad Type	Description
PIO[2]	B3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[3]	B4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[4]	E8	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[5]	F8	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[6]	F10	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[7]	F9	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[8]	C5	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[9]	C3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[10]	C4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[11]	E3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
AIO[0]	H4	Bi-directional	Programmable input/output line
AIO[1]	H5	Bi-directional	Programmable input/output line
AIO[2]	J5	Bi-directional	Programmable input/output line

Power Supplies and Control	Ball	Pad Type	Description
VREG_IN	K6	Regulator input	Linear regulator voltage input
VDD_USB	K9	VDD	Positive supply for UART/USB ports
VDD_PIO	A3	VDD	Positive supply for PIO and AUX DAC(1)
VDD_PADS	D10	VDD	Positive supply for all other digital input/output ports(2)
VDD_MEM	A6,A7, A9, H6, J6, K7	VDD	Positive supply AIO ports (and flash memory on flash parts)
VDD_CORE	E10	VDD	Positive supply for internal digital circuitry and internal ROM
VDD_RADIO	C1, C2	VDD	Positive supply for RF circuitry
VDD_VCO	H1	VDD	Positive supply for VCO and synthesiser circuitry
VDD_ANA	K4	VDD/Regulator output	Positive supply for analogue circuitry and 1.8V regulated output
VSS_PADS	A1, A2, D9, J9, K10	VSS	Ground connection for input/output
VSS_MEM	A10, B5, B7, B10, J7	VSS	Ground connections AIO ports (and flash memory on flash parts)
VSS_CORE	E9	VSS	Ground connection for internal digital circuitry and internal ROM
VSS_RADIO	D2, E2, F2	VSS	Ground connections for RF circuitry
VSS_VCO	G1, G2	VSS	Ground connections for VCO and synthesiser
VSS_ANA	J2, J4, K2	VSS	Ground connections for analogue circuitry
VSS	F3	VSS	Ground connection for internal package shield

Unconnected Terminals	Ball	Description
	A4, A5, A8, B6, G3, H3, J1, K1, K5	Leave unconnected

Notes:

(1) Positive supply for PIO[3:0] and PIO[11:8]

(2) Positive supply for SPI/PCM ports and PIO[7:4]

See Section 4, Electrical Characteristics, for voltage specifications

3 4 x 4 CSP Package Information

3.1 BC213143AXX-XB Pinout Diagram

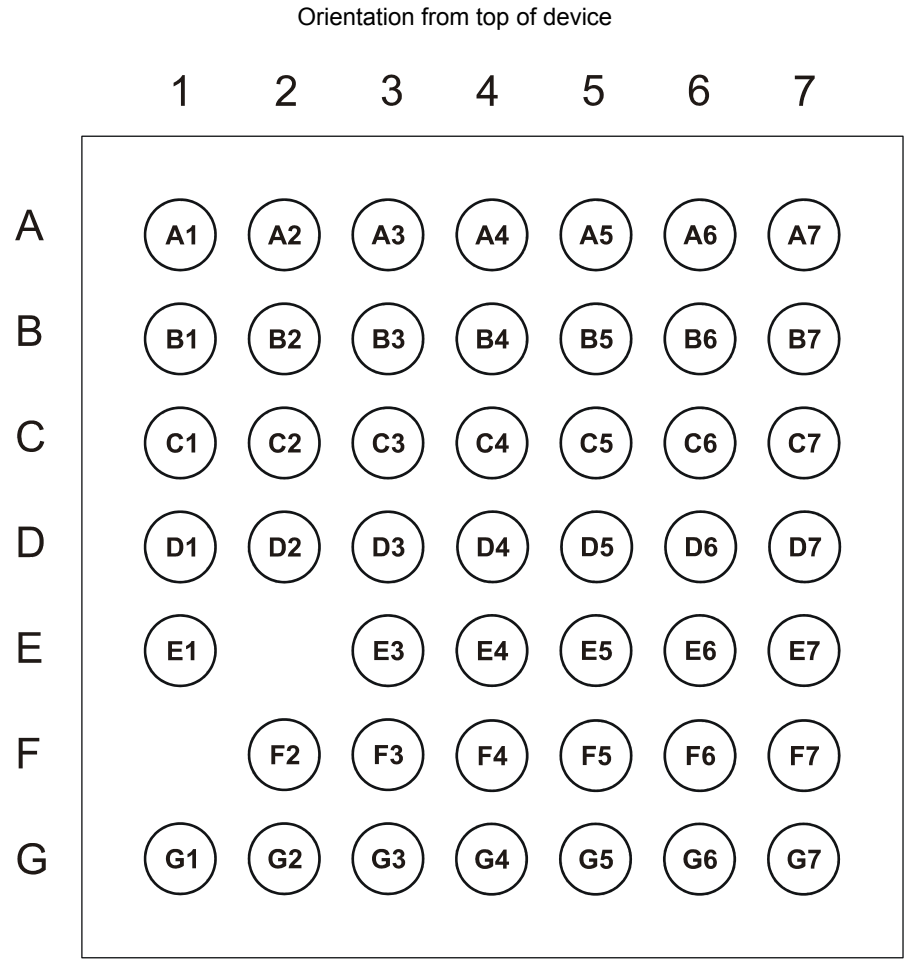


Figure 3.1: BlueCore2-ROM 4 x 4mm CSP Package (BC213143AXX-XB)

Note:

Performance and characterisation data reported is not guaranteed for the CSP package option. All data should be regarded as Pre-Production Information with respect to the CSP package.

3.2 Device Terminal Functions

Radio	Ball	Pad Type	Description
PIO[0]/RXEN	G3	Bi-directional with programmable strength internal pull-up/down	Control output for external LNA (if fitted) (=PIO[0])
PIO[1]/TXEN	E3	Bi-directional with programmable strength internal pull-up/down	Control output for external PA Class 1 only (=PIO[1])
TX_A	G2	Analogue	Transmitter output/Switched Receiver input
TX_B	G1	Analogue	Complement of TX_A
AUX_DAC	F2	Analogue	Voltage DAC output

Synthesiser and Oscillator	Ball	Pad Type	Description
XTAL_IN	A1	Analogue	For crystal or external clock input
XTAL_OUT	A2	Analogue	Drive for crystal

PCM Interface	Ball	Pad Type	Description
PCM_OUT	C7	CMOS output, tristatable with weak internal pull-down	Synchronous data output
PCM_IN	C5	CMOS input, with weak internal pull-down	Synchronous data input
PCM_SYNC	C6	Bi-directional with weak internal pull-down	Synchronous data sync
PCM_CLK	D5	Bi-directional with weak internal pull-down	Synchronous data clock

USB and UART	Ball	Pad Type	Description
UART_TX	B7	CMOS output, tristatable with weak internal pull-up	UART data output active low
UART_RX	B6	CMOS input with weak internal pull-down	UART data input active low (idle status high)
UART_RTS	B5	CMOS output, tristatable with weak internal pull-up	UART request to send active low
UART_CTS	C4	CMOS input with weak internal pull-down	UART clear to send active low
USB_DP	A5	Bi-directional	USB data plus with selectable internal 1.5kΩ pull-up resistor
USB_DN	A6	Bi-directional	USB data minus

Test and Debug	Ball	Pad Type	Description
RESETB	E4	CMOS input with weak internal pull-up	Reset if low. Input debounced so must be low for >5ms to cause a reset
SPI_CSB	G6	CMOS input with weak internal pull-up	Chip select for Synchronous Serial Interface active low
SPI_CLK	F5	CMOS input with weak internal pull-down	Serial Peripheral Interface clock
SPI_MOSI	F7	CMOS input with weak internal pull-down	Serial Peripheral Interface data input
SPI_MISO	G7	CMOS output, tristatable with weak internal pull-down	Serial Peripheral Interface data output
TEST_EN	D2	CMOS input with strong internal pull-down	For test purposes only (leave unconnected)

PIO Port	Ball	Pad Type	Description
PIO[2]	D3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[3]	F4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[4]	E5	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[5]	D7	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[6]	D6	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[7]	D4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[8]	F3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
AIO[0]	B3	Bi-directional	Programmable input/output line
AIO[1]	C2	Bi-directional	Programmable input/output line
AIO[2]	C3	Bi-directional	Programmable input/output line

Power Supplies and Control	Ball	Pad Type	Description
VREG_IN	A4	Regulator input	Linear regulator voltage input
VDD_USB	B4	VDD	Positive supply for UART/USB and AIO ports
VDD_PIO	G5	VDD	Positive supply for PIO and AUX DAC(1)
VDD_PADS	F6	VDD	Positive supply for all other digital input/output ports(2)
VDD_CORE	E6	VDD	Positive supply for internal digital circuitry
VDD_RADIO	D1	VDD	Positive supply for RF circuitry
VDD_VCO	B1	VDD	Positive supply for VCO and synthesiser circuitry
VDD_ANA	A3	VDD	Positive supply for analogue circuitry and 1.8V regulated output
VSS_PADS	A7, E7, G4	VSS	Ground connection for internal digital circuitry and input/output
VSS_RADIO	E1	VSS	Ground connections for RF circuitry
VSS_VCO	C1	VSS	Ground connections for VCO and synthesiser
VSS_ANA	B2	VSS	Ground connections for analogue circuitry

Notes:

(1) Positive supply for PIO[3:0] and PIO[8].

(2) Positive supply for SPI/PCM ports and PIO[7:4].

4 Electrical Characteristics

Absolute Maximum Ratings		
Rating	**Min**	**Max**
Storage Temperature	-40°C	150°C
Supply Voltage: VDD_RADIO, VDD_VCO, VDD_ANA, VDD_CORE and VDD_MEM	-0.4V	2.2V
Supply Voltage: VDD_PADS, VDD_PIO, VDD_USB	-0.4V	3.7V
Supply Voltage: VREG_IN	-0.4V	4.2V
Other Terminal Voltages	VSS-0.4V	VDD+0.4V

Recommended Operating Conditions		
Operating Condition	**Min**	**Max**
Guaranteed RF performance range	-40°C	105°C
Supply Voltage: VDD_RADIO, VDD_VCO, VDD_ANA, VDD_CORE and VDD_MEM	1.7V	1.9V
Supply Voltage: VDD_PADS, VDD_PIO, VDD_USB	1.7V	3.6V
Supply Voltage: VREG_IN(1)	2.2V	3.6V(2)

Note:

(1) If the internal linear regulator is not required VREG_IN should be connected to 1.8V.

(2) The device will operate with VREG_IN as high as 4.2V, however performance is not guaranteed above 3.6V.

Input/Output Terminal Characteristics[1]				
Linear Regulator	**Min**	**Typ**	**Max**	**Unit**
Normal Operation				
Output Voltage (Iload = 70mA / VREG_IN = 3.0V)	1.70	1.78	1.85	V
Temperature Coefficient	-250	-	250	ppm/C
Output Noise[2][3]	-	-	1	mV rms
Load Regulation (Iload < 100mA)[8]	-	-	50	mV/A
Settling Time[2][4]	-	-	50	µs
Line Regulation[2][5]	-20	-	-	dB
Maximum Output Current	100	-	-	mA
Minimum Load Current	5	-	-	µA
Dropout Voltage (Iload = 70mA)	-	-	350	mV
Quiescent Current (excluding load, Iload <1mA)	25	35	50	µA
Low Power Mode[6]				
Quiescent Current (excluding load, Iload <100µA)	4	7	10	µA
Disabled Mode[7]				
Quiescent Current	1.5	2.5	3.5	µA

Notes:

(1) These parameters are guaranteed for 2.2 to 3.6V. Between 3.6V and 4.2V the output voltage is not guaranteed to remain below 1.85V, but full functionality of the chip will be preserved and no damage will ensue.

(2) Regulator output connected to 47nF pure and 4.7µF 2.2Ω ESR capacitors

(3) Frequency range 100Hz to 100kHz

(4) 1mA to 70mA pulsed load

(5) Frequency range 100Hz to 10MHz

(6) Low power mode is entered and exited automatically when the chip enters/leaves Deep Sleep mode

(7) Regulator is disabled when VREG_IN is either open circuit or driven to the same voltage as VDD_ANA

(8) On-chip voltage: This figure does not include bondwire or ball-to-PCB resistance effects.

Input/Output Terminal Characteristics (Continued)					
Digital Terminals		**Min**	**Typ**	**Max**	**Unit**
Input Voltage Levels					
V_{IL} input logic level low	2.7 ≤VDD ≤3.6	-0.4	-	0.8	V
	1.7 ≤VDD ≤1.9	-0.4	-	0.4	V
V_{IH} input logic level high		0.7VDD	-	VDD+0.4	V
Output Voltage Levels					
V_{OL} output logic level low, (I_O = 4.0mA)	2.7 ≤VDD ≤3.6	-	-	0.2	V
V_{OL} output logic level low, (I_O = 4.0mA)	1.7 ≤VDD ≤1.9	-	-	0.4	V
V_{OH} output logic level high, (I_O = -4.0mA)	2.7 ≤VDD ≤3.6	VDD-0.2	-	-	V
V_{OH} output logic level high, (I_O = -4.0mA)	1.7 ≤VDD ≤1.9	VDD-0.4	-	-	V
Input and Tristate Current with					
Strong pull-up		-100	-40	-10	µA
Strong pull-down		10	40	100	µA
Weak pull-up		-5	-1	0	µA
Weak pull-down		0	1	5	µA
I/O pad leakage current		-1	0	1	µA
CI Input Capacitance		1.0	-	5.0	pF

USB Terminals(1)	**Min**	**Typ**	**Max**	**Unit**
Input Threshold				
V_{IL} input logic level low	-	-	0.3 VDD_USB	V
V_{IH} input logic level high	0.57 VDD_USB	-	-	V
Input Leakage Current				
VSS_USB <V_{IN}< VDD_USB(2)	-1	1	5	µA
CI Input capacitance	2.5	-	10.0	pF
Output Voltage Levels To Correctly Terminated USB Cable				
V_{OL} output logic level low	0.0	-	0.2	V
V_{OH} output logic level high	2.8	-	VDD_USB	V

Input/Output Terminal Characteristics (Continued)				
Auxiliary DAC, 8-Bit Resolution	**Min**	**Typ**	**Max**	**Unit**
Resolution	-	-	8	Bits
Average output step size(3)	12.5	14.5	17.0	mV
Output Voltage		Monotonic(3)		
Voltage range (I_O=0mA)	VSS_PIO	-	VDD_PIO	V
Current range	-10.0	-	+0.1	mA
Minimum output voltage (I_O=100µA)	0.0	-	0.2	V
Maximum output voltage (I_O=10mA)	VDD_PIO-0.3	-	VDD_PIO	V
High Impedance leakage current	-1	-	1	µA
Offset	-220	-	120	mV
Integral non linearity(3)	-2	-	2	LSB
Starting time (50pF load)	-	-	10	µs
Settling time (50pF load)	-	-	5	µs

Crystal Oscillator	**Min**	**Typ**	**Max**	**Unit**
Crystal frequency(4) (7)	8.0	-	32.0	MHz
Digital trim range(5)	5.0	6.2	8.0	pF
Trim step size	-	0.1	-	pF
Transconductance	2.0	-	-	mS
Negative resistance(6)	870	1500	2400	Ω
External Clock				
Input frequency(7)	7.5	-	40.0	MHz
Clock input level(8)	0.4	-	VDD_ANA	V pk-pk
Phase noise (at zero crossing)	-	-	15	ps rms
XTAL_IN input impedance	10	-	-	kΩ
XTAL_IN input capacitance	-	7	10	pF
Power-on Reset				
VDD_CORE falling threshold	1.40	1.50	1.60	V
VDD_CORE rising threshold	1.50	1.60	1.70	V
Hysteresis	0.05	0.10	0.15	V

Notes:

VDD_CORE, VDD_RADIO, VDD_VCO, VDD_ANA and VDD_MEM are at 1.8V unless shown otherwise.

VDD_PADS, VDD_PIO and VDD_USB are at 3.0V unless shown otherwise

The same setting of the digital trim is applied to both XTAL_IN and XTAL_OUT.

Current drawn into a pin is defined as positive, current supplied out of a pin is defined as negative.

(1) 3.1V ≤VDD_USB ≤3.6V

(2) Internal USB pull-up disabled

(3) Specified for an output voltage between 0.2V and VDD_PIO -0.3V

(4) Integer multiple of 250kHz

(5) The difference between the internal capacitance at minimum and maximum settings of the internal digital trim

(6) XTAL frequency = 16MHz (Please refer to your software build release note for frequencies supported); XTAL C0 = 0.75pF; XTAL load capacitance = 8.5pF

(7) Clock input can be any frequency between 8 and 40MHz in steps of 250kHz + CDMA/3G TCXO frequencies of 7.68, 14.4, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz

(8) Clock input can either be sinusoidal or square wave. If the peaks of the signal are below VSS_ANA or above VDD_ANA a DC blocking capacitor is required between the signal and XTAL_IN

5 Radio Characteristics

Important Notes

BlueCore2-ROM meets the Bluetooth specification v1.1 and v1.2 when used in a suitable application circuit between -40°C and +105°C.

All data presented in the Radio Characteristics section was measured using the application circuit shown in Figure 10.63 unless otherwise stated.

All data presented in the Radio Characteristics section was measured using a PSKEY_LC_MAX_TX_POWER setting of 3 which corresponds to a PSKEY_LC_POWER_TABLE power table entry of 55 unless otherwise stated.

Performance and characterisation data reported is not guaranteed for the CSP package option. All data should be regarded as Pre-Production Information with respect to the CSP package

Tx output is guaranteed to be unconditionally stable over the guaranteed temperature range.

5.1 Temperature +20°C

5.1.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +20°C						
		Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Maximum RF transmit power[1][2]		3	6.5	-	-6 to +4[3]	dBm
Variation in RF power over temperature range with compensation enabled (+/-)[4]		-	0.5	1	~	dB
Variation in RF power over temperature range with compensation disabled (+/-)[4]		-	2	3	~	dB
Emitted power in cellular bands measured at chip terminals Output power ≤4dBm	**Frequency (GHz)**					
	0.869 – 0.894[5]	-	-133	-130	-	dBm/Hz
	0.925 – 0.960[5]	-	-143	-138		
	1.570 – 1.580[6]	-	-138	-135		
	1.805 – 1.880[5]	-	-131	-115		
	1.930 – 1.990[7]	-	-135	-125		
	1.930 – 1.990[5]	-	-135	-126		
	1.930 – 1.990[8]	-	-137	-130		
	2.110 – 2.170[8]	-	-132	-122		
	2.110 – 2.170[9]	-	-135	-127		
RF power control range		25	35	-	≥16	dB
RF power range control resolution [10]		-	0.5	1.2	-	dB
20dB bandwidth for modulated carrier		-	820	1000	≤1000	kHz
Adjacent channel transmit power $F=F_0 \pm 2MHz$[11][12]		-	-35	-20	≤-20	dBm
Adjacent channel transmit power $F=F_0 \pm 3MHz$[11][12]		-	-45	-40	≤-40	dBm
Adjacent channel transmit power $F=F_0 > \pm 3MHz$[11][12]		-	-50	-	≤-40	dBm
Δf1avg “Maximum Modulation”		140	165	175	$140 < \Delta f1_{avg} < 175$	kHz
Δf2max “Minimum Modulation”		115	140	-	115	kHz
Δf2avg / Δf1avg		0.8	0.9	-	≥0.80	-
Initial carrier frequency tolerance		-	10	35	±75	kHz

Radio Characteristics VDD = 1.8V Temperature = +20°C (continued)					
	Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Drift Rate	-	8	20	≤20	kHz/50µs
Drift (single slot packet)	-	9	20	≤25	kHz
Drift (five slot packet)	-	10	25	≤40	kHz
2nd Harmonic Content	-	-60	-50	≤30	dBm
3rd Harmonic Content	-	-55	-45	≤30	dBm

Notes:

(1) BlueCore2-ROM firmware maintains the transmit power to be within the Bluetooth specification v1.1 and v1.2 limits

(2) Measurement made using a PSKEY_LC_MAX_TX_POWER setting corresponds to a PSKEY_LC_POWER_TABLE power table entry of 63

(3) Class 2 RF transmit power range, Bluetooth specification v1.1 and v1.2

(4) To some extent these parameters are dependent on the matching circuit used, and its behaviour over temperature. Therefore these parameters may be beyond CSR's direct control

(5) Integrated in 200kHz bandwidth

(6) Integrated in 1MHz bandwidth

(7) Integrated in 30kHz bandwidth

(8) Integrated in 1.2MHz bandwidth

(9) Integrated in 5MHz bandwidth

(10) Resolution guaranteed over the range -5dB to -25dB relative to maximum power for Tx Level >20 (see Figure 10.4)

(11) Measured at F_0 = 2441MHz

(12) Up to three exceptions are allowed in v1.1 and v1.2 of the Bluetooth specification. BlueCore2-ROM is guaranteed to meet the ACP performance as specified by the Bluetooth specification v1.1 and v1.2

5.1.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = +20°C						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER for all packet types	2.402	-	-84	-80	≤-70	dBm
	2.441	-	-85	-81		
	2.480	-	-85	-81		
Maximum received signal at 0.1% BER		0	3	-	≥-20	dBm
Continuous power in cellular bands required to block Bluetooth reception (for sensitivity of -67dBm with 0.1% BER) measured at chip terminals	**Frequency (GHz)**					
	0.824 – 0.849[1][6]	-2	2	-	-	dBm
	0.880 – 0.915[6]	5	7	-	-	
	1.710 – 1.785[6]	3	6	-	-	
	1.850 – 1.910[6]	1	5	-	-	
	1.920 – 1.980[7]	-8	-6	-	-	
Continuous power in cellular bands required to block Bluetooth reception (for sensitivity of -80dBm with 0.1% BER) measured at chip terminals	0.824 – 0.849[1] [6]	-10	-5	-	-	dBm
	0.880 – 0.915[6]	-8	-4	-	-	
	1.710 – 1.785[6]	-7	-3	-	-	
	1.850 – 1.910[6]	-11	-4	-	-	
	1.920 – 1.980[7]	-18	-14	-	-	
Continuous power required to block Bluetooth reception (for sensitivity of -67dBm with 0.1% BER) measured at chip terminals	**Frequency (MHz)**					dBm
	30 – 2000	-10	> +10	-	-	
	2000 – 2200	-27	> 0	-	-	
	2200 – 2399	-27	> -20	-	-	
	2498 – 2700	-27	> -20	-	-	
	2700 – 3000	-27	> 0	-	-	
	3000 – 12750	-10	> 8	-	-	
	BT freq / 2 ±2Mhz	-30	-25	-	-	
	N*BT freq ±2MHz	-30	-25	-	-	
C/I co-channel		-	9	11	≤11	dB
Adjacent channel selectivity C/I $F=F_0+1MHz$[2] [3]		-	-4	0	≤0	dB
Adjacent channel selectivity C/I $F=F_0-1MHz$[2] [3]		-	-4	0	≤0	dB
Adjacent channel selectivity C/I $F=F_0+2MHz$[2] [3]		-	-35	-30	≤-30	dB
Adjacent channel selectivity C/I $F=F_0-2MHz$[2] [3]		-	-21	-20	≤-20	dB
Adjacent channel selectivity C/I $F\geq F_0+3MHz$[2] [3]		-	-45	-40	≤-40	dB
Adjacent channel selectivity C/I $F\leq F_0-5MHz$[2] [3]		-	-45	-40	≤-40	dB
Adjacent channel selectivity C/I $F=F_{Image}$[2] [3]		-	-18	-9	≤-9	dB
Maximum level of intermodulation interferers [4]		-	-30	-39	≥-39	dBm
Spurious output level[5]		-	-140	-	~	dBm/Hz

Notes:

(1) $| 3f_{Blocking} - f_{Bluetooth} | > 4MHz$

(2) Up to five exceptions are allowed in v1.1 and v1.2 of the Bluetooth specification. BlueCore2-ROM is guaranteed to meet the C/I performance as specified by the Bluetooth specification v1.1 and v1.2.

(3) Measured at F_0 = 2405MHz, 2441MHz, 2477MHz

(4) Measured at f1-f2 = 5MHz. Measurement is performed in accordance with Bluetooth RF test RCV/CA/05/c. i.e. wanted signal at -64dBm

(5) Integrated in 100kHz bandwidth. Actual figure is typically below -140dBm/Hz except for peaks of -125dBm/Hz at 1.2GHz and -100dBm/Hz in-band at 2.4GHz

(6) GSM band

(7) W-CDMA band

5.2 Temperature -40°C

5.2.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = -40°C					
	Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Maximum RF transmit power(1)	4	8	-	-6 to +4(2)	dBm
RF power control range	25	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	820	1000	≤1000	kHz
Adjacent channel transmit power F=F_0 ±2MHz(3) (4)	-	-35	-20	≤-20	dBm
Adjacent channel transmit power F=F_0 ±3MHz(3) (4)	-	-45	-40	≤-40	dBm
Δf1avg “Maximum Modulation”	140	165	175	140<$\Delta f1_{avg}$<175	kHz
Δf2max “Minimum Modulation”	115	135	-	115	kHz
Δf2avg / Δf1avg	0.8	0.9	-	≥0.80	-
Initial carrier frequency tolerance	-	10	35	±75	kHz
Drift Rate	-	8	20	≤20	kHz/50μs
Drift (single slot packet)	-	9	25	≤25	kHz
Drift (five slot packet)	-	10	40	≤40	kHz

Notes:

(1) BlueCore2-ROM firmware maintains the transmit power to be within the Bluetooth specification v1.1 and v1.2 limits

(2) Class 2 RF transmit power range, Bluetooth specification v1.1 and v1.2

(3) Measured at F_0 = 2441MHz

(4) Up to three exceptions are allowed in v1.1 and v1.2 of the Bluetooth specification

5.2.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = -40°C						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER for all packet types	2.402	-	-86.0	-81	≤-70	dBm
	2.441	-	-88.0	-82		
	2.480	-	-86.5	-82		
Maximum received signal at 0.1% BER		-2	1	-	≥-20	dBm

5.3 Temperature -25°C

5.3.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = -25°C					
	Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Maximum RF transmit power(1)	3.5	7	-	-6 to +4(2)	dBm
RF power control range	25	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	820	1000	≤1000	kHz
Adjacent channel transmit power F=F_0 ±2MHz(3) (4)	-	-35	-20	≤-20	dBm
Adjacent channel transmit power F=F_0 ±3MHz(3) (4)	-	-45	-40	≤-40	dBm
Δf1avg "Maximum Modulation"	140	165	175	140<$\Delta f1_{avg}$<175	kHz
Δf2max "Minimum Modulation"	115	140	-	115	kHz
Δf2avg / Δf1avg	0.8	0.9	-	≥0.80	-
Initial carrier frequency tolerance	-	10	35	±75	kHz
Drift Rate	-	8	20	≤20	kHz/50μs
Drift (single slot packet)	-	9	20	≤25	kHz
Drift (five slot packet)	-	10	25	≤40	kHz

Notes:

(1) BlueCore2-ROM firmware maintains the transmit power to be within the Bluetooth specification v1.1 and v1.2 limits

(2) Class 2 RF transmit power range, Bluetooth specification v1.1 and v1.2

(3) Measured at F_0 = 2441MHz

(4) Up to three exceptions are allowed in v1.1 and v1.2 of the Bluetooth specification

5.3.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = -25°C						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER for all packet types	2.402	-	-85.5	-81	≤-70	dBm
	2.441	-	-86.5	-82		
	2.480	-	-86.5	-82		
Maximum received signal at 0.1% BER		-2	1	-	≥-20	dBm

5.4 Temperature +85°C

5.4.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +85°C					
	Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Maximum RF transmit power(1)	0	3	-	-6 to +4(2)	dBm
RF power control range	25	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	820	1000	≤1000	kHz
Adjacent channel transmit power F=F_0 ±2MHz(3) (4)	-	-33	-20	≤-20	dBm
Adjacent channel transmit power F=F_0 ±3MHz(3) (4)	-	-43	-40	≤-40	dBm
Δf1avg "Maximum Modulation"	140	165	175	140<$\Delta f1_{avg}$<175	kHz
Δf2max "Minimum Modulation"	115	140	-	115	kHz
Δf2avg / Δf1avg	0.8	0.9	-	≥0.80	-
Initial carrier frequency tolerance	-	10	35	±75	kHz
Drift Rate	-	9	20	≤20	kHz/50µs
Drift (single slot packet)	-	9	20	≤25	kHz
Drift (five slot packet)	-	10	28	≤40	kHz

Notes:

(1) BlueCore2-ROM firmware maintains the transmit power to be within the Bluetooth specification v1.1and v1.2 limits

(2) Class 2 RF transmit power range, Bluetooth specification v1.1 and v1.2

(3) Measured at F_0 = 2441MHz

(4) Up to three exceptions are allowed in v1.1 and v1.2 of the Bluetooth specification

5.4.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = +85°C						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER for all packet types	2.402	-	-81	-77	≤-70	dBm
	2.441	-	-83	-79		
	2.480	-	-83	-79		
Maximum received signal at 0.1% BER		0	5	-	≥-20	dBm

5.5 Temperature +105°C

5.5.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +105°C					
	Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Maximum RF transmit power(1)	-2.5	1	-	-6 to +4(2)	dBm
RF power control range	25	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	820	1000	≤1000	kHz
Adjacent channel transmit power $F=F_0 \pm 2MHz$(3) (4)	-	-35	-20	≤-20	dBm
Adjacent channel transmit power $F=F_0 \pm 3MHz$(3) (4)	-	-45	-40	≤-40	dBm
Δf1avg "Maximum Modulation"	140	165	175	$140<\Delta f1_{avg}<175$	kHz
Δf2max "Minimum Modulation"	-	135	-	115	kHz
Δf2avg / Δf1avg	-	0.9	-	≥0.80	-
Initial carrier frequency tolerance	-	10	35	±75	kHz
Drift Rate	-	9	20	≤20	kHz/50µs
Drift (single slot packet)	-	9	25	≤25	kHz
Drift (five slot packet)	-	10	40	≤40	kHz

Notes:

(1) BlueCore2-ROM firmware maintains the transmit power to be within the Bluetooth specification v1.1and v1.2 limits

(2) Class 2 RF transmit power range, Bluetooth specification v1.1 and v1.2

(3) Measured at F_0 = 2441MHz

(4) Up to three exceptions are allowed in v1.1 and v1.2 of the Bluetooth specification

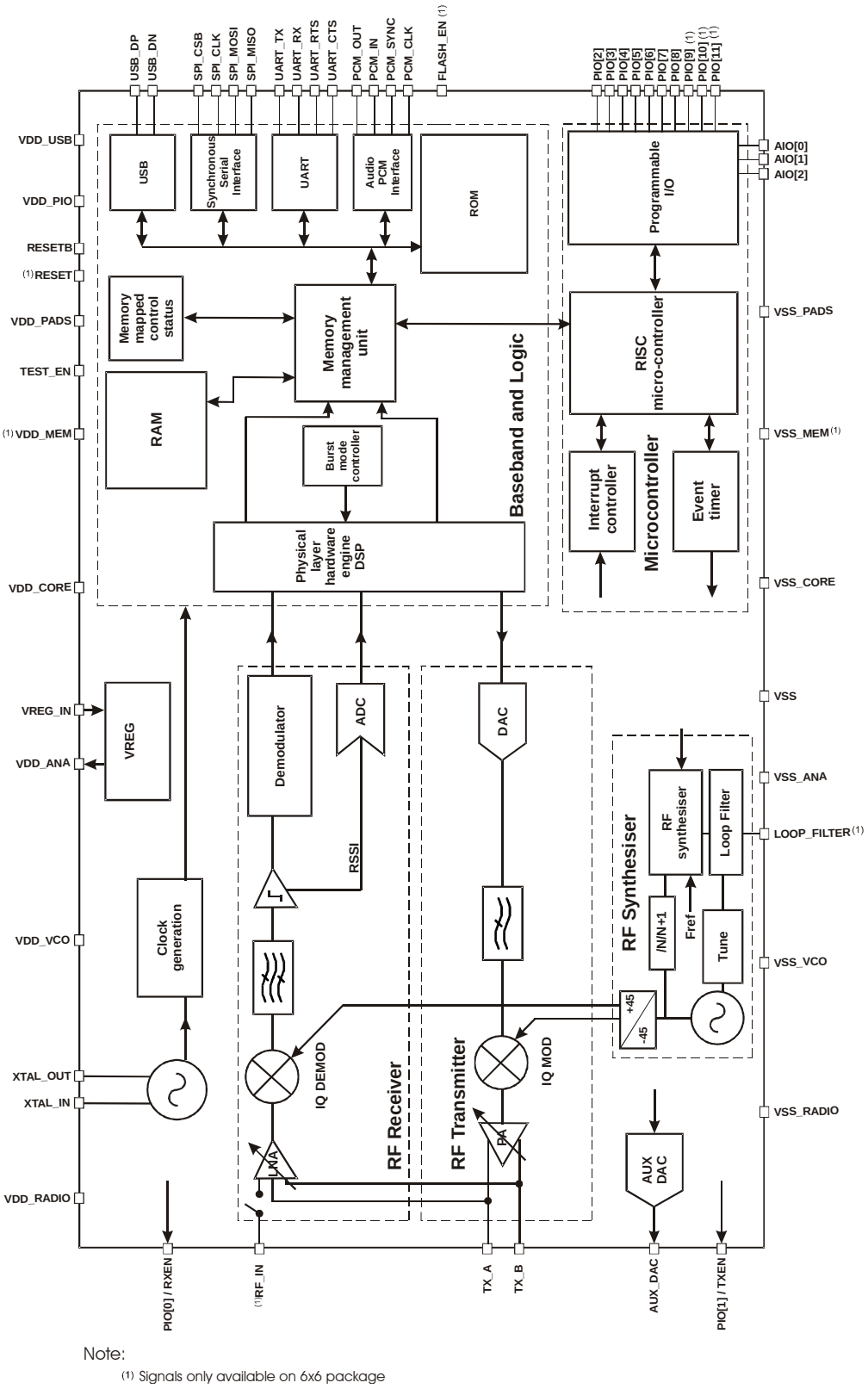
5.5.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = +105°C						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER for all packet types	2.402	-	-81	-77	≤-70	dBm
	2.441	-	-82	-78		
	2.480	-	-82	-78		
Maximum received signal at 0.1% BER		0	5	-	≥-20	dBm

5.6 Power Consumption

Mode	Average	Unit
SCO connection HV3 (30ms interval Sniff Mode) (Slave)	26.0	mA
SCO connection HV3 (30ms interval Sniff Mode) (Master)	26.0	mA
SCO connection HV3 (No Sniff Mode) (Slave)	32.0	mA
SCO connection HV1 (Slave)	43.0	mA
SCO connection HV1 (Master)	43.0	mA
ACL data transfer 115.2kbps UART no traffic (Master)	7.0	mA
ACL data transfer 115.2kbps UART no traffic (Slave)	24.0	mA
ACL data transfer 720kbps UART (Master or Slave)	50.0	mA
ACL data transfer 720kbps USB (Master or Slave)	50.0	mA
ACL connection, Sniff Mode 40ms interval, 38.4kbps UART	4.0	mA
ACL connection, Sniff Mode 1.28s interval, 38.4kbps UART	0.5	mA
Parked Slave, 1.28s beacon interval, 38.4kbps UART	0.6	mA
Standby Mode (Connected to host, no RF activity)	85.0	µA
Reset (RESET high or RESETB low)	50.0	µA

6 Device Diagrams



Note:
(1) Signals only available on 6x6 package

Figure 6.1: BlueCore2-ROM Device Diagram for 6 x 6mm VFBGA and 4 x 4mm CSP Packages

7 Description of Functional Blocks

7.1 RF Receiver

The receiver features a near zero Intermediate Frequency (IF) architecture that allows the channel filters to be integrated on to the die. Sufficient out of band blocking specification at the Low Noise Amplifier (LNA) input allows the radio to be used in close proximity to Global System for Mobile Communications (GSM) and Wideband Code Division Multiple Access (W-CDMA) cellular phone transmitters without being desensitised. The use of a digital Frequency Shift Keying (FSK) discriminator means that no discriminator tank is needed, and its excellent performance in the presence of noise allows BlueCore2-ROM to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

7.1.1 Low Noise Amplifier

The LNA can be configured to operate in single ended or differential mode. Single ended mode is used for Class 1 Bluetooth operation and differential mode is used for Class 2 operation.

7.1.2 Analogue to Digital Converter

The analogue to digital converter (ADC) is used to implement fast automatic gain control (AGC). The ADC samples the Received Signal Strength Indicator (RSSI) voltage on a slot by slot basis. The front end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference limited environments.

7.2 RF Transmitter

7.2.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise the frequency drift during a transmit timeslot which results in a controlled modulation index. A digital baseband transmit filter provides the required spectral shaping.

7.2.2 Power Amplifier

The internal power amplifier (PA) has a maximum output power of +6dBm allowing BlueCore2-ROM to be used in Class 2 and Class 3 radios without an external RF PA. Support for transmit power control allows a simple implementation for Class 1 with an external RF PA.

7.2.3 Auxiliary DAC

An 8-bit voltage Auxiliary DAC is provided for power control of an external PA for Class 1 operation.

7.3 RF Synthesiser

The radio synthesiser is fully integrated onto the die with no requirement for an external voltage controlled oscillator (VCO) screening can, varactor tuning diodes, LC resonators or loop filter. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth specification v1.1 and v1.2.

7.4 Clock Input and Generation

The reference clock for the system is generated from a TCXO or crystal input between 8 and 40MHz. All internal reference clocks are generated using a phase locked loop (PLL), which is locked to the external reference frequency.

7.5 Baseband and Logic

7.5.1 Memory Management Unit

The memory management unit (MMU) provides a number of dynamically allocated ring buffers that hold the data which is in transit between the host and the air or vice versa. The dynamic allocation of memory ensures efficient use of the available random access memory (RAM) and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers.

7.5.2 Burst Mode Controller

During radio transmission the burst mode controller (BMC) constructs a packet from header information previously loaded into memory mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During radio reception, the BMC stores the packet header in memory mapped

registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

7.5.3 Physical Layer Hardware Engine DSP

Dedicated logic is used to perform the following:

- Forward error correction (FEC)
- Header error control (HEC)
- Cyclic redundancy check (CRC)
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding
- The following voice data translations and operations are performed by firmware:
  - A-law/μ-law/linear voice data from host
  - A-law/μ-law/Continuously Variable Slope Delta (CVSD) over the air
  - Voice interpolation for lost packets
  - Rate mismatches

7.5.4 RAM

32Kbytes of on chip RAM is provided and is shared between the ring buffers used to hold voice/data for each active connection and the general purpose memory required by the Bluetooth stack.

7.5.5 ROM

4Mbits of metal programmable ROM is provided for system firmware implementation.

7.5.6 USB

This is a full speed universal serial bus (USB) interface for communicating with other compatible digital devices. BlueCore2-ROM acts as a USB peripheral, responding to requests from a Master host controller such as a PC.

7.5.7 Synchronous Serial Interface

This is a synchronous serial port interface (SPI) for interfacing with other digital devices. The SPI port can be used for system debugging.

7.5.8 UART

This is a standard Universal Asynchronous Receiver Transmitter (UART) interface for communicating with other serial devices.

7.5.9 Audio PCM Interface

The audio pulse code modulation (PCM) Interface supports continuous transmission and reception of PCM encoded audio data over Bluetooth.

7.6 Microcontroller

The microcontroller, interrupt controller and event timer run the Bluetooth software stack and control the radio and host interfaces. A 16-bit reduced instruction set computer (RISC) microcontroller is used for low power consumption and efficient use of memory.

7.6.1 Programmable I/O

BlueCore2-ROM has up to 15 (12 digital and 3 analogue) programmable I/O terminals. These are controlled by firmware running on the device.

8 CSR Bluetooth Software Stacks

8.1 Important Information

Due to the nature of a ROM device the initial boot configuration of CSR's generic ROM part is fixed to a predetermined default configuration. Areas covered include clock frequency, host transport, baud rate, persistent store values, etc.

To reconfigure the device to meet a design's requirements the PIO lines are read during the initial cold boot procedure and the device is reprogrammed accordingly. These new settings are activated after sending a warm reset to the device.

For details of the implementation and the PIO line configurations please refer to latest software release note.

BlueCore2-ROM is supplied with Bluetooth stack firmware which runs on the internal RISC microcontroller. This is compliant with the Bluetooth specification v1.1 and v1.2.

The BlueCore2-ROM software architecture allows Bluetooth processing overheads to be shared in different ways between the internal RISC microcontroller and the host processor. The upper layers of the Bluetooth stack (above HCI) can be run either on chip or on the host processor.

Running the upper stack on BlueCore2-ROM reduces or eliminates in the case of a virtual machine (VM) application, the need for host side software and processing time. Running the upper layers on the host processor allows greater flexibility.

8.2 BlueCore HCI Stack

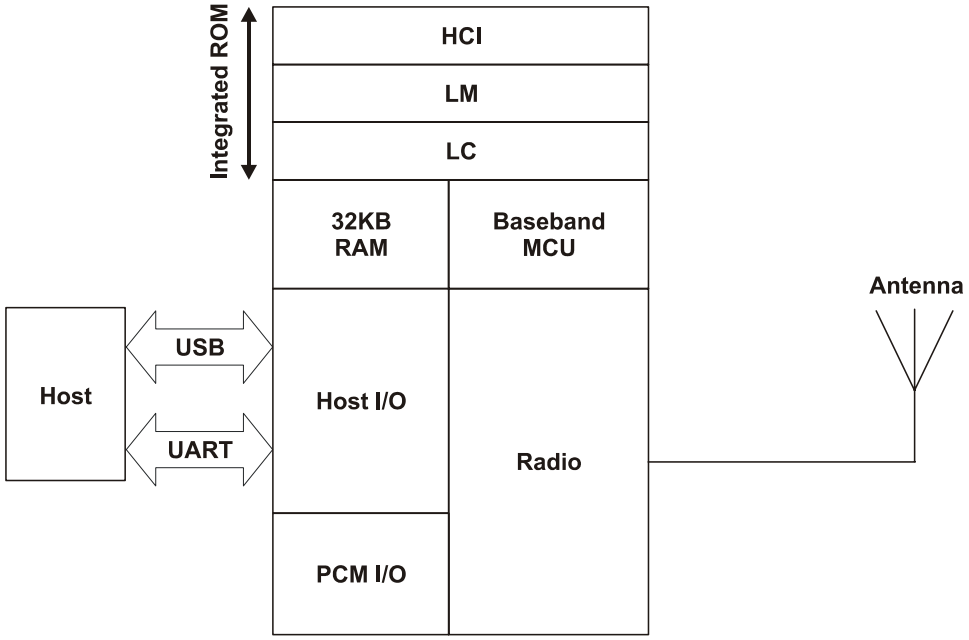


Figure 8.1: BlueCore HCI Stack

In the implementation shown in Figure 8.1, the internal processor runs the Bluetooth stack up to the Host Controller Interface (HCI). All upper layers must be provided by the Host processor.

8.2.1 Key Features of the HCI Stack

Standard Bluetooth Functionality

- The firmware has been written against the Bluetooth Core Specification v1.1 and v1.2
- Bluetooth components: Baseband (including LC), LM and HCI
- Standard USB v1.1 and UART (H4) HCI transport layers
- All standard radio packet types
- Full Bluetooth data rate, up to 723.2kb/s asymmetric (1)
- Operation with up to 7 active slaves (1)
- Maximum number of simultaneous active ACL connections: 7(2)
- Maximum number of simultaneous SCO connections: 3(2)
- Operation with up to 3 SCO links, routed to one or more slaves
- Role switch: can reverse Master/Slave relationship
- All standard SCO voice codings, plus “transparent SCO”
- Standard operating modes: page, inquiry, page-scan and inquiry-scan
- All standard pairing, authentication, link key and encryption operations
- Standard Bluetooth power saving mechanisms: Hold, Sniff and Park modes, including Forced Hold
- Dynamic control of peers’ transmit power via LMP
- Master/Slave switch
- Broadcast
- Channel quality driven data rate
- All standard Bluetooth test modes

The firmware’s supported Bluetooth features are detailed in the standard Protocol Implementation Conformance Statement (PICS) documents, available from www.csrsupport.com.

Notes:

(1) Maximum allowed by Bluetooth specification v1.1 and v1.2

(2) BlueCore2-ROM supports all combinations of active ACL and SCO channels for both Master and Slave operation, as specified by the Bluetooth specification v1.1 and v1.2

Extra Functionality

The firmware extends the standard Bluetooth functionality with the following features:

- Supports BlueCore serial protocol (BCSP), a proprietary, reliable alternative to the standard Bluetooth H4 UART Host Transport
- Provides a set of approximately 50 manufacturer-specific HCI extension commands. This command set, called BCCMD (BlueCore Command), provides:
  - Access to the device's general-purpose PIO port
  - Access to the device's Bluetooth clock (this can help transfer connections to other Bluetooth devices)
  - The negotiated effective encryption key length on established Bluetooth links
  - Access to the firmware's random number generator
  - Controls to set the default and maximum transmit powers e.g. These can help minimise interference between overlapping, fixed-location piconets
  - Dynamic UART configuration
  - Radio transmitter enable/disable e.g. A simple command connects to a dedicated hardware switch that determines whether the radio can transmit
- The firmware can read the voltage on a pair of the chip's external pins e.g. This is normally used to build a battery monitor, using either VM or host code.
- A block of BCCMD commands provides access to the chip's Persistent Store configuration database. The database sets the device's Bluetooth address, Class of device, radio (transmit class) configuration, SCO routing, LM and USB.
- A UART break condition can be used in three ways:
  - Presenting a UART break condition to the chip can force the chip to perform a hardware reboot
  - Presenting a break condition at boot time can hold the chip in a low power state, preventing normal
  - initialisation while the condition exists
  - With BCSP, the firmware can be configured to send a break to the host before sending data normally used to wake the host from a deep sleep state
- A block of radio test or BIST commands allows direct control of the device's radio. This aids the development of modules' radio designs, and can be used to support Bluetooth qualification.
- Virtual Machine (VM). The firmware provides the VM environment in which to run application-specific code. Although the VM is mainly used with BlueLab™ and RFCOMM builds (alternative firmware builds providing L2CAP, SDP and RFCOMM), the VM can be used with this build to perform simple tasks such as flashing LEDs via the chip's PIO port.
- Hardware low power modes:
  - Shallow sleep
  - Deep sleep
- The device drops into modes that significantly reduce power consumption when the software goes idle.
- SCO channels are normally routed over HCI (over BCSP). However, a single SCO channel can be routed over the chip's single PCM port at the same time as routing up to two other SCO channels over HCI. Alternatively up to 3 SCO channels can be mapped to the PCM port.

8.3 BlueCore RFCOMM Stack

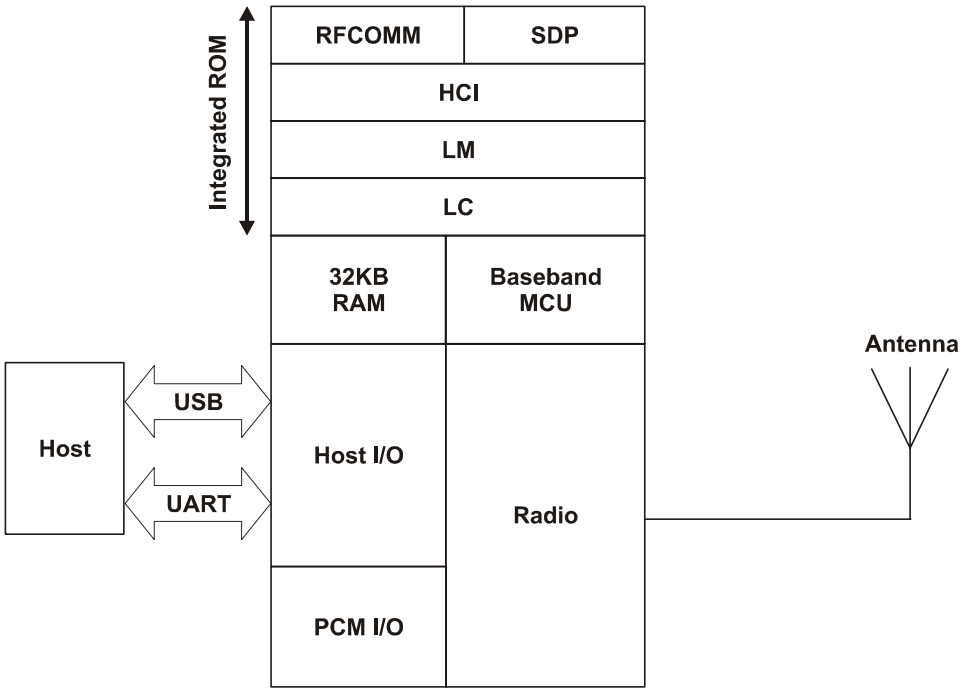


Figure 8.2: BlueCore RFCOMM Stack

In this version of the firmware the upper layers of the Bluetooth stack up to RFCOMM are run on chip. This reduces host side software and hardware requirements at the expense of some of the power and flexibility of the HCI only stack.

8.3.1 Key Features of the BlueCore2-ROM RFCOMM Stack

Interfaces to Host

- RFCOMM, an RS-232 serial cable emulation protocol
- SDP, a service database look-up protocol

Connectivity

- Maximum number of active slaves: 3
- Maximum number of simultaneous active ACL connections: 3
- Maximum number of simultaneous active SCO connections: 3
- Data Rate: up to 350Kb/s

Security

- Full support for all Bluetooth security features up to and including strong 128-bit encryption

Power Saving

- Full support for all Bluetooth power saving modes Park, Sniff and Hold

Data Integrity

- Channel quality driven data rate (CQDDR) increases the effective data rate in noisy environments.
- Receive signal strength indication (RSSI) used to minimise interference to other radio devices using the industrial, scientific and medical (ISM) band

8.4 BlueCore Virtual Machine Stack

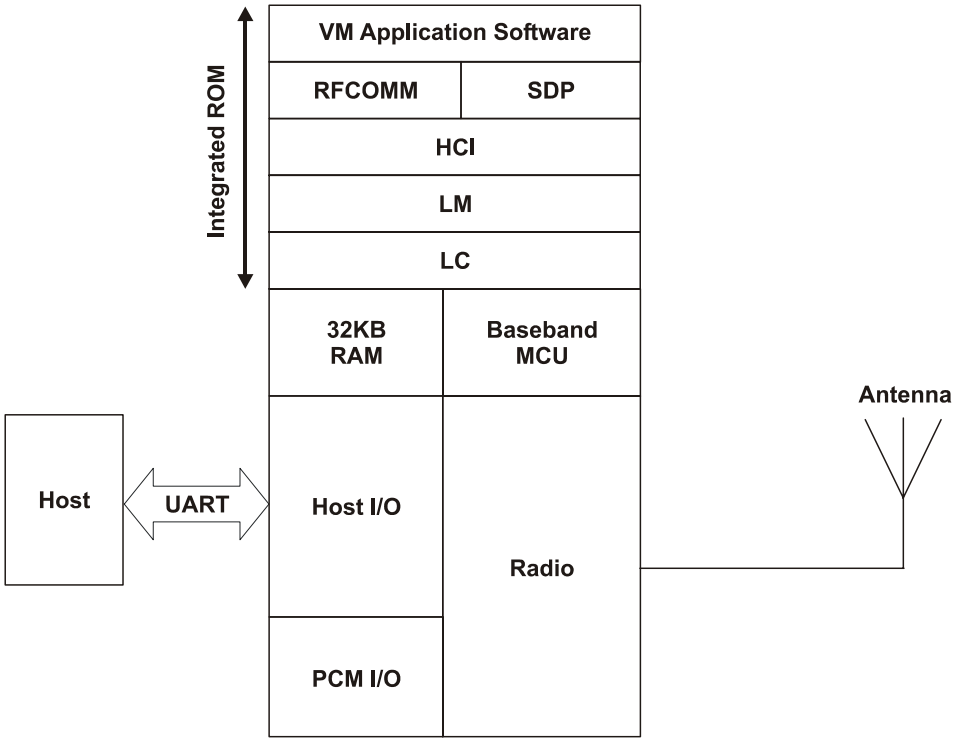


Figure 8.3: Virtual Machine

This version of the stack firmware requires no host processor. All software layers, including application software, run on the internal RISC microcontroller in a protected user software execution environment known as a virtual machine (VM).

The user may write custom application code to run on the BlueCore VM using BlueLab software development kit (SDK) supplied with the BlueLab and Casira™ development kits, available separately from CSR. This code will then execute alongside the main BlueCore firmware. The user is able to make calls to the BlueCore firmware for various operations.

The execution environment is structured so the user application does not adversely affect the main software routines, thus ensuring that the Bluetooth stack software component does not need re-qualification when the application is changed.

Using the VM and the BlueLab SDK the user is able to develop applications such as a cordless headset or other profiles without the requirement of a host controller. BlueLab is supplied with example code including a full implementation of the headset profile.(1)

On successful completion of firmware development and testing using BlueCore2-Flash (BC215159A), CSR can commit the code to a mask set for mass production of the device. A non recurring engineering (NRE) charge will be required.

Notes:

Sample applications to control PIO lines can also be written with BlueLab SDK and the VM for the HCI stack.

(1) BlueLab Professional contains headset

8.5 BlueCore HID Stack

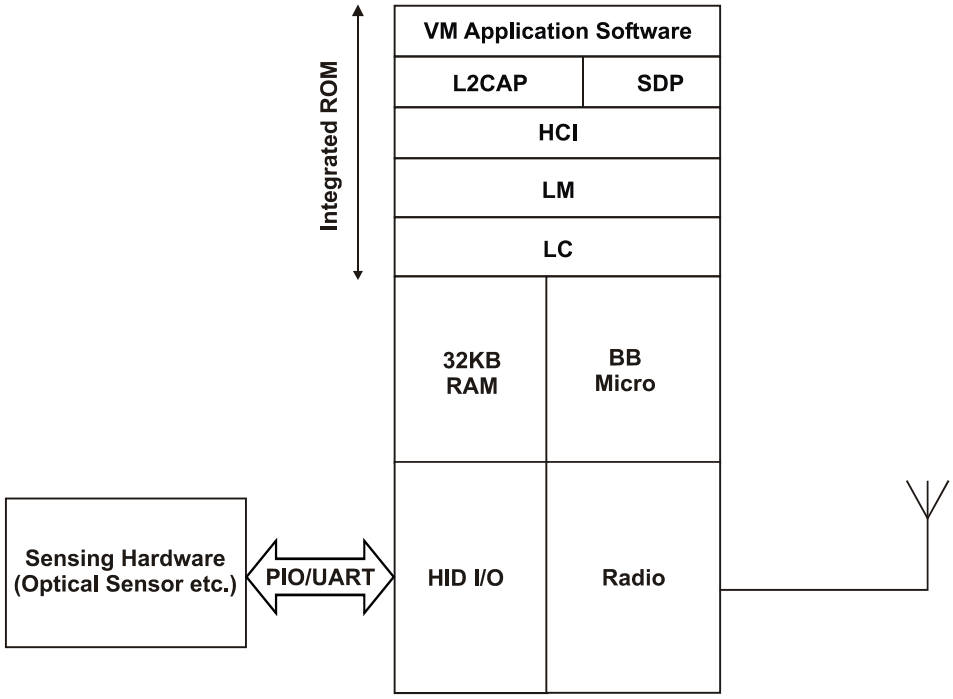


Figure 8.4: HID Stack

This version of the stack firmware requires no host processor. All software layers, including application software, run on the internal RISC microcontroller in a protected user software execution environment known as a virtual machine (VM).

The user may write custom application code to run on the BlueCore VM using BlueLab Professional software development kit (SDK) supplied with the BlueLab Professional and Casira development kits, available separately from CSR. This code will then execute alongside the main BlueCore firmware. The user is able to make calls to the BlueCore firmware for various operations.

The execution environment is structured so the user application does not adversely affect the main software routines, thus ensuring that the Bluetooth stack software component does not need re-qualification when the application is changed.

Using the VM and the BlueLab Professional SDK the user is able to develop Bluetooth HID devices such as an optical mouse or keyboard. The user is able to customise features such as power management and connect/reconnect behaviour.

The HID I/O component in the HID stack controls low latency data acquisition from external sensor hardware. With this component running in native code, it does not incur the overhead of the VM code interpreter. Supported external sensors include 5 mouse buttons, the Agilent ADNS-2030 optical sensor, quadrature scroll wheel, direct coupling to a keyboard matrix and a UART interface to custom hardware.

On successful completion of firmware development and testing using BlueCore2-Flash (BC215159A), CSR can commit the code to a mask set for mass production of the device. A non recurring engineering (NRE) charge will be required.

A reference schematic for implementing a three button, optical mouse with scroll wheel is available from CSR.

8.6 Host Side Software

BlueCore2-ROM can be ordered with companion host side software:

- BlueCore2-PC includes software for a full Windows® 98/ME, Windows 2000 or Windows XP Bluetooth host side stack together with chip hardware described in this document.
- BlueCore2-Mobile includes software for a full host side stack designed for modern ARM based mobile handsets together with chip hardware described in this document.

8.7 Additional Software for Other Embedded Applications

When the upper layers of the Bluetooth protocol stack are run as firmware on BlueCore2-ROM, a UART software driver is supplied that presents the L2CAP, RFCOMM and Service Discovery (SDP) APIs to higher Bluetooth stack layers running on the host. The code is provided as 'C' source or object code.

8.8 CSR Development Systems

CSR's BlueLab and Casira development kits are available to allow the evaluation of the BlueCore2 hardware and software, and as toolkits for developing on chip and host software.

9 Device Terminal Descriptions

9.1 RF Ports

The BlueCore2-ROM RF_IN terminal can be configured as either a single ended or differential input. The operational mode is determined by setting the PS Key PSKEY_TXRX_PIO_CONTROL (0x209). Using a single-ended RF input allows an external PA to be used for Class 1 operation, as shown in Figure 9.2.

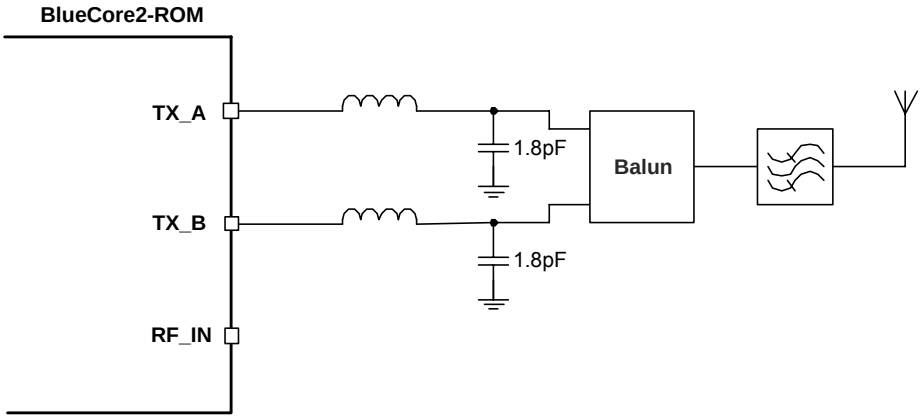


Figure 9.1: Common Differential RF Input and Output Ports (Class 2)

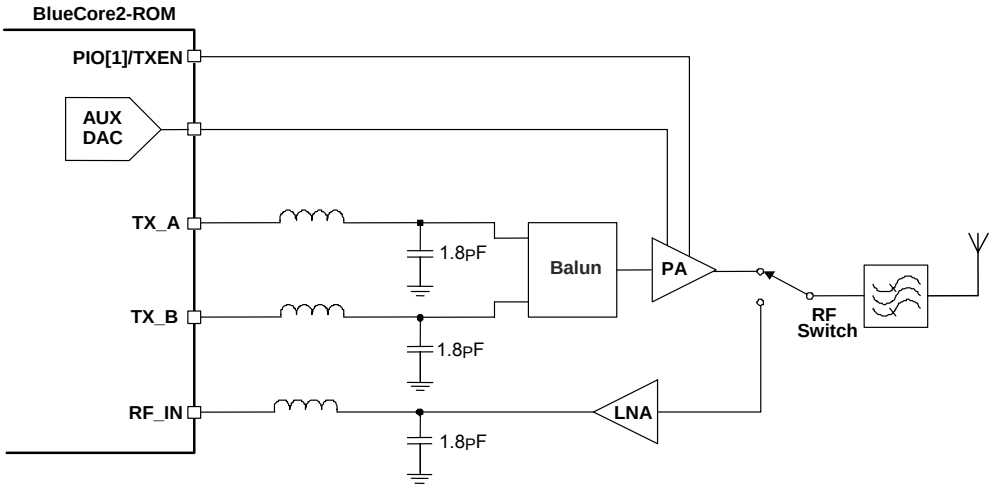


Figure 9.2: Single Ended RF Input (Class 1)

9.1.1 TX_A and TX_B

TX_A and TX_B form a complementary balanced pair. On transmit, their outputs are combined using a balun into the single-ended output required for the antenna. Similarly, on receive, their input signals are combined internally. Both terminals present similar complex impedances that require matching networks between them and the balun. Starting from the substrate (chip side), the outputs can each be modelled as an ideal current source in parallel with a lossy resistance and a capacitor. The bond wire can be represented as series inductance.

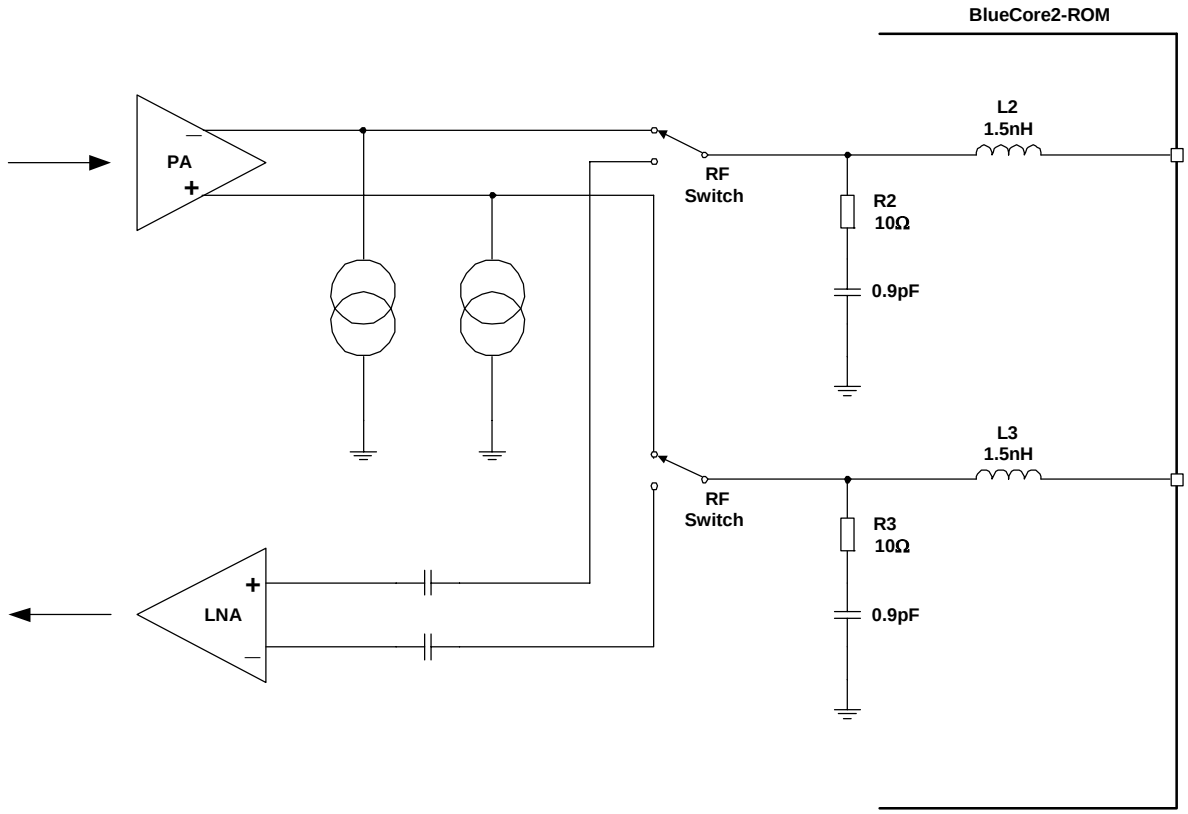


Figure 9.3: Circuit TX/RX_A and TX/RX_B

Transmit Port Impedances for 6 x 6 VFBGA Package (2-3GHz vs. Temperature)

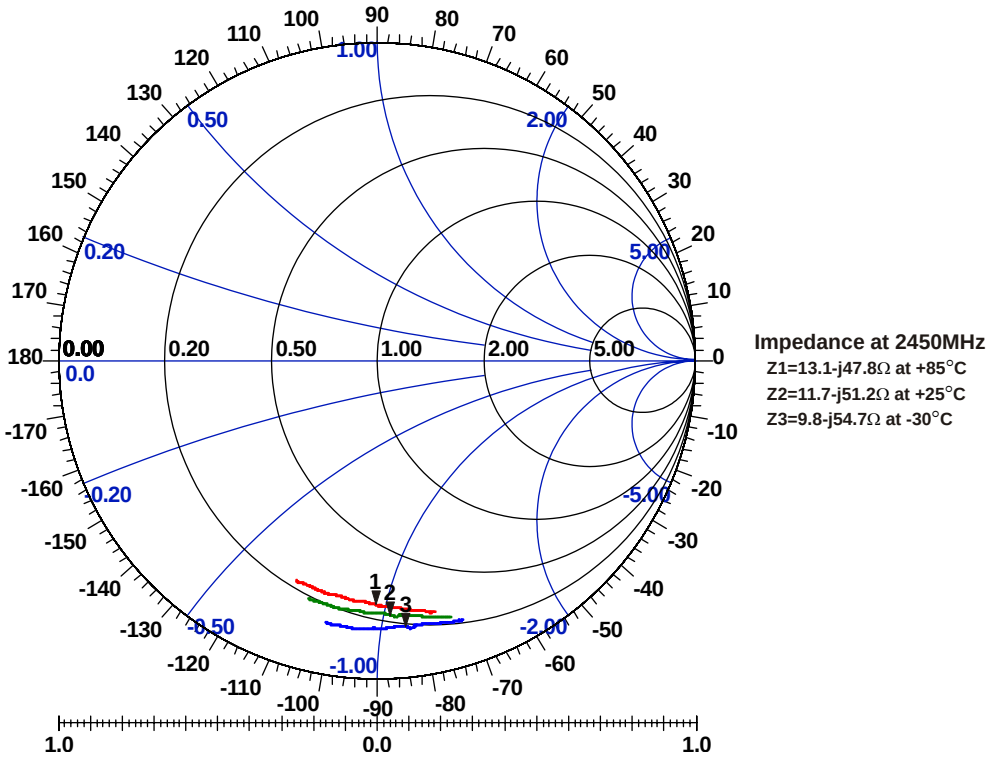


Figure 9.4: TX_A Output at Power Setting 35

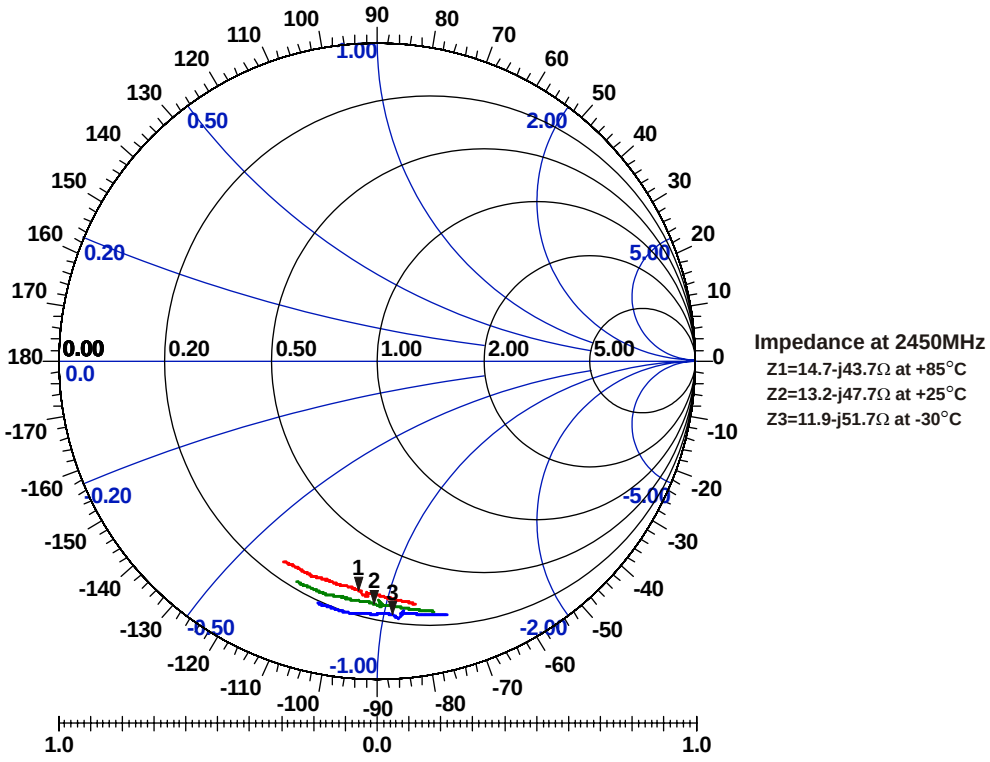


Figure 9.5: TX_A Output at Power Setting 50

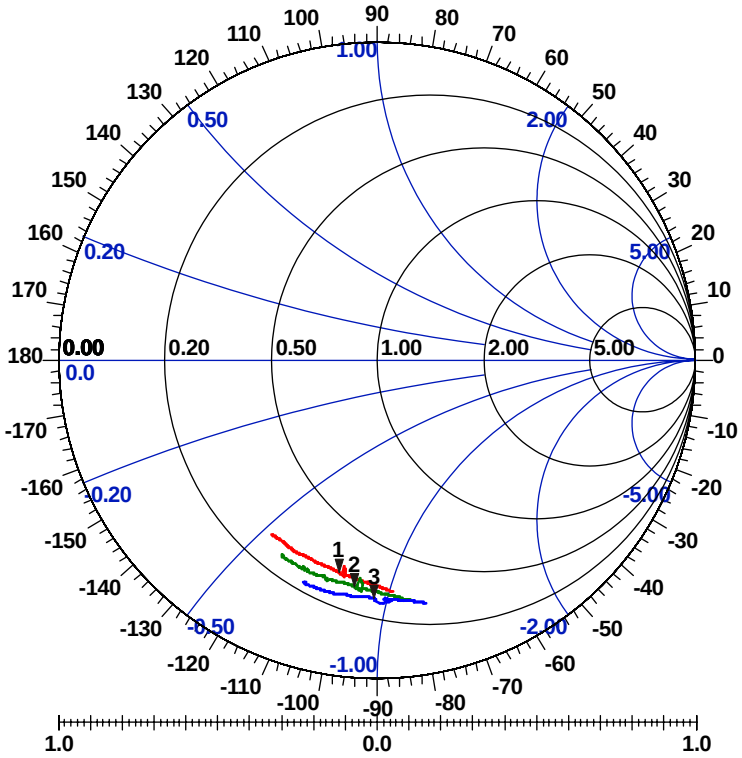


Figure 9.6: TX_A Output at Power Setting 63

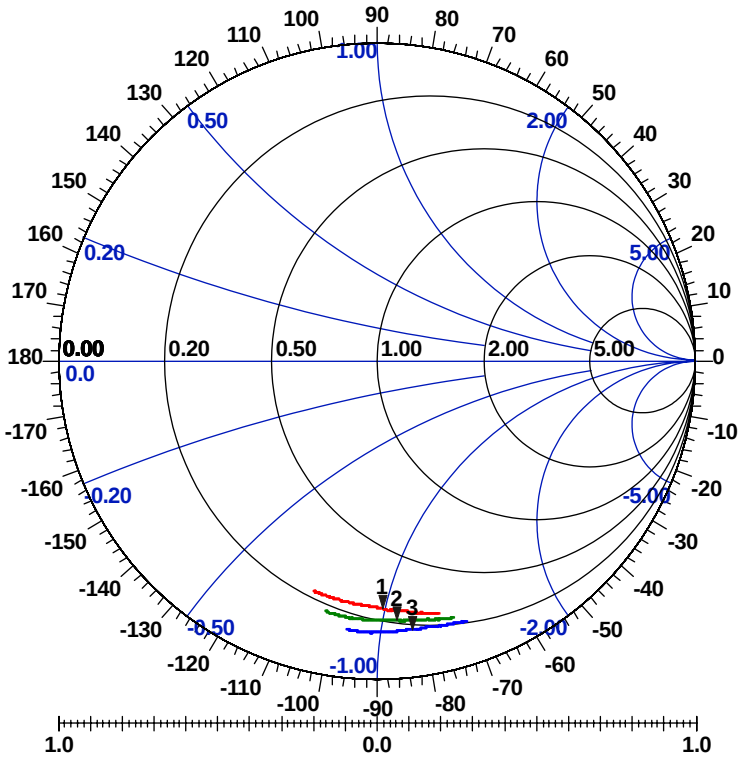


Figure 9.7: TX_B Output at Power Setting 35

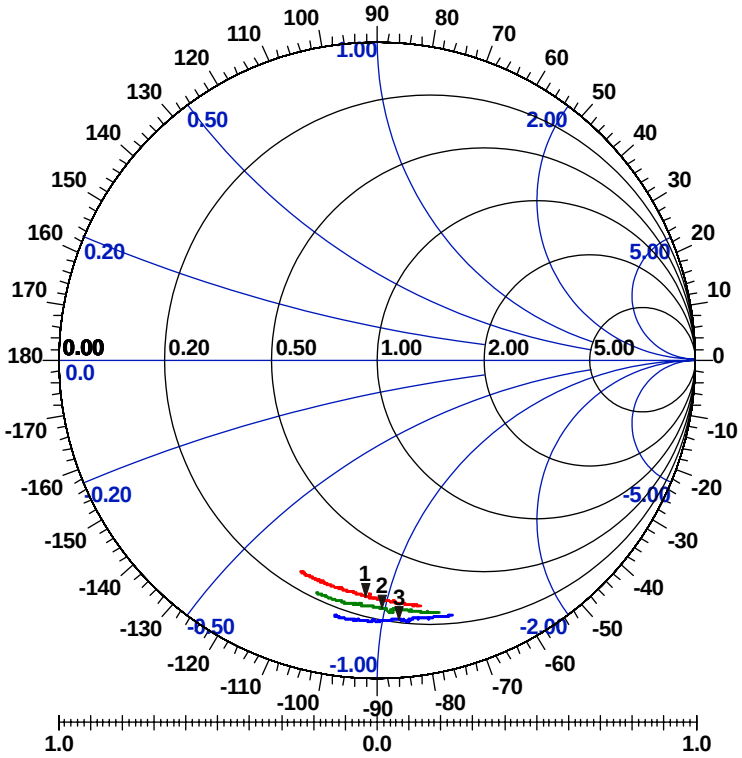


Figure 9.8: TX_B Output at Power Setting 50

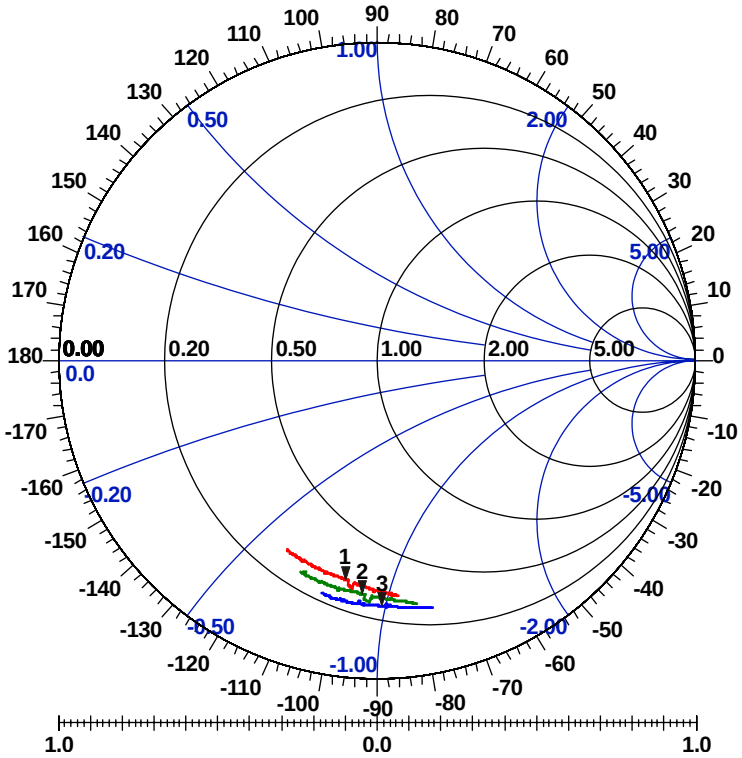


Figure 9.9: TX_B Output at Power Setting 63

Receive Port Impedances for 6 x 6 VFBGA Package (2-3GHz vs. Temperature)

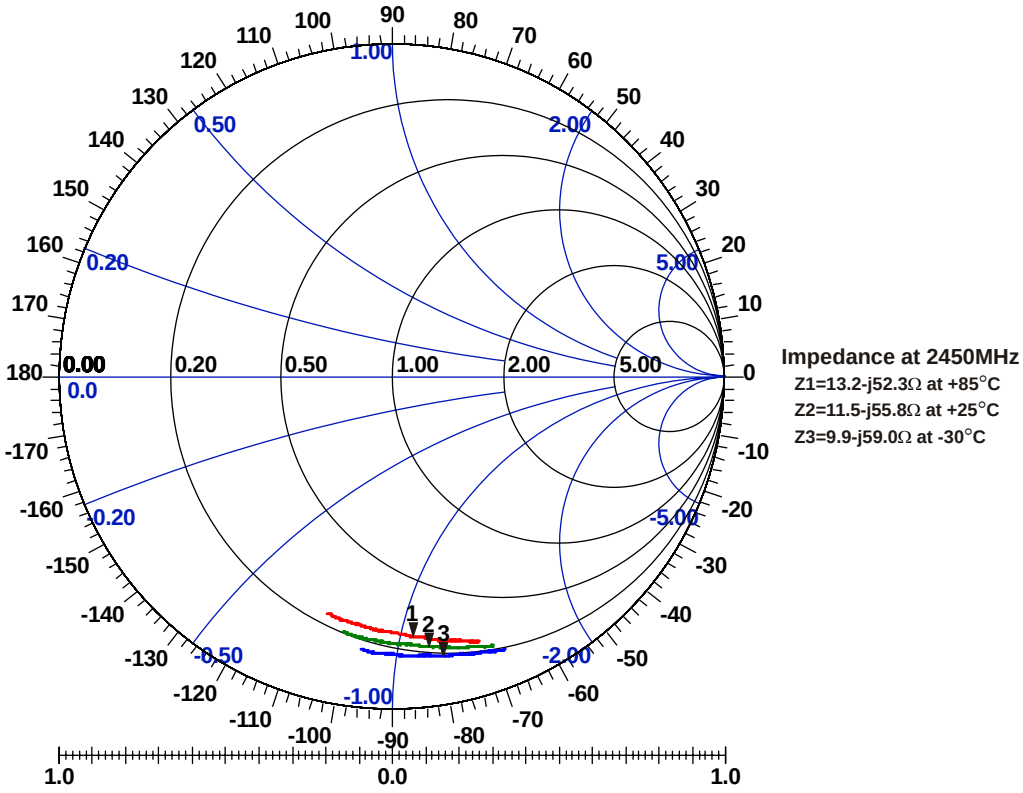


Figure 9.10: TX_A Balanced Receive Input Impedance

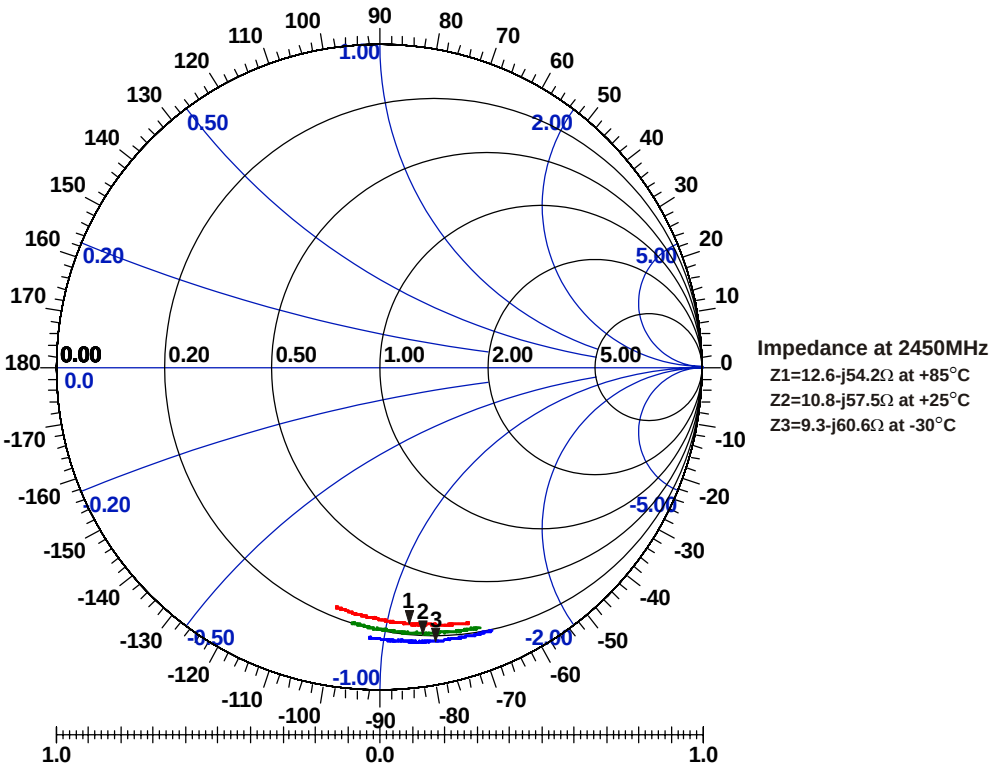


Figure 9.11: TX_B Balanced Receive Input Impedance

Transmit Impedance

Port 1: TX_A

Port 2: TX_B

Temperature: +25°C

Power Level: 50[1]

MHZ S RI R 50

Frequency (MHz)	S11		S21		S12		S22	
	Real	Imaginary	Real	Imaginary	Real	Imaginary	Real	Imaginary
2402	7.45E-03	-7.55E-01	-3.74E-03	4.75E-02	-4.43E-03	5.67E-02	4.23E-02	-7.90E-01
2408	8.61E-03	-7.56E-01	-7.39E-03	5.03E-02	-2.11E-03	5.66E-02	3.82E-02	-7.90E-01
2414	9.70E-03	-7.69E-01	-1.32E-02	6.40E-02	-1.72E-03	4.93E-02	2.98E-02	-7.81E-01
2420	4.76E-03	-7.67E-01	-1.03E-02	6.31E-02	-2.51E-03	4.99E-02	2.88E-02	-7.81E-01
2426	1.01E-03	-7.66E-01	-8.91E-03	6.24E-02	-2.28E-03	4.99E-02	2.60E-02	-7.80E-01
2432	-2.01E-03	-7.65E-01	-8.34E-03	6.19E-02	-2.30E-03	4.97E-02	2.36E-02	-7.79E-01
2438	-4.58E-03	-7.63E-01	-8.05E-03	6.17E-02	-2.43E-03	4.96E-02	2.10E-02	-7.79E-01
2444	-6.99E-03	-7.62E-01	-7.87E-03	6.16E-02	-2.60E-03	4.96E-02	1.91E-02	-7.78E-01
2450	-9.52E-03	-7.61E-01	-7.68E-03	6.16E-02	-2.71E-03	4.96E-02	1.69E-02	-7.78E-01
2456	-1.22E-02	-7.60E-01	-7.47E-03	6.17E-02	-2.86E-03	4.97E-02	1.50E-02	-7.77E-01
2462	-1.51E-02	-7.59E-01	-7.32E-03	6.17E-02	-2.97E-03	4.98E-02	1.29E-02	-7.77E-01
2468	-1.79E-02	-7.59E-01	-7.23E-03	6.18E-02	-3.06E-03	4.98E-02	1.11E-02	-7.77E-01
2474	-2.08E-02	-7.58E-01	-7.19E-03	6.19E-02	-3.12E-03	4.99E-02	9.28E-03	-7.76E-01
2480	-2.33E-02	-7.57E-01	-7.15E-03	6.20E-02	-3.20E-03	5.00E-02	7.45E-03	-7.76E-01

Table 9.1: Transmit Impedance

Notes:

[1] Value assigned to PSKEY_LC_DEFAULT_TX_POWER.

S-Parameter data files available upon request.

Balanced Receive Impedance

Port 1: TX_A

Port 2: TX_B

Temperature: +25°C

Rx in balanced mode

MHZ S RI R 50

Frequency (MHz)	S11		S21		S12		S22	
	Real	Imaginary	Real	Imaginary	Real	Imaginary	Real	Imaginary
2402	1.31E-01	-8.09E-01	2.93E-02	2.99E-02	3.42E-02	2.42E-02	1.51E-01	-8.21E-01
2408	1.29E-01	-8.09E-01	2.92E-02	3.01E-02	3.41E-02	2.41E-02	1.49E-01	-8.21E-01
2414	1.25E-01	-8.08E-01	2.92E-02	3.00E-02	3.40E-02	2.39E-02	1.46E-01	-8.22E-01
2420	1.23E-01	-8.09E-01	2.93E-02	3.00E-02	3.38E-02	2.38E-02	1.46E-01	-8.22E-01
2426	1.20E-01	-8.08E-01	2.90E-02	3.00E-02	3.35E-02	2.37E-02	1.42E-01	-8.22E-01
2432	1.17E-01	-8.09E-01	2.90E-02	3.01E-02	3.32E-02	2.37E-02	1.40E-01	-8.21E-01
2438	1.14E-01	-8.09E-01	2.88E-02	3.03E-02	3.32E-02	2.37E-02	1.36E-01	-8.21E-01
2444	1.12E-01	-8.09E-01	2.91E-02	3.02E-02	3.19E-02	2.34E-02	1.33E-01	-8.20E-01
2450	1.08E-01	-8.09E-01	2.91E-02	3.01E-02	3.16E-02	2.35E-02	1.32E-01	-8.21E-01
2456	1.05E-01	-8.09E-01	2.89E-02	3.02E-02	3.12E-02	2.35E-02	1.29E-01	-8.21E-01
2462	1.04E-01	-8.09E-01	2.87E-02	3.02E-02	3.10E-02	2.33E-02	1.27E-01	-8.20E-01
2468	1.02E-01	-8.08E-01	2.85E-02	3.01E-02	3.08E-02	2.33E-02	1.25E-01	-8.21E-01
2474	9.81E-02	-8.08E-01	2.82E-02	3.01E-02	3.07E-02	2.31E-02	1.23E-01	-8.20E-01
2480	9.67E-02	-8.08E-01	2.80E-02	3.00E-02	3.05E-02	2.29E-02	1.20E-01	-8.20E-01

Table 9.2: Balanced Receiver Impedance

Note:

S-Parameter data files available upon request.

9.1.2 Single-Ended Input (RF_IN)

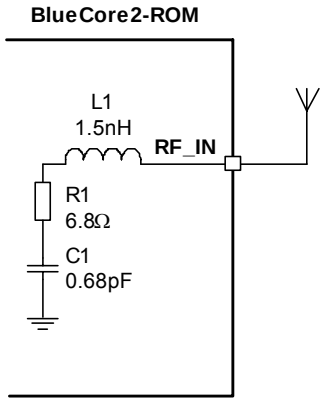


Figure 9.12: Circuit RF_IN

This is the single ended RF input from the antenna. The input presents a complex impedance that requires a matching network between the terminal and the antenna. Starting from the substrate (chip) side, the input can be modelled as a lossy capacitor with the bond wire to the ball grid represented as a series inductance.

The terminal is DC blocked. The DC level must not exceed (VSS_RADIO -0.3V to VDD_RADIO + 0.3V).

Note:

Both terminals must be externally DC biased to VDD_RADIO.

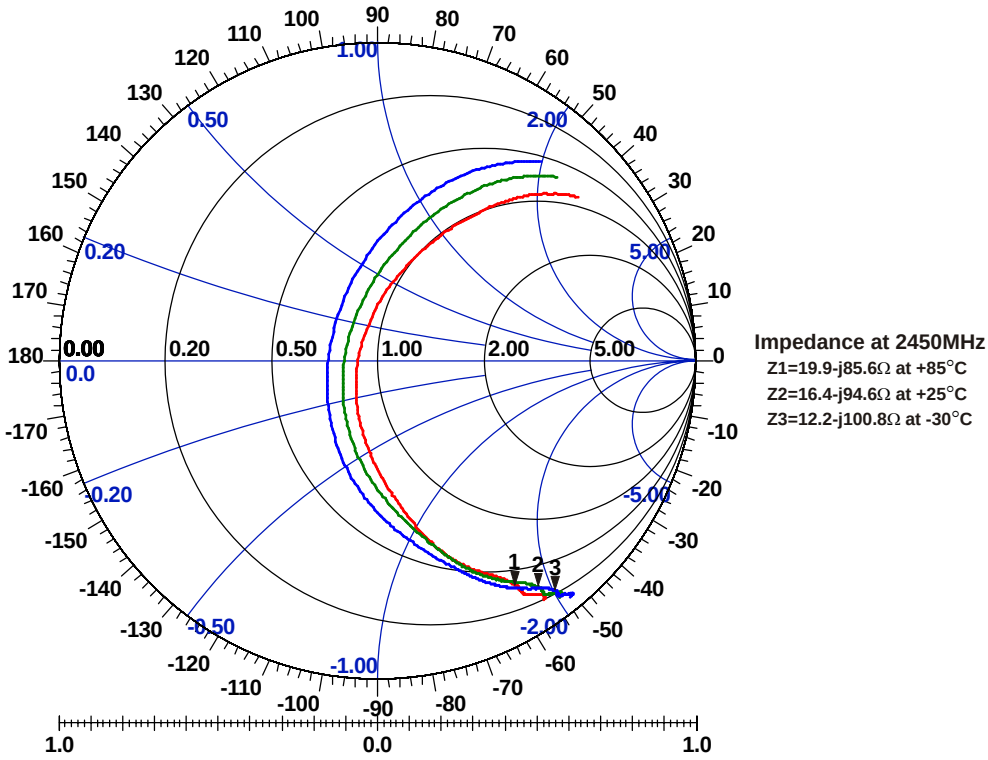


Figure 9.13: RX_SINGLE_ENDED Receive Input Impedance

Single-Ended Receive Impedance

Port 1: RF_IN

Temperature: +25°C

Rx in unbalanced mode

MHZ S RI R 50

Frequency (MHz)	S11	
	Real	Imaginary
2402	5.18E-01	-7.25E-01
2408	5.18E-01	-7.23E-01
2414	5.15E-01	-7.21E-01
2420	5.16E-01	-7.18E-01
2426	5.14E-01	-7.17E-01
2432	5.14E-01	-7.15E-01
2438	5.11E-01	-7.12E-01
2444	5.07E-01	-7.11E-01
2450	5.03E-01	-7.09E-01
2456	4.99E-01	-7.08E-01
2462	4.95E-01	-7.06E-01
2468	4.90E-01	-7.03E-01
2474	4.85E-01	-7.03E-01
2480	4.80E-01	-7.01E-01

Table 9.3: Single-Ended Impedance

Note:

S-Parameter data files available upon request.

9.1.3 Transmit RF Power Control for Class 1 Applications (TX_PWR)

An 8-bit voltage DAC (AUX_DAC) is used to control the amplification level of the external PA for Class 1 operation. The DAC output is derived from the on chip band gap and is virtually independent of temperature and supply voltage. The output voltage is given by:

$$V_{DAC} = MIN\left(\left(3.3v \times \frac{CNTRL\_WORD}{255}\right), (VDD\_PIO - 0.3v)\right)$$

for a load current ≤10mA (sourced from the device).

or

$$V_{DAC} = MIN\left(\left(3.3v \times \frac{CNTRL\_WORD}{255}\right), VDD\_PIO\right)$$

for no load current.

BlueCore2-ROM enables the external PA only when transmitting. Before transmitting, the chip normally ramps up the power to the internal PA, then it ramps it down again afterwards. However, if a suitable external PA is used, it may be possible to ramp the power externally by driving the TX_PWR pin on the PA from AUX_DAC.

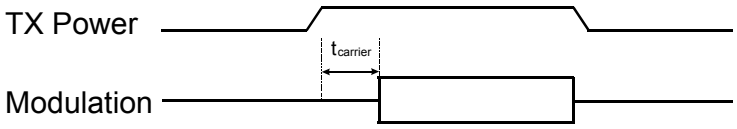


Figure 9.14: Internal Power Ramping

The persistent store key (PS Key) PSKEY_TX_GAINRAMP (0x1d), is used to control the delay (in units of μs) between the end of the transmit power ramp and the start of modulation. In this period the carrier is transmitted, which gives the transmit circuitry time to fully settle to the correct frequency.

Bits [15:8] define a delay, $t_{carrier}$, (in units of μs) between the end of the transmit power ramp and the start of modulation. In this period carrier is transmitted, which aids interoperability with some other vendor equipment which is not strictly Bluetooth compliant.

9.2 Control of External RF Components

A PS Key TXRX_PIO_CONTROL (0x209) is used to control external RF components such as a switch, an external PA or an external LNA. PIO[0], PIO[1] and the AUX_DAC can be used for this purpose, as indicated in Table 9.4: TXRX_PIO_CONTROL Values

.

TXRX_PIO_CONTROL Value	AUX_DAC Use
0	PIO[0], PIO[1], AUX_DAC not used to control RF. Power ramping is internal.
1	PIO[0] is high during RX, PIO[1] is high during TX. AUX_DAC not used. Power ramping is internal.
2	PIO[0] is high during RX, PIO[1] is high during TX. AUX_DAC used to set gain of external PA. Power ramping is external.
3	PIO[0] is low during RX, PIO[1] is low during TX. AUX_DAC used to set gain of external PA. Power ramping is external.
4	PIO[0] is high during RX, PIO[1] is high during TX. AUX_DAC used to set gain of external PA. Power ramping is internal.

Table 9.4: TXRX_PIO_CONTROL Values

9.3 External Reference Clock Input (XTAL_IN)

9.3.1 Introduction

The BlueCore2-ROM RF local oscillator and internal digital clocks are derived from the reference clock at the BlueCore2-ROM XTAL_IN input. This reference may be either an external clock or from a crystal connected between XTAL_IN and XTAL_OUT. The crystal mode is described in Section 9.4.

9.3.2 External Mode

BlueCore2-ROM can be configured to accept an external reference clock (from another device, such as TCXO) at XTAL_IN by connecting XTAL_OUT to ground. The external clock can either be a digital level square wave or sinusoidal and this may be directly coupled to XTAL_IN without the need for additional components. If the peaks of the reference clock are below VSS_ANA or above VDD_ANA, it must be driven through a DC blocking capacitor (~33pF) connected to XTAL_IN. A digital level reference clock gives superior noise immunity as the high slew rate clock edges have lower voltage to phase conversion.

The external clock signal should meet the specifications in Table 9.5:

	Min	Typ	Max
Frequency[1]	8MHz	16MHz	40MHz
Duty cycle	20:80	50:50	80:20
Edge Jitter (At Zero Crossing)	-	-	15ps rms
Signal Level	400mV pk-pk	-	VDD_ANA[2]

Table 9.5: External Clock Specifications

Notes:

[1] The frequency should be an integer multiple of 250kHz except for the CDMA/3G frequencies

[2] VDD_ANA is 1.8V nominal

9.3.3 XTAL_IN Impedance in External Mode

The impedance of the XTAL_IN will not change significantly between operating modes, typically 10fF. When transitioning from deep sleep to an active state a spike of up to 1pC may be measured. For this reason it is recommended that a buffered clock input be used.

9.3.4 Clock Timing Accuracy

As Figure 9.15 indicates, the 250ppm timing accuracy on the external clock is required 7ms after the assertion of the system clock request line. This is to guarantee that the firmware can maintain timing accuracy in accordance with the Bluetooth specification v1.1 and v1.2. Radio activity may occur after 11ms, therefore at this point, the timing accuracy of the external clock source must be within 20ppm.

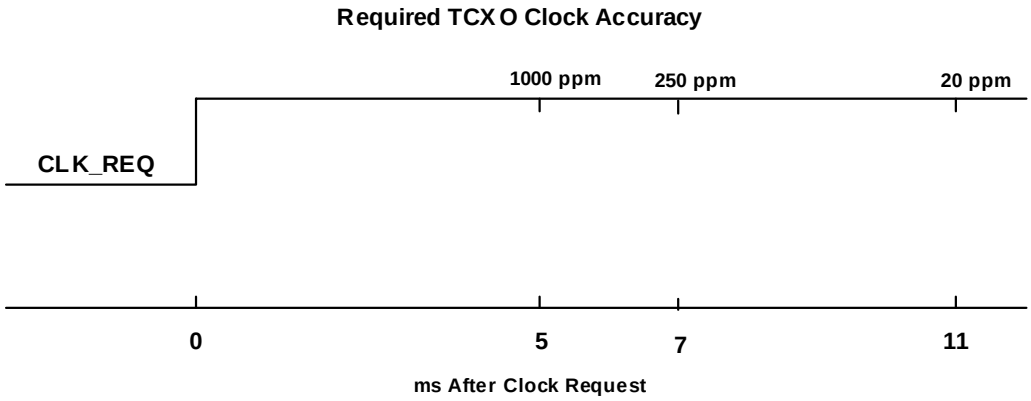


Figure 9.15: TCXO Clock Accuracy

9.3.5 Clock Start-up Delay

BlueCore2-ROM hardware incorporates an automatic 5ms delay after the assertion of the system clock request signal before running firmware. This is suitable for most applications using an external clock source. However, there may be scenarios where the clock cannot be guaranteed to either exist or be stable after this period. Under these conditions, BlueCore2-ROM firmware provides a software function which will extend the system clock request signal by a period stored in PSKEY_CLOCK_STARTUP_DELAY. This value is set in milliseconds from 5-31ms.

This PS Key allows the designer to optimise a system where clock latencies may be longer than 5ms while still keeping the current consumption of BlueCore2-ROM as low as possible. BlueCore2-ROM will consume about 2mA of current for the duration of PSKEY_CLOCK_STARTUP_DELAY before activating the firmware.

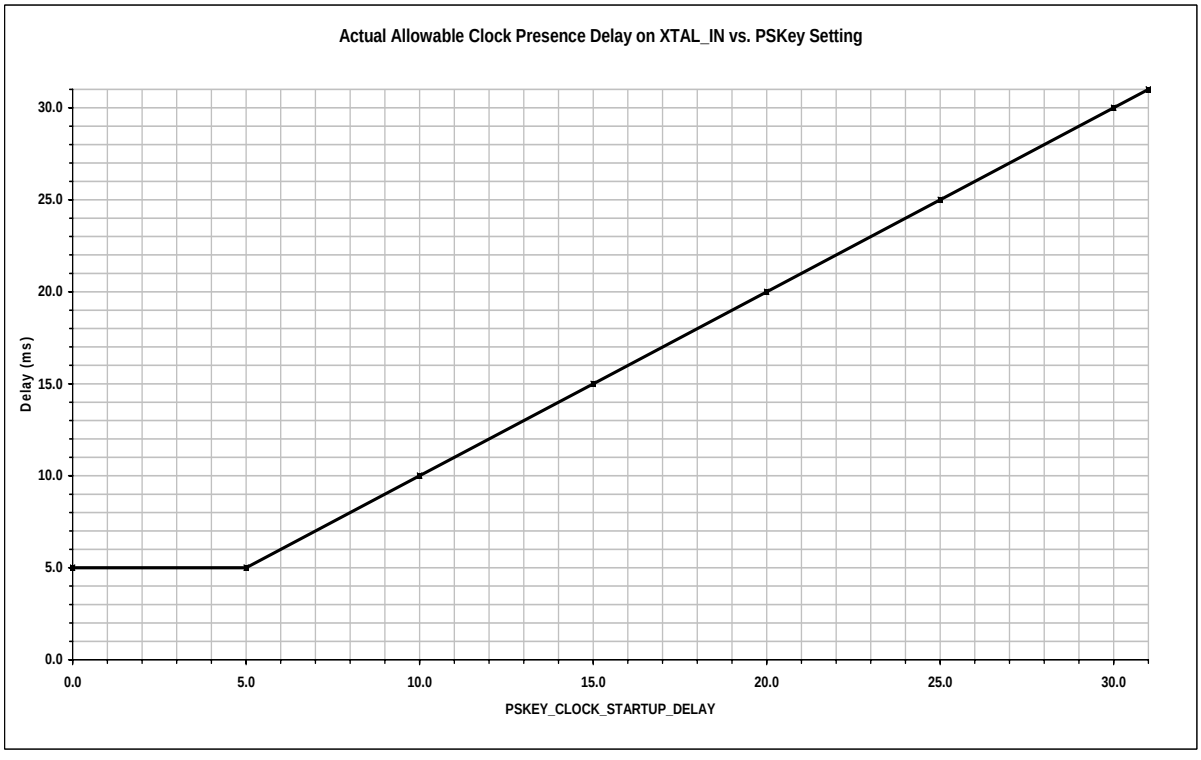


Figure 9.16: Actual Allowable Clock Presence Delay on XTAL_IN vs. PS Key setting

9.3.6 Input Frequencies and PS Key Settings

BlueCore2-ROM should be configured to operate with the chosen reference frequency. This is accomplished by setting the PS Key PSKEY_ANA_FREQ (0x1fe) for all frequencies with an integer multiple of 250KHz. The input frequency default setting in BlueCore2-ROM is 26MHz.

The following CDMA/3G TCXO frequencies are also catered for: 7.68, 14.4, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz. This is accomplished by also changing PSKEY PLLX_FREQ_REF (0xabc).

Reference Crystal Frequency MHz	PSKEY_ANA_FREQ (0x1fe) Hex	PLLX_FREQ_REF (0xabc) Hex
7.68	49	05
14.40	12	05
15.36	04	05
16.20	5c	0c
16.80	3c	05
19.20	1e	05
19.44	5c	05
19.68	59	05
19.80	02	0c
38.40	9e	05
n x 250KHz	-	0e

Table 9.6: PS Key Values for CDMA/3G phone TCXO Frequencies

Table 9.7 shows PS Key values for PS KEY_ANA_FREQ (0x1fe), as a function of reference or crystal frequency:

Reference or Crystal Frequency (MHz)	PS Key Value (Hex)
8.00	49
8.25	72
8.50	05
8.75	6b
9.00	36
9.25	0c
9.50	78
9.75	11
10.00	43
10.25	66
10.50	2d
10.75	3b
11.00	17
11.25	4f
11.50	7e
11.75	1d
12.00	5b
12.25	56
12.50	4d
12.75	7a
13.00	15
13.25	4b
13.50	76
13.75	0d
14.00	7b
14.25	16
14.50	4c
14.75	79
15.00	12
15.25	44
15.50	69
15.75	32
16.00	04
16.25	68
16.50	31
16.75	03
17.00	67
17.25	2e
17.50	3c
17.75	18
18.00	50
18.25	41
18.50	62
18.75	25

Reference or Crystal Frequency (MHz)	PS Key Value (Hex)
20.00	1e
20.25	5c
20.50	59
20.75	52
21.00	45
21.25	6a
21.50	35
21.75	0b
22.00	77
22.25	0e
22.50	7c
22.75	19
23.00	53
23.25	46
23.50	6d
23.75	3a
24.00	14
24.25	48
24.50	71
24.75	02
25.00	64
25.25	29
25.50	33
25.75	07
26.00	6f
26.25	3e
26.50	1c
26.75	58
27.00	51
27.25	42
27.50	65
27.75	2a
28.00	34
28.25	08
28.50	70
28.75	01
29.00	63
29.25	26
29.50	2c
29.75	38
30.00	10
30.25	40
30.50	61
30.75	22

19.00	2b
19.25	37
19.50	0f
19.75	7f

31.00	24
31.25	28
31.50	30
31.75	00
32.00	60

Table 9.7: Reference or Crystal Frequency Persistent Store Key Values

9.4 Crystal Oscillator (XTAL_IN, XTAL_OUT)

9.4.1 Introduction

The BlueCore2-ROM RF local oscillator and internal digital clocks are derived from the reference clock at the BlueCore2-ROM XTAL_IN input. This reference may be either an external clock or from a crystal connected between XTAL_IN and XTAL_OUT. The external reference clock mode is described in Section 9.3.

9.4.2 XTAL Mode

BlueCore2-ROM contains a crystal driver circuit. This operates with an external crystal and capacitors to form a Pierce oscillator.

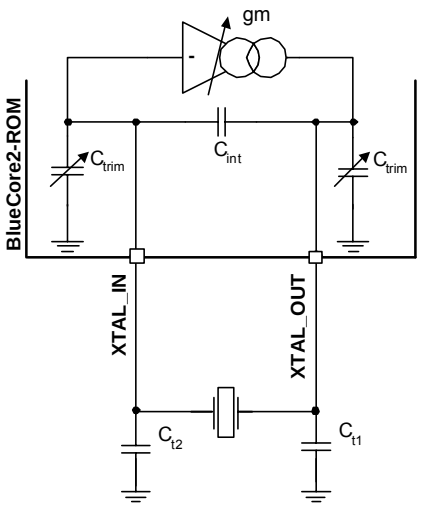


Figure 9.17: BlueCore2-ROM Crystal Driver Circuit

Figure 9.18 shows an electrical equivalent circuit for a crystal. The crystal appears inductive near its resonant frequency. It forms a resonant circuit with its load capacitors.

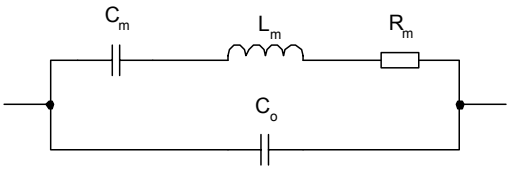


Figure 9.18: Crystal Equivalent Circuit

The resonant frequency may be trimmed with the crystal load capacitance. BlueCore2-ROM contains variable internal capacitors to provide a fine trim.

The BlueCore2-ROM driver circuit is a transconductance amplifier. A voltage at XTAL_IN generates a current at XTAL_OUT. The value of transconductance is variable and may be set for optimum performance.

9.4.3 Load Capacitance

For resonance at the correct frequency the crystal should be loaded with its specified load capacitance, which is defined for the crystal. This is the total capacitance across the crystal viewed from its terminals. BlueCore2-ROM provides some of this load with the capacitors C_{trim} and C_{int}. The remainder should be from the external capacitors labelled C_{t1} and C_{t2}. C_{t1} should be three times the value of C_{t2} for best noise performance. This maximises the signal swing, hence slew rate at XTAL_IN, to which all on chip clocks are referred. Crystal load capacitance, C_l is calculated with the following equation:

$$C_l = C_{int} + \frac{C_{trim}}{2} + \frac{C_{t1}.C_{t2}}{C_{t1} + C_{t2}}$$

Where:

C_{trim} = 3.4pF nominal (Mid range setting)

C_{int} = 1.5pF

Note:

(C_{int}) does not include the crystal internal self capacitance, it is the driver self capacitance.

9.4.4 Frequency Trim

BlueCore2-ROM enables frequency adjustments to be made. This feature is typically used to remove initial tolerance frequency errors associated with the crystal. Frequency trim is achieved by adjusting the crystal load capacitance with on chip trim capacitors, C_{trim}. The value of C_{trim} is set by a 6-bit word in the Persistent Store Key PSKEY_ANA_FTRIM (0x1f6). Its value is calculated thus:

C_{trim} = 110 fF × PSKEY_ANA_FTRIM

There are two C_{trim} capacitors, which are both connected to ground. When viewed from the crystal terminals, they appear in series so each least significant bit (LSB) increment of frequency trim presents a load across the crystal of 55fF.

The frequency trim is described by the following equation:

$\Delta(Fx) / Fx$ = pullability × $55x10^{-3}$ (ppm/LSB)

Where F_x is the crystal frequency and pullability is a crystal parameter with units of ppm/pF. Total trim range is 63 times the value above.

If not specified, the pullability of a crystal may be calculated from its motional capacitance with the following equation:

$$\frac{\partial(F_x)}{\partial(C)} = F_x . \frac{C_m}{4(C_l + C_0)^2}$$

Where:

C_0 = Crystal self capacitance (shunt capacitance)

C_m = Crystal motional capacitance (series branch capacitance in crystal model). See figure 9.18.

Note:

It is a Bluetooth requirement that the frequency is always within ±20ppm. The trim range should be sufficient to pull the crystal within ±5ppm of the exact frequency. This leaves a margin of ±15ppm for frequency drift with ageing and temperature. A crystal with an ageing and temperature drift specification of better than ±15ppm is required.

9.4.5 Transconductance Driver Model

The crystal and its load capacitors should be viewed as a transimpedance element, whereby a current applied to one terminal generates a voltage at the other. The transconductance amplifier in BlueCore2-ROM uses the voltage at its input, XTAL_IN, to generate a current at its output, XTAL_OUT. Therefore, the circuit will oscillate if the transconductance, transimpedance product is greater than unity. For sufficient oscillation amplitude, the product should be greater than 3. The transconductance required for oscillation is defined by the following relationship:

$$gm > \frac{3(C_{t1}+C_{trim})(C_{t2}+C_{trim})}{(2\pi F_x)^2 R_m((C_o+C_{\text{int}})(C_{t1}+C_{t2}+2C_{trim})+(C_{t1}+C_{trim})(C_{t2}+C_{trim}))^2}$$

BlueCore2-ROM guarantees a transconductance value of at least 2mA/V at maximum drive level.

Notes:

More drive strength is required for higher frequency crystals, higher loss crystals (larger R_m) or higher capacitance loading.

Optimum drive level is attained when the level at XTAL_IN is approximately 1V pk–pk. The drive level is determined by the crystal driver transconductance, by setting the Persistent Store KEY_XTAL_LVL (0x241).

9.4.6 Negative Resistance Model

An alternative representation of the crystal and its load capacitors is a frequency dependent resistive element. The driver amplifier may be considered as a circuit that provides negative resistance. For oscillation, the value of the negative resistance must be greater than that of the crystal circuit equivalent resistance. Although the BlueCore2-ROM crystal driver circuit is based on a transimpedance amplifier, an equivalent negative resistance may be calculated for it with the following formula:

$$Rneg = \frac{3(C_{t1}+C_{trim})(C_{t2}+C_{trim})}{g_m(2\pi F_x)^2(C_0+C_{\text{int}})((C_{t1}+C_{t2}+2C_{trim})+(C_{t1}+C_{trim})(C_{t2}+C_{trim}))^2}$$

This formula shows the negative resistance of the BlueCore2-ROM driver as a function of its drive level setting.

The value of the driver negative resistance may be easily measured by placing an additional resistance in series with the crystal. The maximum value of this resistor (oscillation occurs) is the equivalent negative resistance of the oscillator.

	Min	Typ	Max
Frequency	8MHz	16MHz	32MHz
Initial Tolerance	-	±25ppm	-
Pullability	-	±20ppm/pF	-

Table 9.8: Oscillator Negative Resistance

9.4.7 Crystal PS Key Settings

See tables in Section 9.3.6.

9.4.8 Crystal Oscillator Characteristics

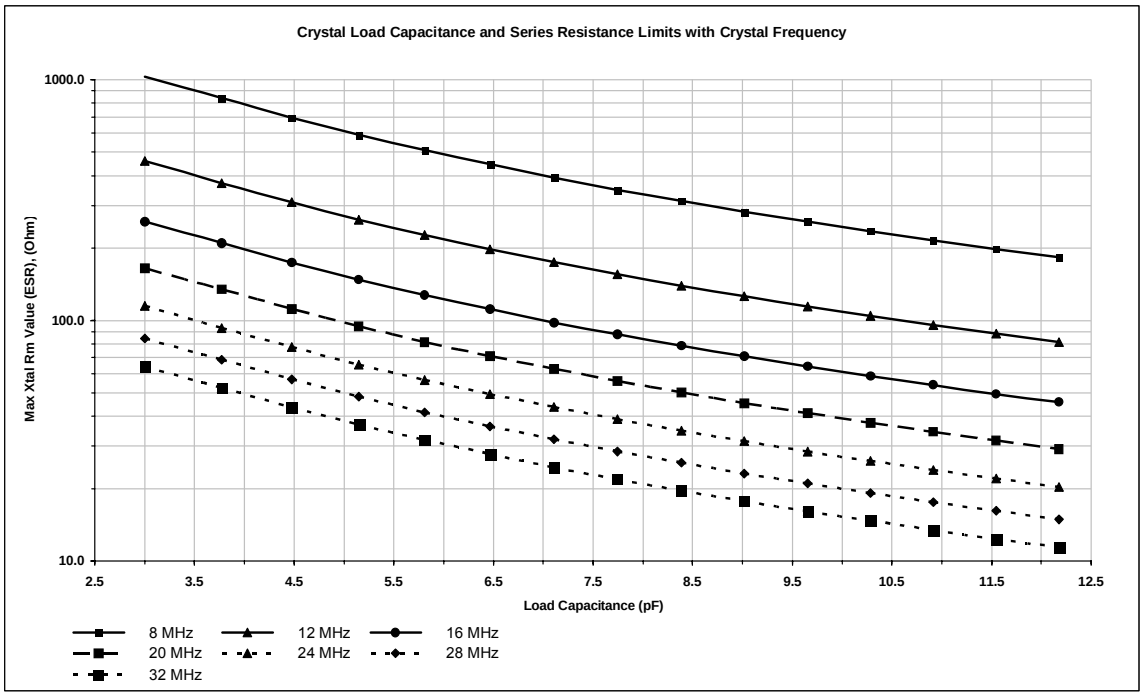


Figure 9.19: Crystal Load Capacitance and Series Resistance Limits with Crystal Frequency

Note:

Graph shows results for BlueCore2-ROM crystal driver at maximum drive level.

Conditions:

C_{trim} = 3.4pF centre value

Crystal C_o = 2pF

Transconductance setting = 2mA/V

Loop gain = 3

C_{t1}/C_{t2} = 3

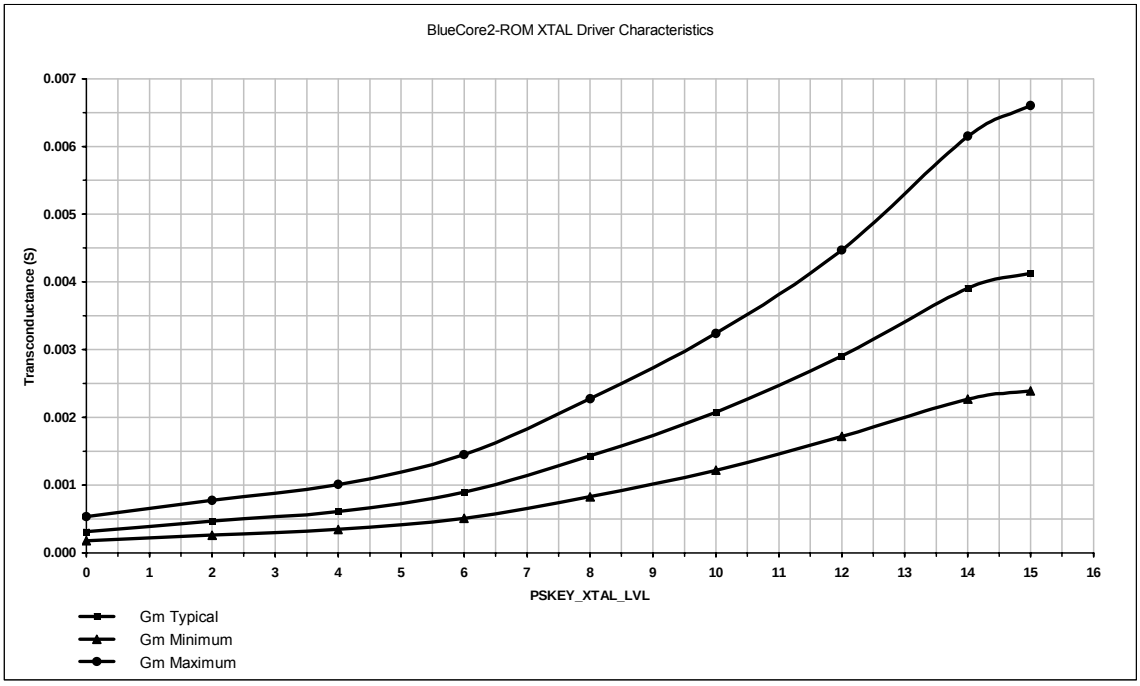


Figure 9.20: Crystal Driver Transconductance vs. Driver Level Register Setting

Note:

Drive level is set by Persistent Store Key PSKEY_XTAL_LVL (0x241).

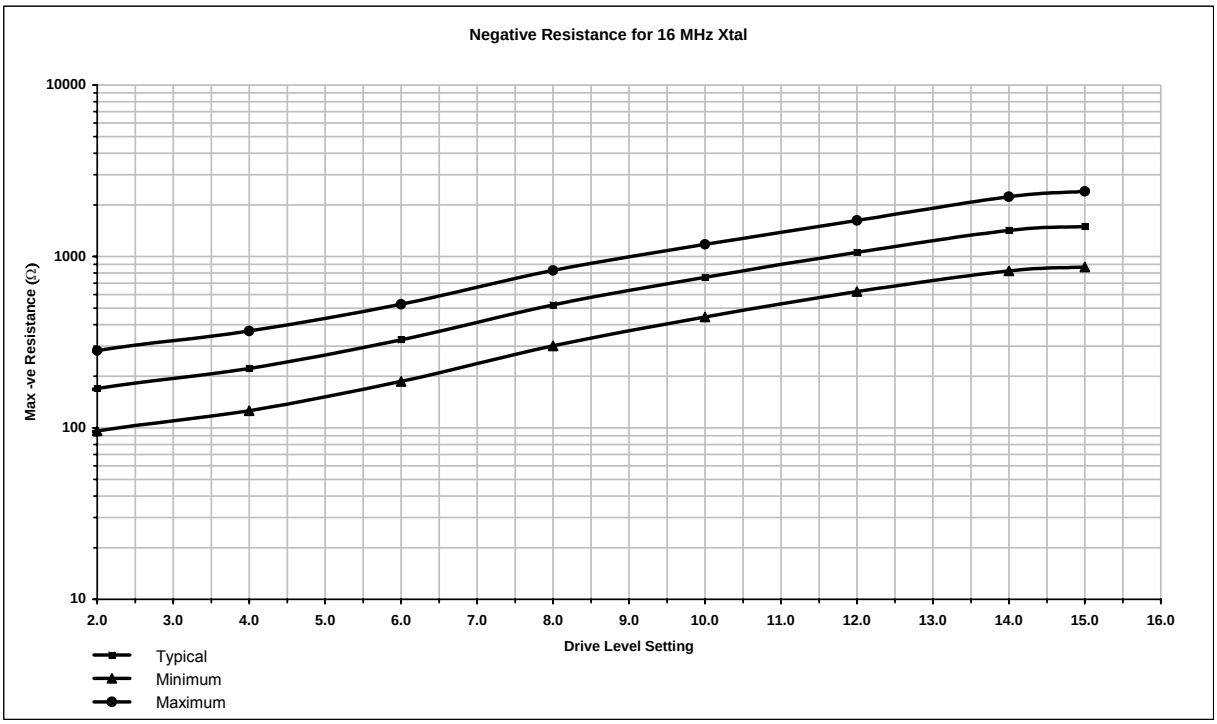


Figure 9.21: Crystal Driver Negative Resistance as a Function of Drive Level Setting

Crystal parameters:

Crystal frequency 16MHz (Please refer to your software build release note for frequencies supported);

Crystal C_0 = 0.75pF

Circuit parameters:

C_{trim} = 8pF, maximum value

C_{t1},C_{t2} = 5pF (3.9pF plus 1.1 pF stray)

(Crystal total load capacitance 8.5pF)

Note:

This is for a specific crystal and load capacitance.

9.5 UART Interface

BlueCore2-ROM Universal Asynchronous Receiver Transmitter (UART) interface provides a simple mechanism for communicating with other serial devices using the RS232 standard [(1)].

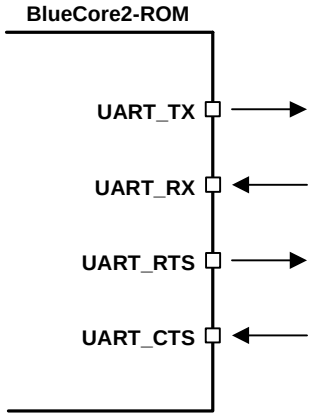


Figure 9.22: Universal Asynchronous Receiver

Four signals are used to implement the UART function, as shown in Figure 9.22. When BlueCore2-ROM is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators. All UART connections are implemented using CMOS technology and have signalling levels of 0V and VDD_PADS.

UART configuration parameters, such as baud rate and packet format, are set using BlueCore2-ROM software.

Notes:

In order to communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

(1) Uses RS232 protocol but voltage levels are 0V to VDD_USB, (requires external RS232 transceiver chip)

Parameter		**Possible Values**
Baud Rate	Minimum	1200 baud (≤2%Error) 9600 baud (≤1%Error)
	Maximum	1.5M baud (≤1%Error)
Flow Control		RTS/CTS or None
Parity		None, Odd or Even
Number of Stop Bits		1 or 2
Bits per channel		8

Table 9.9: Possible UART Settings

The UART interface is capable of resetting BlueCore2-ROM upon reception of a break signal. A Break is identified by a continuous logic low (0V) on the UART_RX terminal, as shown in Figure 9.23. If t_{BRK} is longer than the value, defined by the PS Key PSKEY_HOST_IO_UART_RESET_TIMEOUT, (0x1a4), a reset will occur. This feature allows a host to initialise the system to a known state. Also, BlueCore2-ROM can emit a Break character that may be used to wake the Host.

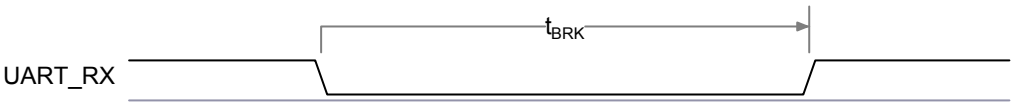


Figure 9.23: Break Signal

Note:

The DFU boot loader must be loaded into the Flash device before the UART or USB interfaces can be used. This initial flash programming can be done via the SPI.

Table 9.8 shows a list of commonly used baud rates and their associated values for the Persistent Store Key PSKEY_UART_BAUD_RATE (0x204). There is no requirement to use these standard values. Any baud rate within the supported range can be set in the Persistent Store Key according to the following formula:

$$\text{Baud Rate} = \frac{\text{PSKEY\_UART\_BAUD\_RATE}}{0.004096}$$

Baud Rate	Persistent Store Value		Error
	Hex	Dec	
1200	0x0005	5	1.73%
2400	0x000a	10	1.73%
4800	0x0014	20	1.73%
9600	0x0027	39	-0.82%
19200	0x004f	79	0.45%
38400	0x009d	157	-0.18%
57600	0x00ec	236	0.03%
76800	0x013b	315	0.14%
115200	0x01d8	472	0.03%
230400	0x03b0	944	0.03%
460800	0x075f	1887	-0.02%
921600	0x0ebf	3775	0.00%
1382400	0x161e	5662	-0.01%

Table 9.10: Standard Baud Rates

9.5.1 UART Bypass

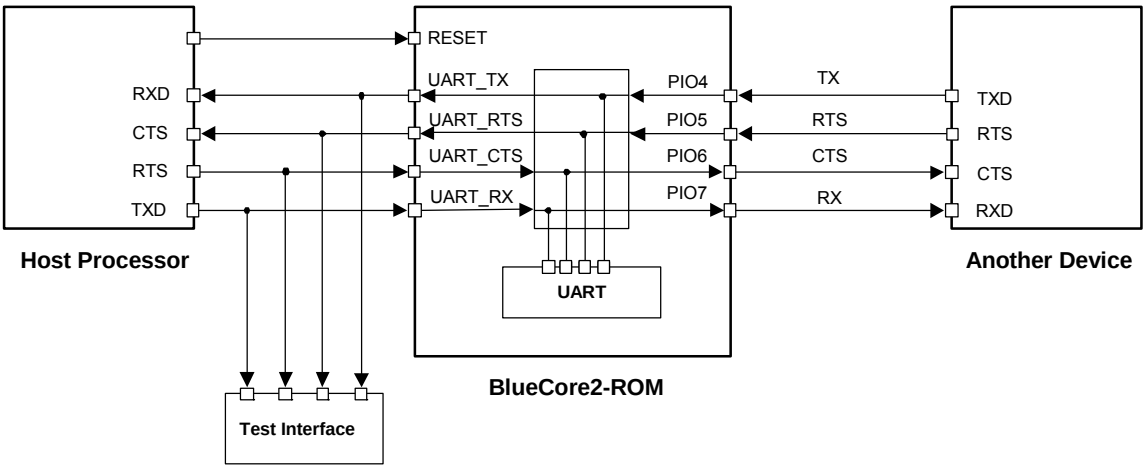


Figure 9.24: UART Bypass Architecture

9.5.2 UART Configuration while RESET is Active

The UART interface for BlueCore2-ROM while the chip is being held in reset is tri-statable. This will allow the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tri-state when BlueCore2-ROM reset is de-asserted and the firmware begins to run.

9.5.3 UART Bypass Mode

Alternatively, for devices that do not tri-state the UART bus, the UART bypass mode on BlueCore2-ROM can be used. The default state of BlueCore2-ROM after reset is de-asserted is for the host UART bus to be connected to the BlueCore2-ROM UART, thereby allowing communication to BlueCore2-ROM via the UART.

In order to apply the UART bypass mode, a BCCMD command will be issued to BlueCore2-ROM. It will switch the bypass to PIO[7:4], as shown in Figure 9.24. Once the bypass mode has been invoked, BlueCore2-ROM will enter the deep sleep state indefinitely.

In order to re-establish communication with BlueCore2-ROM, the chip must be reset so that the default configuration takes effect.

It is important for the host to ensure a clean Bluetooth disconnection of any active links before the bypass mode is invoked. Therefore it is not possible to have active Bluetooth links while operating the bypass mode.

9.5.4 Current Consumption In UART Bypass Mode

The current consumption for a device in UART Bypass Mode is equal to the values quoted for a device in standby mode.

9.6 USB Interface

BlueCore2-ROM USB devices contain a full speed (12Mbits/s) USB interface that is capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported. The set of USB endpoints implemented behave as specified in the USB section of the Bluetooth specification v1.1 and v1.2.

As USB is a Master/Slave oriented system (in common with other USB peripherals), BlueCore2-ROM only supports USB Slave operation.

9.6.1 USB Data Connections

The USB data lines emerge as pins USB_D+ and USB_D-. These terminals are connected to the internal USB I/O buffers of the BlueCore2-ROM and therefore have a low output impedance. To match the connection to the characteristic impedance of the USB cable, resistors must be placed in series with USB_D+ / USB_D- and the cable.

9.6.2 USB Pull-up Resistor

BlueCore2-ROM features an internal USB pull-up resistor. This pulls the USB_D+ pin weakly high when BlueCore2-ROM is ready to enumerate. It signals to the PC that it is a full speed (12Mbit/s) USB device.

The USB internal pull-up is implemented as a current source, and is compliant with Section 7.1.5 of the USB specification v1.1. The internal pull-up pulls USB_D+ high to at least 2.8V when loaded with a 15kΩ ±5% pull-down resistor (in the hub/host) when VDD_PADS=3.1V. This presents a Thevenin resistance to the host of at least 900Ω. Alternatively, an external 1.5kΩ pull-up resistor can be placed between a PIO line and D+ on the USB cable. The firmware must be alerted to which mode is used by setting PS Key PSKEY_USB_PIO_PULLUP appropriately. The default setting uses the internal pull-up resistor.

9.6.3 Power Supply

The USB specification dictates that the minimum output high voltage for USB data lines is 2.8V. To safely meet the USB specification, the voltage on the VDD_USB supply terminals must be an absolute minimum of 3.1V. CSR recommends 3.3V for optimal USB signal quality.

9.6.4 Self Powered Mode

In self powered mode, the circuit is powered from its own power supply and not from the VBUS (5V) line of the USB cable. It draws only a small leakage current (below 0.5mA) from VBUS on the USB cable. This is the easier mode for which to design for, as the design is not limited by the power that can be drawn from the USB hub or root port. However, it requires that VBUS be connected to BlueCore2-ROM via a resistor network (R_{vb1} and R_{vb2}), so BlueCore2-ROM can detect when VBUS is powered up. BlueCore2-ROM will not pull USB_D+ high when VBUS is off.

Self powered USB designs (powered from a battery or PSU) must ensure that a PIO line is allocated for USB pull-up purposes. A 1.5K 5% pull-up resistor between USB_DP and the selected PIO line should be fitted to the design. Failure to fit this resistor may result in the design failing to be USB compliant in self powered mode. The internal pull-up in BlueCore is only suitable for bus powered USB devices i.e. dongles.

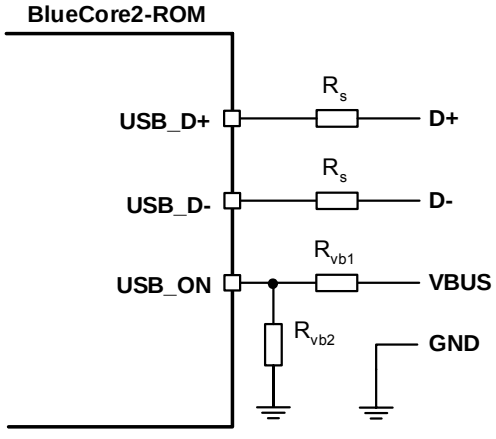


Figure 9.25: Connections to BlueCore2-ROM for Self Powered Mode

The terminal marked USB_ON can be any free PIO pin. The PIO pin selected must be registered by setting PSKEY_USB_PIO_VBUS to the corresponding pin number.

9.6.5 Bus Powered Mode

In bus powered mode the application circuit draws its current from the 5V VBUS supply on the USB cable. BlueCore2-ROM negotiates with the PC during the USB enumeration stage about how much current it is allowed to consume.

For Class 2 Bluetooth applications, CSR recommends that the regulator used to derive 3.3V from VBUS is rated at 100mA average current and should be able to handle peaks of 120mA without foldback or limiting. In bus powered mode, BlueCore2-ROM requests 100mA during enumeration.

For Class 1 Bluetooth applications, the USB power descriptor should be altered to reflect the amount of power required. This is accomplished by setting the PS Key PSKEY_USB_MAX_POWER (0x2c6). This is higher than for a Class 2 application due to the extra current drawn by the Transmit RF PA.

When selecting a regulator, be aware that VBUS may go as low as 4.4V. The inrush current (when charging reservoir and supply decoupling capacitors) is limited by the USB specification (see USB specification v1.1, Section 7.2.4.1). Some applications may require soft start circuitry to limit inrush current if more than 10μF is present between VBUS and GND.

The 5V VBUS line emerging from a PC is often electrically noisy. As well as regulation down to 3.3V and 1.8V, applications should include careful filtering of the 5V line to attenuate noise that is above the voltage regulator bandwidth. Excessive noise on the 1.8V supply to the analogue supply pins of BlueCore2-ROM will result in reduced receive sensitivity and a distorted RF transmit signal.

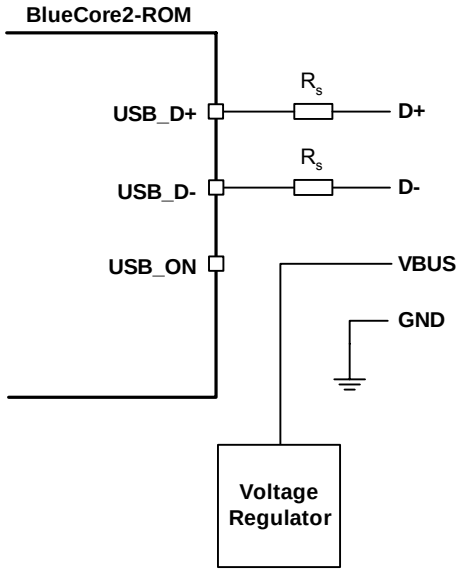


Figure 9.26: Connections to BlueCore2-ROM for Bus Powered Mode

Note:

USB_ON is shared with BlueCore2-ROM's PIO terminals

Identifier	Value	Function
R_s	27Ω nominal	Impedance matching to USB cable
R_{vb1}	22kΩ 5%	VBUS ON sense divider
R_{vb2}	47kΩ 5%	VBUS ON sense divider

Table 9.11: USB Interface Component Values

9.6.6 Suspend Current

USB devices that run off VBUS must be able to enter a suspended state, whereby they consume less that 0.5mA from VBUS. The voltage regulator circuit itself should draw only a small quiescent current (typically less than 100μA) to ensure adherence to the suspend current requirement of the USB specification. This is not normally a problem with modern regulators. Ensure that external LEDs and/or amplifiers can be turned off by BlueCore2-ROM. The entire circuit must be able to enter the suspend mode.

9.6.7 Detach and Wake_Up Signalling

BlueCore2-ROM can provide out-of-band signalling to a host controller by using the control lines called 'USB_DETACH' and 'USB_WAKE_UP'. These are outside the USB specification (no wires exist for them inside the USB cable), but can be useful when embedding BlueCore2-ROM into a circuit where no external USB is visible to the user. Both control lines are shared with PIO pins and can be assigned to any PIO pin by setting the PS Keys PSKEY_USB_PIO_DETACH and PSKEY_USB_PIO_WAKEUP to the selected PIO number.

USB_DETACH is an input which, when asserted high, causes BlueCore2-ROM to put USB_D- and USB_D+ in a high impedance state and turned off the pull-up resistor on D+. This detaches the device from the bus and is logically equivalent to unplugging the device. When USB_DETACH is taken low, BlueCore2-ROM will connect back to USB and await enumeration by the USB host.

USB_WAKE_UP is an active high output (used only when USB_DETACH is active) to wake up the host and allow USB communication to recommence. It replaces the function of the software USB WAKE_UP message (which runs over the USB cable), and cannot be sent while BlueCore2-ROM is effectively disconnected from the bus.

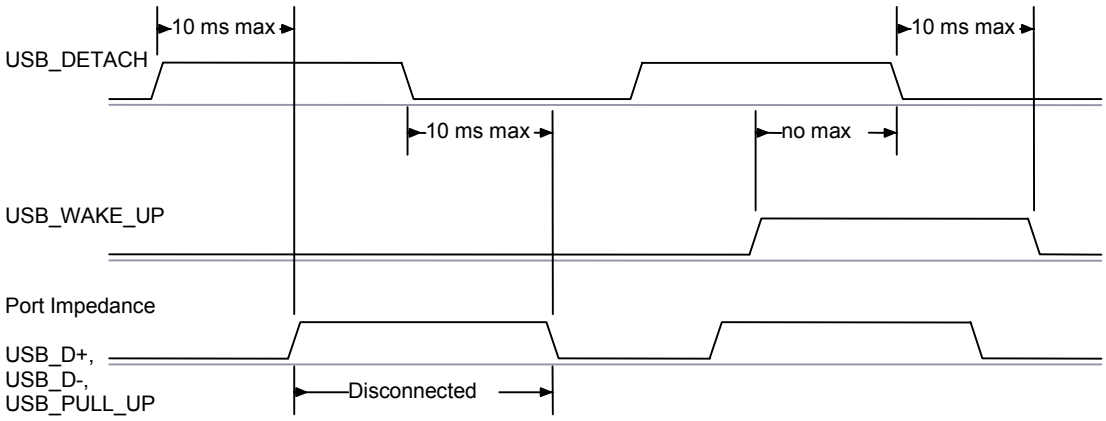


Figure 9.27: USB_DETACH and USB_WAKE_UP Signal

9.6.8 USB Driver

A USB Bluetooth device driver is required to provide a software interface between BlueCore2-ROM and Bluetooth software running on the host computer.

9.6.9 USB 1.1 Compliance

BlueCore2-ROM is qualified to the USB specification v1.1, details of which are available from http://www.usb.org. The specification contains valuable information on aspects such as PCB track impedance, supply inrush current and product labelling.

Although BlueCore2-ROM meets the USB specification, CSR cannot guarantee that an application circuit designed around the chip is USB compliant. The choice of application circuit, component choice and PCB layout all affect USB signal quality and electrical characteristics. The information in this document is intended as a guide and should be read in association with the USB specification, with particular attention being given to Chapter 7. Independent USB qualification must be sought before an application is deemed USB compliant and can bear the USB logo. Such qualification can be obtained from a USB plugfest or from an independent USB test house.

Terminals USB_D+ and USB_D- adhere to the USB specification 2.0 (Chapter 7) electrical requirements.

9.6.10 USB 2.0 Compatibility

BlueCore2-ROM is compatible with USB v2.0 host controllers; under these circumstances the two ends agree the mutually acceptable rate of 12Mbits/s according to the USB v2.0 specification.

9.7 Serial Peripheral Interface

BlueCore2-ROM uses 16-bit data and 16-bit address serial peripheral interface, where transactions may occur when the internal processor is running or is stopped. This section details the considerations required when interfacing to BlueCore2-ROM via the four dedicated serial peripheral interface terminals. Data may be written or read one word at a time or the auto increment feature may be used to access blocks.

9.7.1 Instruction Cycle

The BlueCore2-ROM is the slave and receives commands on SPI_MOSI and outputs data on SPI_MISO. The instruction cycle for a SPI transaction is shown in Table 9.12.

1	Reset the SPI interface	Hold SPI_CSB high for two SPI_CLK cycles
2	Write the command word	Take SPI_CSB low and clock in the 8 bit command
3	Write the address	Clock in the 16-bit address word
4	Write or read data words	Clock in or out 16-bit data word(s)
5	Termination	Take SPI_CSB high

Table 9.12: Instruction Cycle for an SPI Transaction

With the exception of reset, SPI_CSB must be held low during the transaction. Data on SPI_MOSI is clocked into the BlueCore2-ROM on the rising edge of the clock line SPI_CLK. When reading, BlueCore2-ROM will reply to the master on SPI_MISO with the data changing on the falling edge of the SPI_CLK. The master provides the clock on SPI_CLK. The transaction is teminated by taking SPI_CSB high.

Sending a command word and the address of a register for every time it is to be read or written is a significant overhead, especially when large amounts of data are to be transferred. To overcome this BlueCore2-ROM offers increased data transfer efficiency via an auto increment operation. To invoke auto increment, SPI_CSB is kept low, which auto increments the address, while providing an extra 16 clock cycles for each extra word to be written or read.

9.7.2 Writing to BlueCore2-ROM

To write to BlueCore2-ROM, the 8-bit write command (00000010) is sent first (C[7:0]) followed by a 16-bit address (A[15:0]). The next 16-bits (D[15:0]) clocked in on SPI_MOSI are written to the location set by the address (A). Thereafter for each subsequent 16-bits clocked in, the address (A) is incremented and the data written to consecutive locations until the transaction terminates when SPI_CSB is taken high.

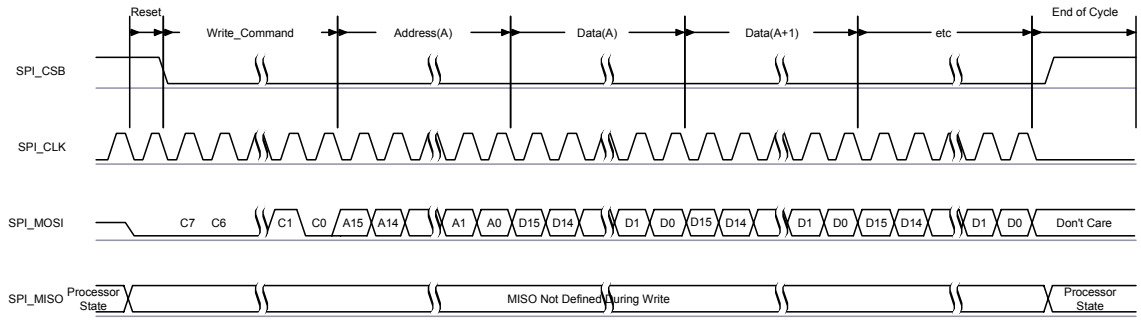


Figure 9.28: Write Operation

9.7.3 Reading from BlueCore2-ROM

Reading from BlueCore2-ROM is similar to writing to it. An 8-bit read command (00000011) is sent first (C[7:0]), followed by the address of the location to be read (A[15:0]). BlueCore2-ROM then outputs on SPI_MISO a check word during T[15:0] followed by the 16-bit contents of the addressed location during bits D[15:0].

The check word is composed of {command, address [15:8]}. The check word may be used to confirm a read operation to a memory location. This overcomes the problems encountered with typical serial peripheral interface slaves, whereby it is impossible to determine whether the data returned by a read operation is valid data or the result of the slave device not responding.

If SPI_CSB is kept low, data from consecutive locations is read out on SPI_MISO for each subsequent 16 clocks, until the transaction terminates when SPI_CSB is taken high.

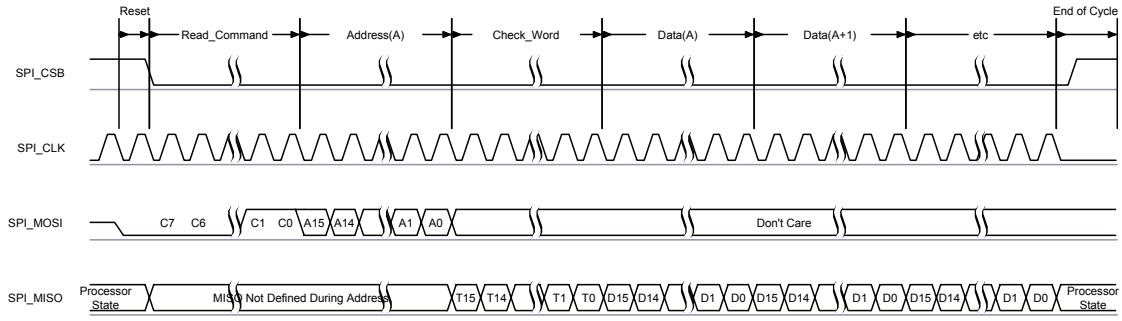


Figure 9.29: Read Operation

9.7.4 Multi Slave Operation

BlueCore2-ROM should not be connected in a multi slave arrangement by simple parallel connection of slave MISO lines. When BlueCore2-ROM is deselected (SPI_CSB = 1), the SPI_MISO line does not float, instead, BlueCore2-ROM outputs 0 if the processor is running or 1 if it is stopped.

9.8 PCM Interface

Pulse Code Modulation (PCM) is a standard method used to digitise human voice patterns for transmission over digital communication channels. Through its PCM interface, BlueCore2-ROM has hardware support for continual transmission and reception of PCM data, thus reducing processor overhead for wireless headset applications. BlueCore2-ROM offers a bi directional digital audio interface that routes directly into the baseband layer of the on chip firmware. It does not pass through the HCI protocol layer.

Hardware on BlueCore2-ROM allows the data to be sent to and received from a SCO connection.

Up to three SCO connections can be supported by the PCM interface at any one time[1].

BlueCore2-ROM can operate as the PCM interface Master generating an output clock of 128, 256 or 512kHz. When configured as PCM interface slave it can operate with an input clock up to 2048kHz. BlueCore2-ROM is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13 or 16-bit linear, 8-bit μ–law or A-law companded sample formats at 8ksamples/s and can receive and transmit on any selection of three of the first four slots following PCM_SYNC. The PCM configuration options are enabled by setting the PS Key PS KEY_PCM_CONFIG (0x1b3).

BlueCore2-ROM interfaces directly to PCM audio devices includes the following:

- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
- OKI MSM7705 four channel A-law and μ–law CODEC
- Motorola MC145481 8-bit A-law and μ–law CODEC
- Motorola MC145483 13-bit linear CODEC
- BlueCore2-ROM is also compatible with the Motorola SSITM interface

Note:

[1] Subject to firmware support, contact CSR for current status.

9.8.1 PCM Interface Master/Slave

When configured as the Master of the PCM interface, BlueCore2-ROM generates PCM_CLK and PCM_SYNC.

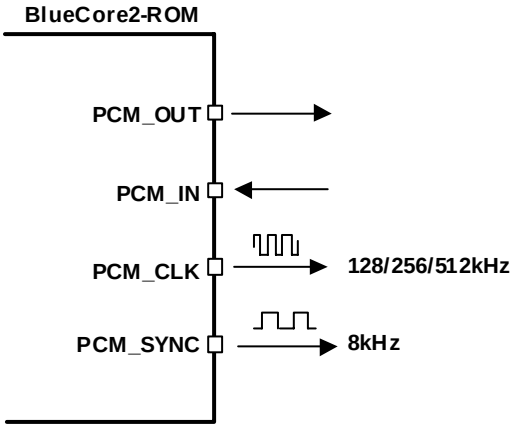


Figure 9.30: BlueCore2-ROM as PCM Interface Master

When configured as the Slave of the PCM interface, BlueCore2-ROM accepts PCM_CLK rates up to 2048kHz.

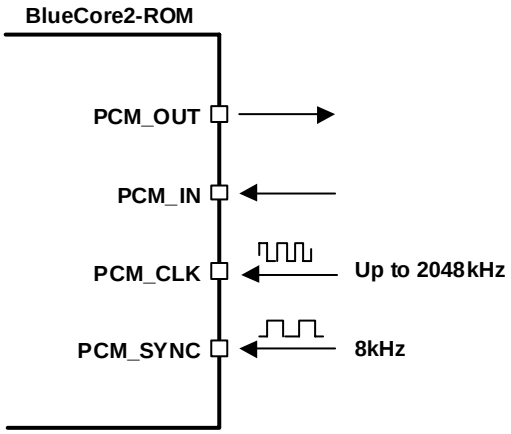


Figure 9.31: BlueCore2-ROM as PCM Interface Slave

9.8.2 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When BlueCore2-ROM is configured as PCM Master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is (8-bits) long. When BlueCore2-ROM is configured as PCM Slave, PCM_SYNC may be from two consecutive falling edges of PCM_CLK to half the PCM_SYNC rate i.e. 62.5μs long.

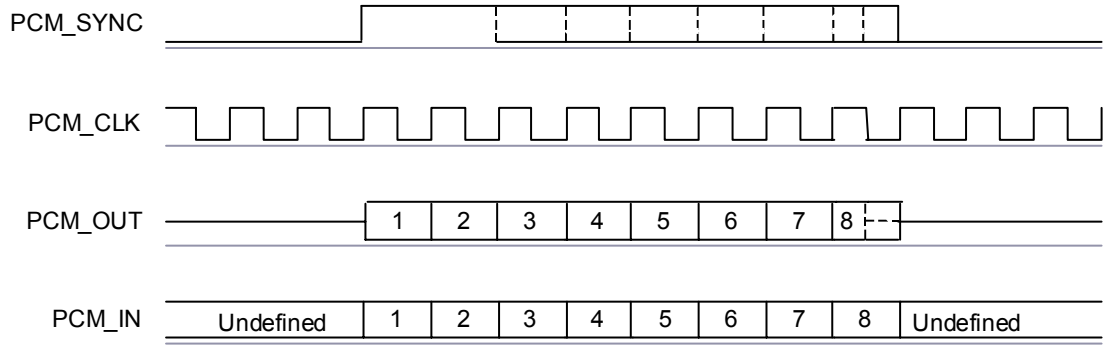


Figure 9.32: Long Frame Sync (Shown with 8-bit Companded Sample)

BlueCore2-ROM samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

9.8.3 Short Frame Sync

In Short Frame Sync the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

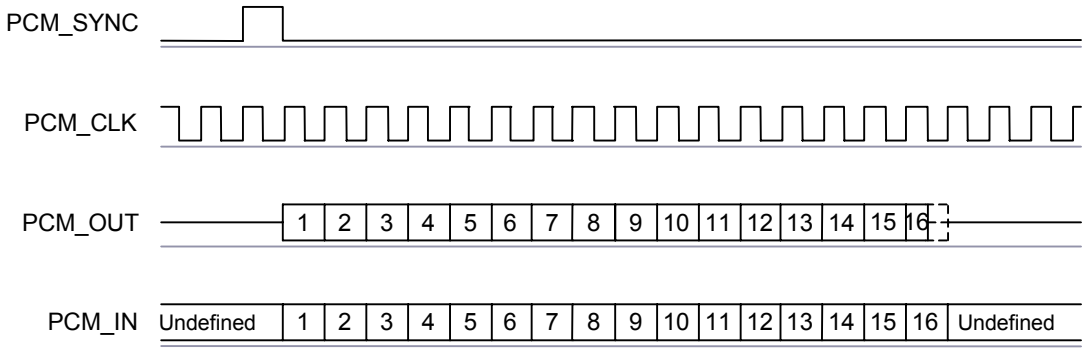


Figure 9.33: Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, BlueCore2-ROM samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

9.8.4 Multi Slot Operation

More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCO connections can be carried over any of the first four slots.

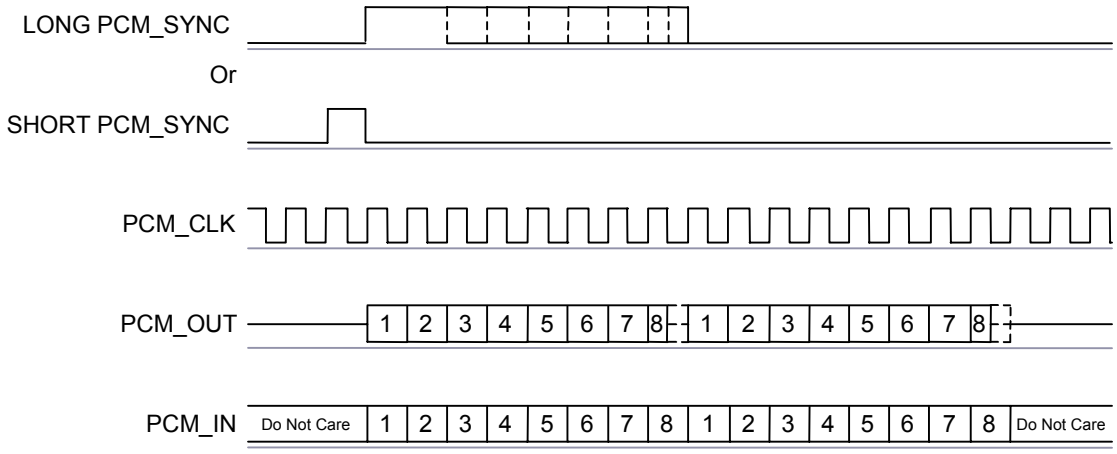


Figure 9.34: Multi slot Operation with Two Slots and 8-bit Companded Samples

9.8.5 GCI Interface

BlueCore2-ROM is compatible with the General Circuit Interface, a standard synchronous 2B+D ISDN timing interface. The two 64Kbps B channels can be accessed when this mode is configured.

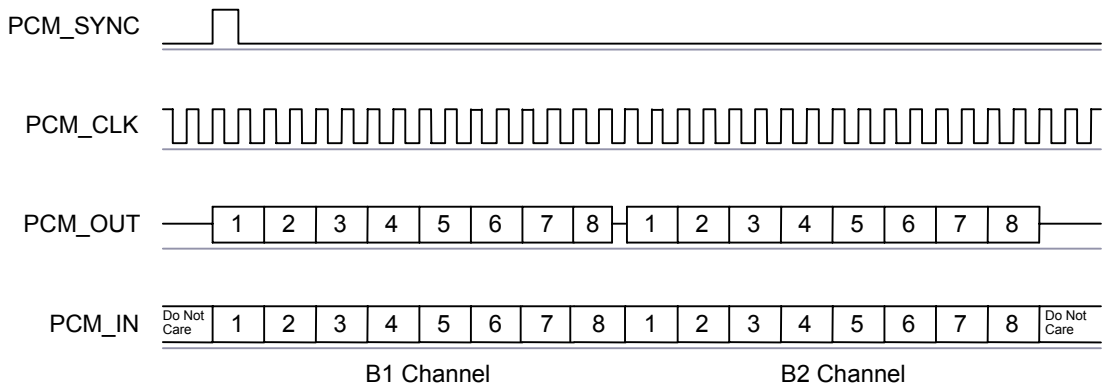


Figure 9.35: GCI Interface

The start of frame is indicated by the rising edge of PCM_SYNC and runs at 8kHz. With BlueCore2-ROM in Slave mode, the frequency of PCM_CLK can be up to 4.096MHz.

9.8.6 Slots and Sample Formats

BlueCore2-ROM can receive and transmit on any selection of the first four slots following each sync pulse. Slot durations can be either 8 or 16 clock cycles. Duration's of 8 clock cycles may only be used with 8-bit sample formats. Durations of 16 clocks may be used with 8, 13 or 16-bit sample formats.

BlueCore2-ROM supports 13-bit linear, 16-bit linear and 8-bit μ-law or A-law sample formats. The sample rate is 8ksamples/s. The bit order may be little or big endian. When 16-bit slots are used, the 3 or 8 unused bits in each slot may be filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some Motorola CODECs.

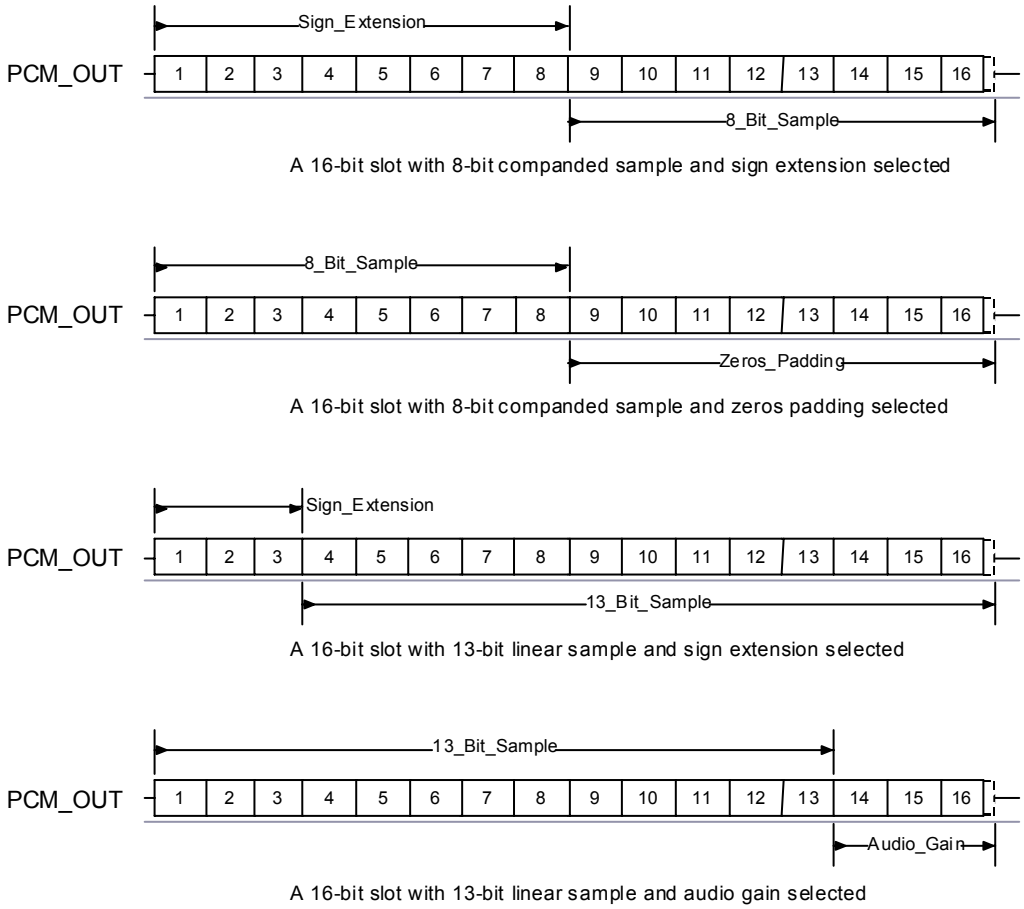


Figure 9.36: 16-bit Slot Length and Sample Formats

9.8.7 Additional Features

BlueCore2-ROM has a mute facility that forces PCM_OUT to be 0. In Master mode, PCM_SYNC may also be forced to 0 while keeping PCM_CLK running which some CODECS use to control power down.

9.8.8 PCM Timing Information

Symbol	Parameter	Min	Typ	Max	Unit
f_{mclk}	PCM_CLK frequency	-	128 256 512	-	kHz
-	PCM_SYNC frequency	-	8		kHz
t_{mclkh} (1)	PCM_CLK high	980	-	-	ns
t_{mclkl} (1)	PCM_CLK low	730	-		ns
$t_{dmclksynch}$	Delay time from PCM_CLK high to PCM_SYNC high	-	-	20	ns
$t_{dmclkpout}$	Delay time from PCM_CLK high to valid PCM_OUT	-	-	20	ns
$t_{dmclklsyncl}$	Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only)	-	-	20	ns
$t_{dmclkhsyncl}$	Delay time from PCM_CLK high to PCM_SYNC low	-	-	20	ns
$t_{dmclklpoutz}$	Delay time from PCM_CLK low to PCM_OUT high impedance	-	-	20	ns
$t_{dmclkhpoutz}$	Delay time from PCM_CLK high to PCM_OUT high impedance	-	-	20	ns
$t_{supinclkl}$	Set-up time for PCM_IN valid to PCM_CLK low	30	-	-	ns
$t_{hpinclkl}$	Hold time for PCM_CLK low to PCM_IN invalid	10	-	-	ns
t_r	Edge rise time (C_l = 50 pf, 10-90 %)	-	-	15	ns
t_f	Edge fall time (C_l = 50 pf, 10-90 %)	-	-	15	ns

Table 9.13: PCM Master Timing

Note:

(1) Assumes normal system clock operation. Figures will vary during low power modes, when system clock speeds are reduced.

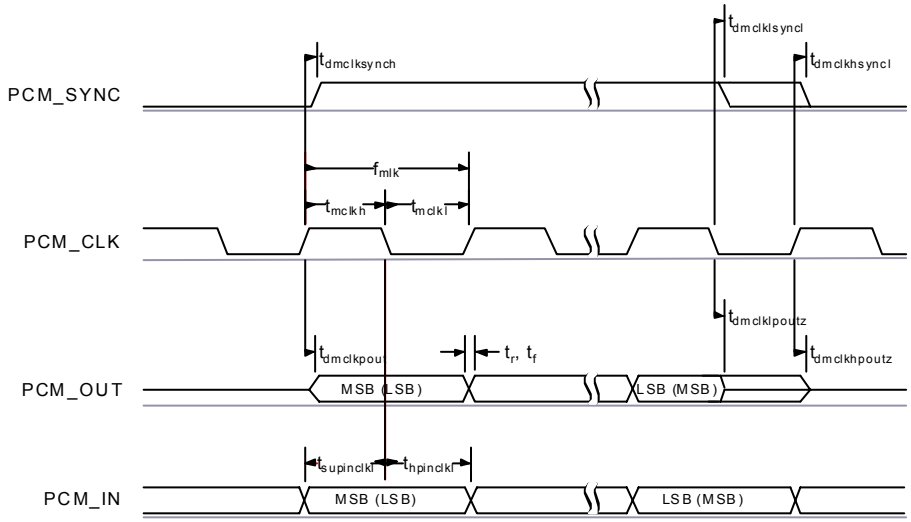


Figure 9.37: PCM Master Timing (Long Frame Sync)

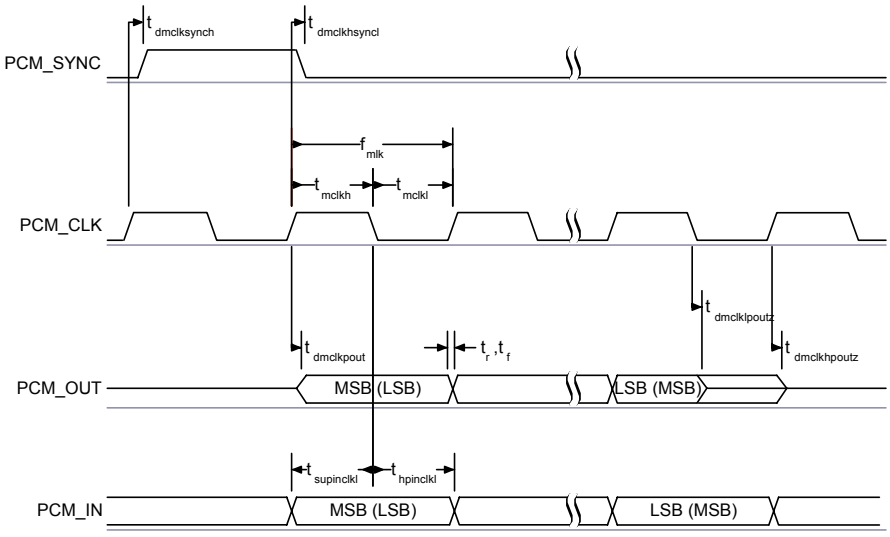


Figure 9.38: PCM Master Timing (Short Frame Sync)

9.8.9 PCM Slave Timing

Symbol	Parameter	Min	Typ	Max	Unit
f_{sclk}	PCM clock frequency (Slave mode: input)	64	-	2048	kHz
f_{sclk}	PCM clock frequency (GCI mode)	128	-	4096	kHz
t_{sclkl}	PCM_CLK low time	200	-	-	ns
t_{sclkh}	PCM_CLK high time	200	-	-	ns
$t_{hsclksynch}$	Hold time from PCM_CLK low to PCM_SYNC high	30	-	-	ns
$t_{susclksynch}$	Set-up time for PCM_SYNC high to PCM_CLK low	30	-	-	ns
t_{dpout}	Delay time from PCM_SYNC or PCM_CLK whichever is later, to valid PCM_OUT data (Long Frame Sync only)	-	-	20	ns
$t_{dsclkhpout}$	Delay time from CLK high to PCM_OUT valid data	-	-	20	ns
t_{dpoutz}	Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	20	ns
$t_{supinsclkl}$	Set-up time for PCM_IN valid to CLK low	30	-	-	ns
$t_{hpinsclkl}$	Hold time for PCM_CLK low to PCM_IN invalid	30	-		ns
t_r	Edge rise time (C_l = 50 pF, 10-90 %)	-	-	15	ns
t_f	Edge fall time (C_l = 50 pF, 10-90 %)	-	-	15	ns

Table 9.14: PCM Slave Timing

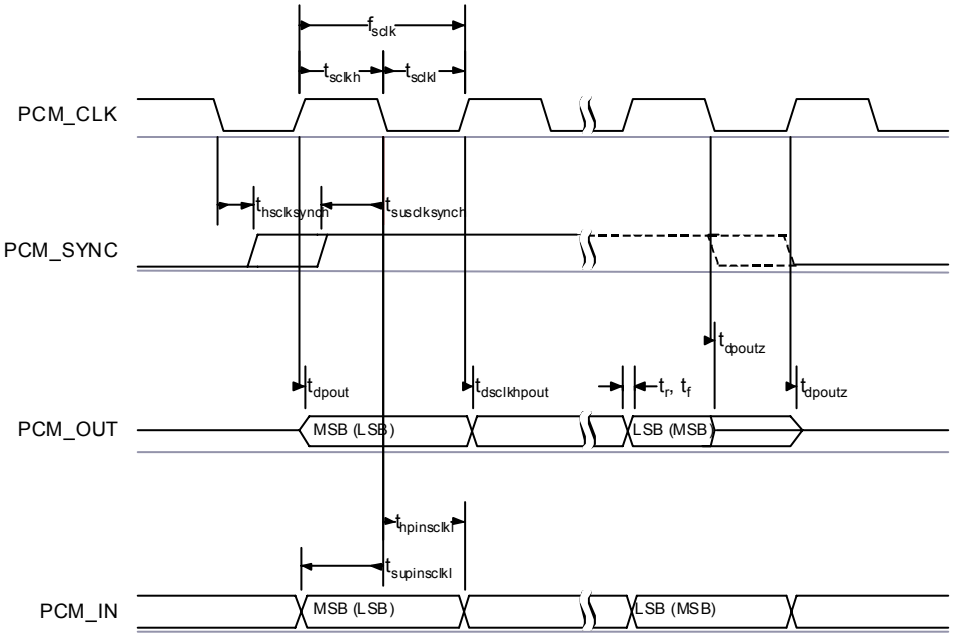


Figure 9.39: PCM Slave Timing (Long Frame Sync)

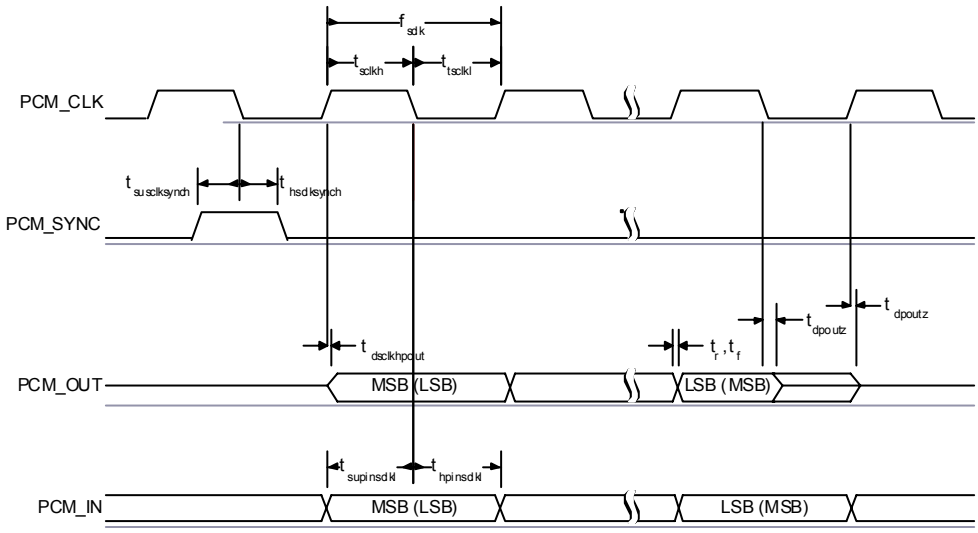


Figure 9.40: PCM Slave Timing (Short Frame Sync)

9.8.10 PCM_CLK and PCM_SYNC Generation

BlueCore2-ROM has two methods of generating PCM_CLK and PCM_SYNC in master mode. The first is generating these signals by Direct Digital Synthesis (DDS) from BlueCore2-ROM internal 4MHz clock (which is used in BlueCore2-External). Using this mode limits PCM_CLK to 128, 256 or 512kHz and PCM_SYNC to 8kHz. The second is generating PCM_CLK and PCM_SYNC by DDS from an internal 48MHz clock which allows a greater range of frequencies to be generated with low jitter but consumes more power. This second method is selected by setting bit '48M_PCM_CLK_GEN_EN' in PSKEY_PCM_CONFIG32. Note that bit 'SLAVE_MODE_EN' should also be set. When in this mode and with long frame sync, the length of PCM_SYNC can be either 8 or 16 cycles of PCM_CLK, determined by 'LONG_LENGTH_SYNC_EN' in PSKEY_PCM_CONFIG32.

The following equation describes PCM_CLK frequency when being generated using the internal 48MHz clock:

$$\frac{CNT\_RATE}{CNT\_LIMIT} \times 24MHz$$

The frequency of PCM_SYNC relative to PCM_CLK can be set using following equation:

$$\frac{PCM\_CLK}{SYNC\_LIMIT \times 8}$$

CNT_RATE, CNT_LIMIT and SYNC_LIMIT are set using PSKEY_PCM_LOW_JITTER_CONFIG. As an example, to generate PCM_CLK at 512kHz with PCM_SYNC at 8kHz, set PSKEY_PCM_LOW_JITTER_CONFIG to 0x08080177.

9.8.11 PCM Configuration

The PCM configuration is set using two PS Keys, PSKEY_PCM_CONFIG32 and PSKEY_PCM_LOW_JITTER_CONFIG. The following tables detail these PS Keys. PSKEY_PCM_CONFIG32. The default for this key is 0x00800000, i.e., first slot following sync is active, 13-bit linear voice format, long frame sync and interface master generating 256kHz PCM_CLK from 4MHz internal clock with no tristating of PCM_OUT. PSKEY_PCM_LOW_JITTER_CONFIG is described in Table 9.16.

Name	Bit Position	Description
-	0	Set to 0.
SLAVE_MODE_EN	1	0 selects Master mode with internal generation of PCM_CLK and PCM_SYNC. 1 selects Slave mode requiring externally generated PCM_CLK and PCM_SYNC. This should be set to 1 if 48M_PCM_CLK_GEN_EN (bit 11) is set.
SHORT_SYNC_EN	2	0 selects long frame sync (rising edge indicates start of frame), 1 selects short frame sync (falling edge indicates start of frame).
-	3	Set to 0.
SIGN_EXTEND_EN	4	0 selects padding of 8 or 13-bit voice sample into a 16-bit slot by inserting extra lsbs, 1 selects sign extension. When padding is selected with 13-bit voice sample, the 3 padding bits are the audio gain setting; with 8-bit samples the 8 padding bits are zeroes.
LSB_FIRST_EN	5	0 transmits and receives voice samples MSB first, 1 uses LSB first.
TX_TRISTATE_EN	6	0 drives PCM_OUT continuously, 1 tri-states PCM_OUT immediately after the falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is not active.
TX_TRISTATE_RISING_EDGE_EN	7	0 tristates PCM_OUT immediately after the falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is also not active. 1 tristates PCM_OUT after the rising edge of PCM_CLK.
SYNC_SUPPRESS_EN	8	0 enables PCM_SYNC output when master, 1 suppresses PCM_SYNC whilst keeping PCM_CLK running. Some CODECS utilise this to enter a low power state.
GCI_MODE_EN	9	1 enables GCI mode.
MUTE_EN	10	1 forces PCM_OUT to 0.
48M_PCM_CLK_GEN_EN	11	0 sets PCM_CLK and PCM_SYNC generation via DDS from internal 4 MHz clock, as for BlueCore2-External. 1 sets PCM_CLK and PCM_SYNC generation via DDS from internal 48 MHz clock.
LONG_LENGTH_SYNC_EN	12	0 sets PCM_SYNC length to 8 PCM_CLK cycles and 1 sets length to 16 PCM_CLK cycles. Only applies for long frame sync and with 48M_PCM_CLK_GEN_EN set to 1.
-	[20:16]	Set to 0b00000.
MASTER_CLK_RATE	[22:21]	Selects 128 (0b01), 256 (0b00), 512 (0b10) kHz PCM_CLK frequency when master and 48M_PCM_CLK_GEN_EN (bit 11) is low.
ACTIVE_SLOT	[26:23]	Default is '0001'. Ignored by firmware.
SAMPLE_FORMAT	[28:27]	Selects between 13 (0b00), 16 (0b01), 8 (0b10) bit sample with 16 cycle slot duration or 8 (0b11) bit sample with 8 cycle slot duration.
-	[32:29]	Set to 0

Table 9.15: PSKEY_PCM_CONFIG32 Description

Name	Bit Position	Description
CNT_LIMIT	[12:0]	Sets PCM_CLK counter limit.
CNT_RATE	[23:16]	Sets PCM_CLK count rate.
SYNC_LIMIT	[31:24]	Sets PCM_SYNC division relative to PCM_CLK.

Table 9.16: PSKEY_PCM_LOW_JITTER_CONFIG Description

9.9 I/O Parallel Ports

Fifteen lines of programmable bi directional input/outputs (I/O) are provided. PIO[11:8] and PIO[3:0] are powered from VDD_PIO. PIO[7:4] are powered from VDD_PADS. AIO [2:0] are powered from VDD_MEM.

PIO lines can be configured through software to have either weak or strong pull-ups or pull-downs. All PIO lines are configured as inputs with weak pull-downs at reset.

BlueCore2-ROM has three general purpose analogue interface pins, AIO[0], AIO[1] and AIO[2]. These are used to access internal circuitry and control signals. One pin is allocated to decoupling for the on-chip bandgap reference voltage, the other two may be configured to provide additional functionality.

Auxiliary functions available via these pins include an 8-bit ADC and an 8-bit DAC. Typically the ADC is used for battery voltage measurement. Signals selectable at these pins include the bandgap reference voltage and a variety of clock signals; 48, 24, 16, 8MHz and the XTAL clock frequency. When used with analogue signals the voltage range is constrained by the analogue supply voltage (1.8V). When configured to drive out digital level signals (clocks) generated from within the analogue part of the device, the output voltage level is determined by VDD_MEM (1.8V).

9.10 I²C Interface

PIO[8:6] can be used to form a Master I²C interface. The interface is formed using software to drive these lines. Therefore it is suited only to relatively slow functions such as driving a dot matrix liquid crystal display (LCD), keyboard scanner or EEPROM.

Note:

PIO lines need to be pulled-up through 2.2kΩ resistors.

For connection to EEPROMs, refer to CSR documentation on I²C EEPROMS for use with BlueCore. This provides information on the type of devices which are currently supported.

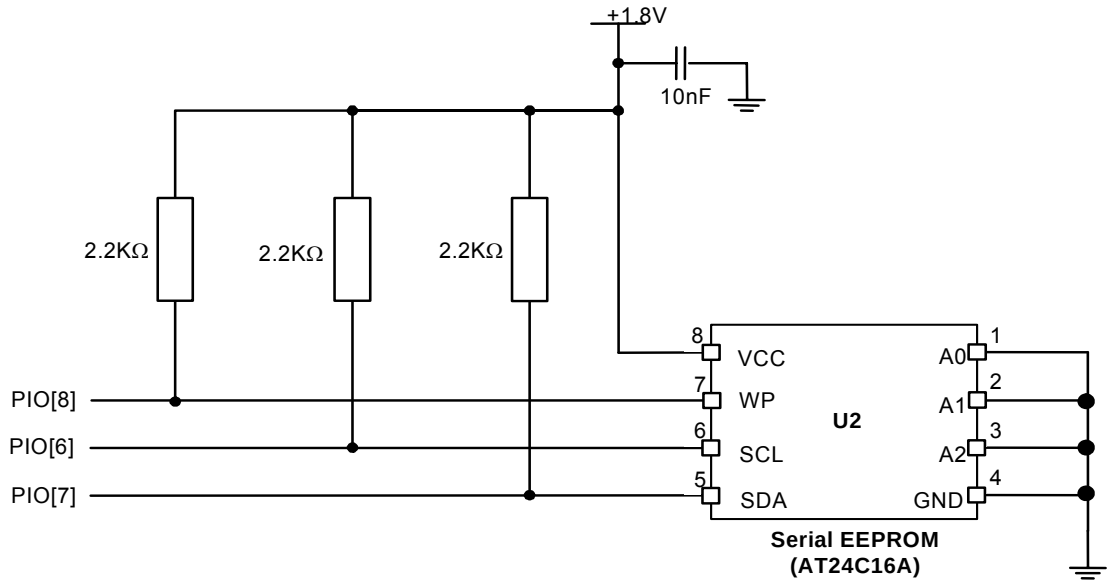


Figure 9.41: Example EEPROM Connection

9.11 TCXO Enable OR Function

An OR function exists for clock enable signals from a host controller and BlueCore2-ROM where either device can turn on the clock without having to wake up the other device. PIO[3] can be used as the Host clock enable input and PIO[2] can be used as the OR output with the TCXO enable signal from BlueCore2-ROM.

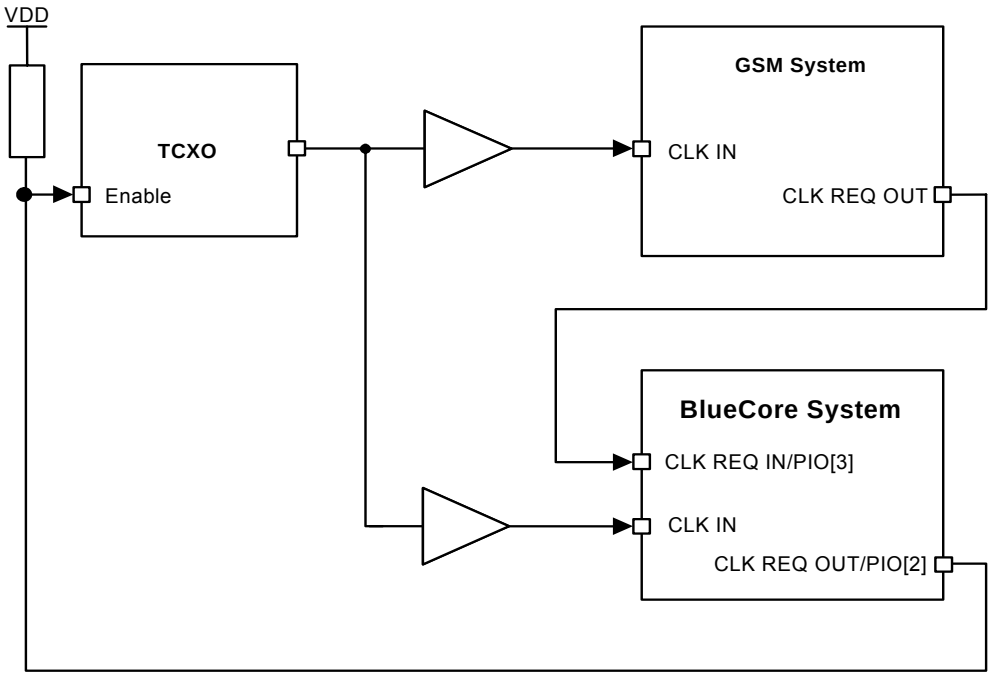


Figure 9.42: Example TXCO Enable OR Function

On reset and up to the time the PIO has been configured, PIO[2] will be tri-stated. Therefore, the developer must ensure that the circuitry connected to this pin is pulled via a 47kΩ resistor to the appropriate power rail. This ensures that the TCXO is oscillating at start up.

9.12 Reset and ResetB

BlueCore2-ROM may be reset from several sources: RESET or RESETB pins, power on reset, a UART break character or via a software configured watchdog timer.

The RESET pin is an active high reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESET being active. It is recommended that RESET is applied for a period greater than 5ms. The RESETB pin is the active low version of RESET and is 'ORed' on chip with the active high RESET with either causing the reset function.

The power on reset occurs when the VDD_CORE supply falls below typically 1.5V and is released when VDD_CORE rises above typically 1.6V.

At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tristated. The PIOs have weak pull-downs.

Following a reset, BlueCore2-ROM assumes the maximum XTAL_IN frequency which ensures that the internal clocks run at a safe (low) frequency until BlueCore-ROM is configured for the actual XTAL_IN frequency. If no clock is present at XTAL_IN, the oscillator in BlueCore2-ROM free runs, again at a safe frequency.

9.12.1 Pin States on Reset

Table 9.17 shows the pin states of BlueCore2-ROM on reset.

Pin name	State: BlueCore2-ROM
PIO[11:0]	Input with weak pull-down
PCM_OUT	Tri-stated with weak pull-down
PCM_IN	Input with weak pull-down
PCM_SYNC	Input with weak pull-down
PCM_CLK	Input with weak pull-down
UART_TX	Output tri-stated with weak pull-up
UART_RX	Input with weak pull-down
UART_RTS	Output tri-stated with weak pull-up
UART_CTS	Input with weak pull-down
USB_DP	Input with weak pull-down
USB_DN	Input with weak pull-down
SPI_CSB	Input with weak pull-up
SPI_CLK	Input with weak pull-down
SPI_MOSI	Input with weak pull-down
SPI_MISO	Output tri-stated with weak pull-down
AIO[2:0]	Output, driving low
RESET	Input with weak pull-down
RESETB	Input with weak pull-up
TEST_EN	Input with strong pull-down
AUX_DAC	High impedance
TX_A	High impedance
TX_B	High impedance
RX_IN	High impedance
LOOP_FILTER	High impedance
XTAL_IN	High impedance, 250k to XTAL_OUT
XTAL_OUT	High impedance, 250k to XTAL_OUT

Table 9.17: Pin States of BlueCore2-ROM on Reset

9.12.2 Status after Reset

The chip status after a reset is as follows:

- Warm Reset: baud rate and RAM data remain available
- Cold Reset[(1)]: baud rate and RAM data not available

Note:

(1) Cold Reset consititutes one of the following: power cycle, system reset (firmware fault code), reset signal

9.13 Power Supply

9.13.1 Voltage Regulator

An on-chip linear voltage regulator can be used to power the 1.8V dependent supplies. It is advised that a smoothing circuit using a 2.2μF low ESR capacitor and 2.2Ω resistor be placed on the output VDD_ANA.

The regulator is switched into a low power mode when the device is sent into deep sleep mode. When the on chip regulator is not required VDD_ANA is a 1.8V input and VREG_IN must be either open circuit or tied to VDD_ANA.

It is recommended that VDD_CORE, VDD_RADIO, VDD_VCO and VDD_MEM are powered at the same time. The order of powering supplies for VDD_CORE, VDD_PIO, VDD_PADS and VDD_USB is not important; however if VDD_CORE is not present all inputs have a weak pull-down irrespective of the reset state.

9.13.2 Sensitivity to Disturbances

It is recommended that if you are supplying BlueCore2-ROM from an external voltage source that VDD_VCO, VDD_ANA and VDD_RADIO should have less than 10mV RMS noise levels between 0 to 10MHz. Single tone frequencies are also to be avoided. A simple RC filter is recommended for VDD_CORE as this reduces transients put back onto the power supply rails.

The transient response of the regulator is also important as at the start of a packet, power consumption will jump to the levels defined in average current consumption section. It is essential that the power rail recovers quickly, so the regulator should have a response time of 20μs or less.

10 Typical Radio Performance

10.1 Transmitter Performance

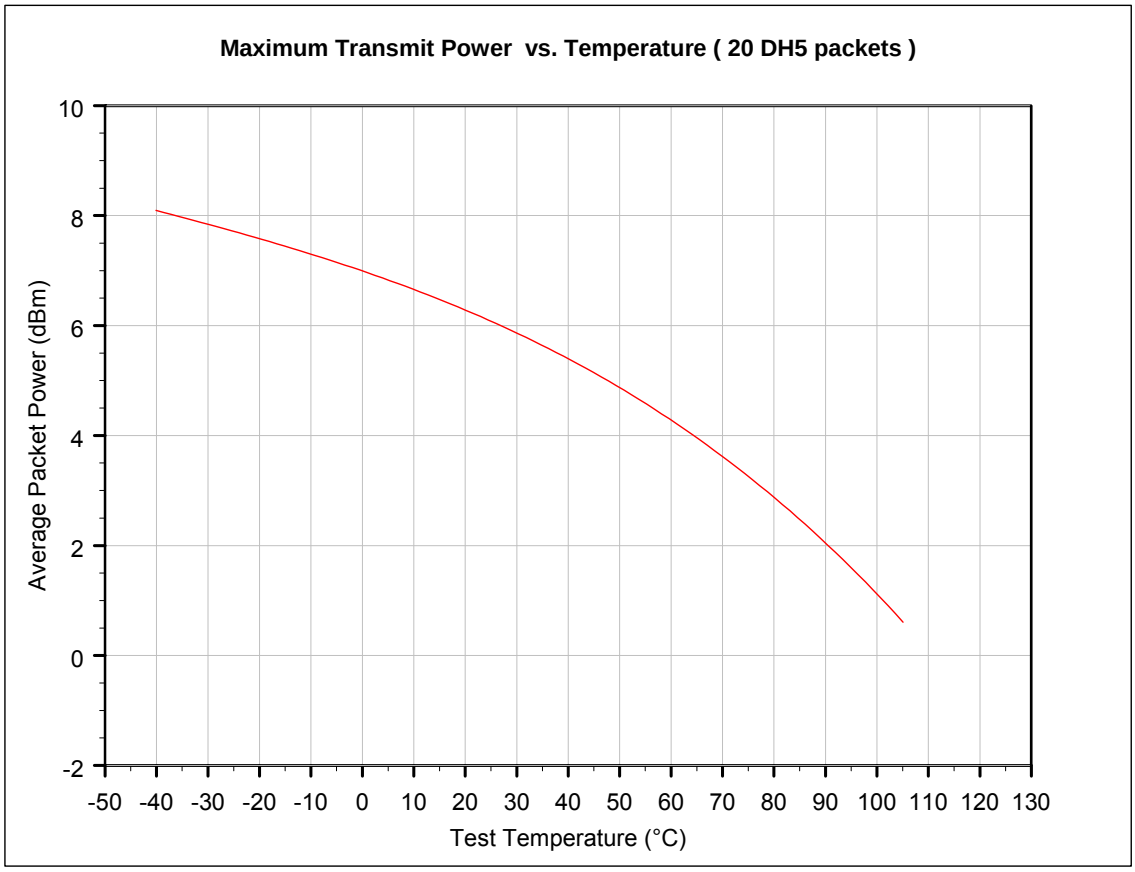


Figure 10.1: Variation of Transmit Power vs. Temperature

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63.

Output power temperature compensation disabled.

The actual power output during Bluetooth activity is controlled by the firmware to compensate for temperature variation.

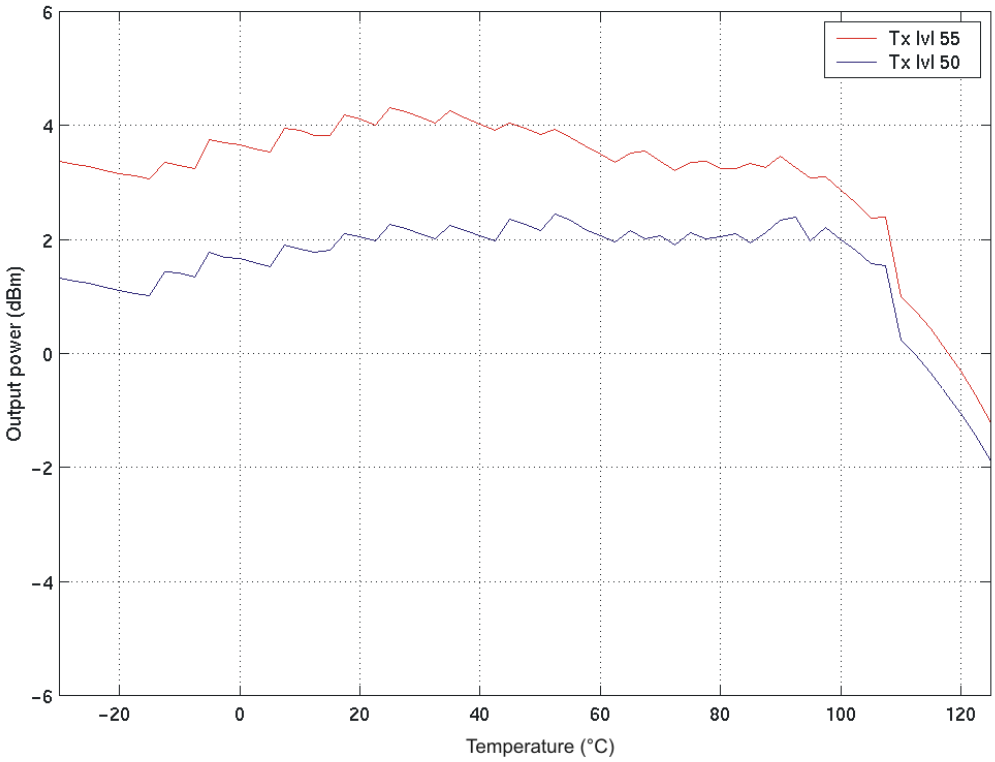


Figure 10.2: Firmware Controlled Output Power vs. Temperature

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63.

Output power temperature compensation enabled.

Persistent store settings for output power set to 50 and 55 respectively.

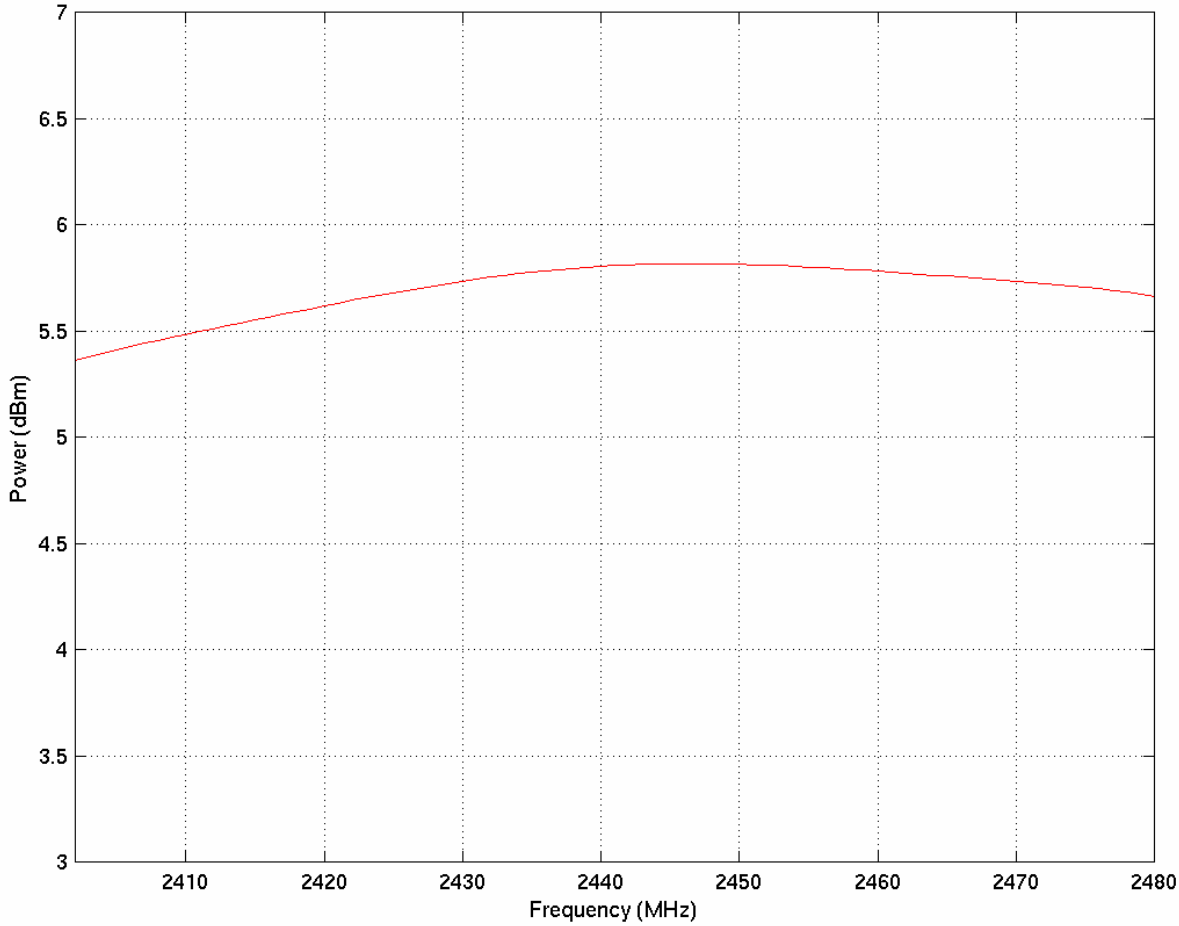


Figure 10.3: Variation of Transmit Power with Frequency

Note:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63.

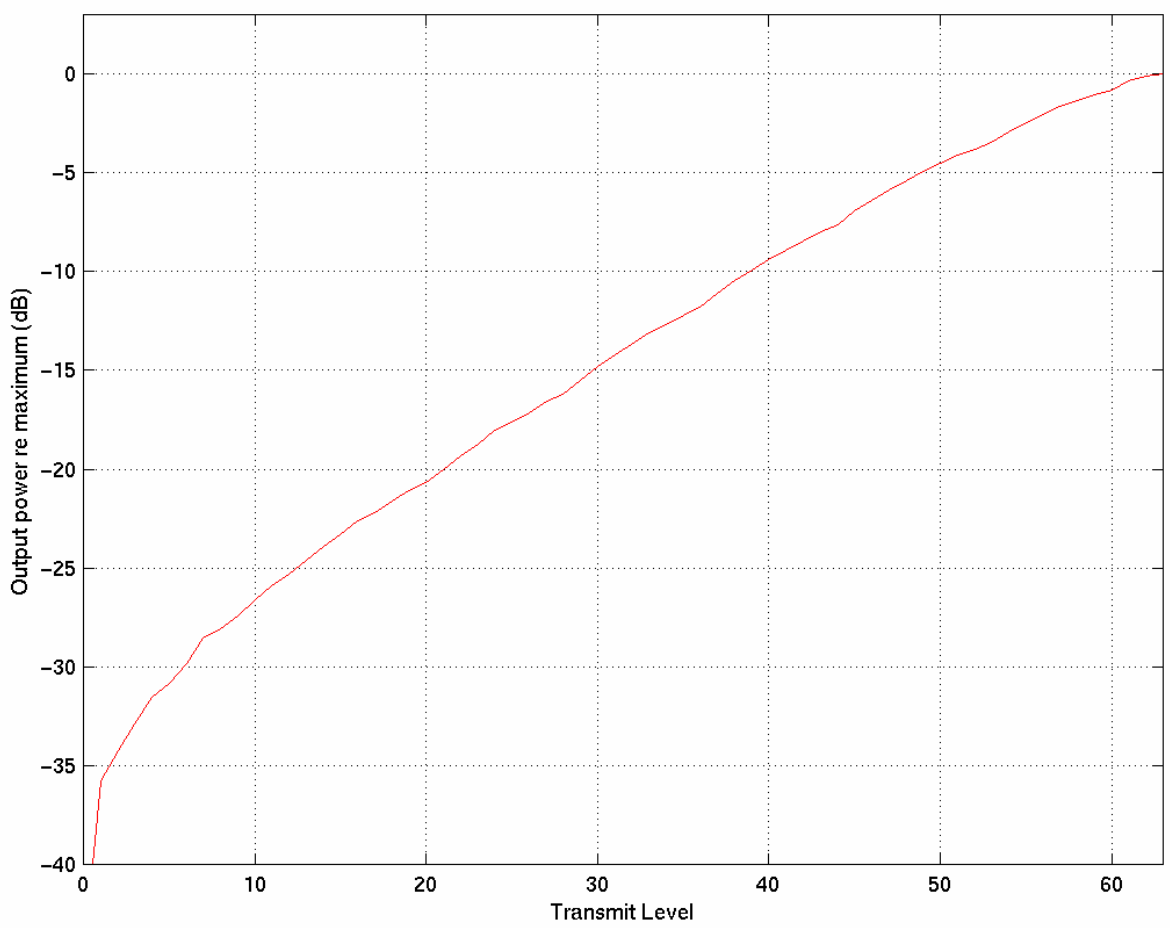


Figure 10.4: Power Control Characteristics

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63.

Temperature: 20°C

Relative to maximum output power

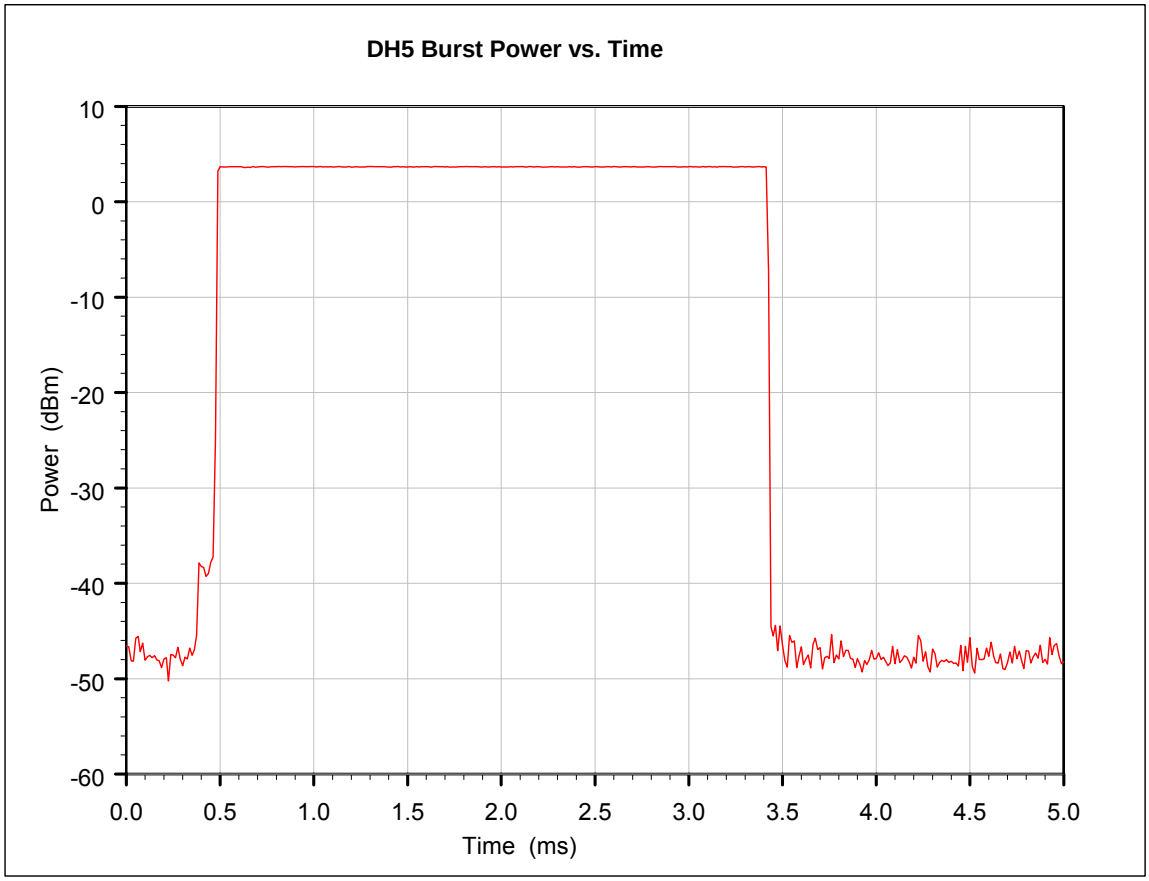


Figure 10.5: Power Flatness Across Packet

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63.

Temperature: 20°C

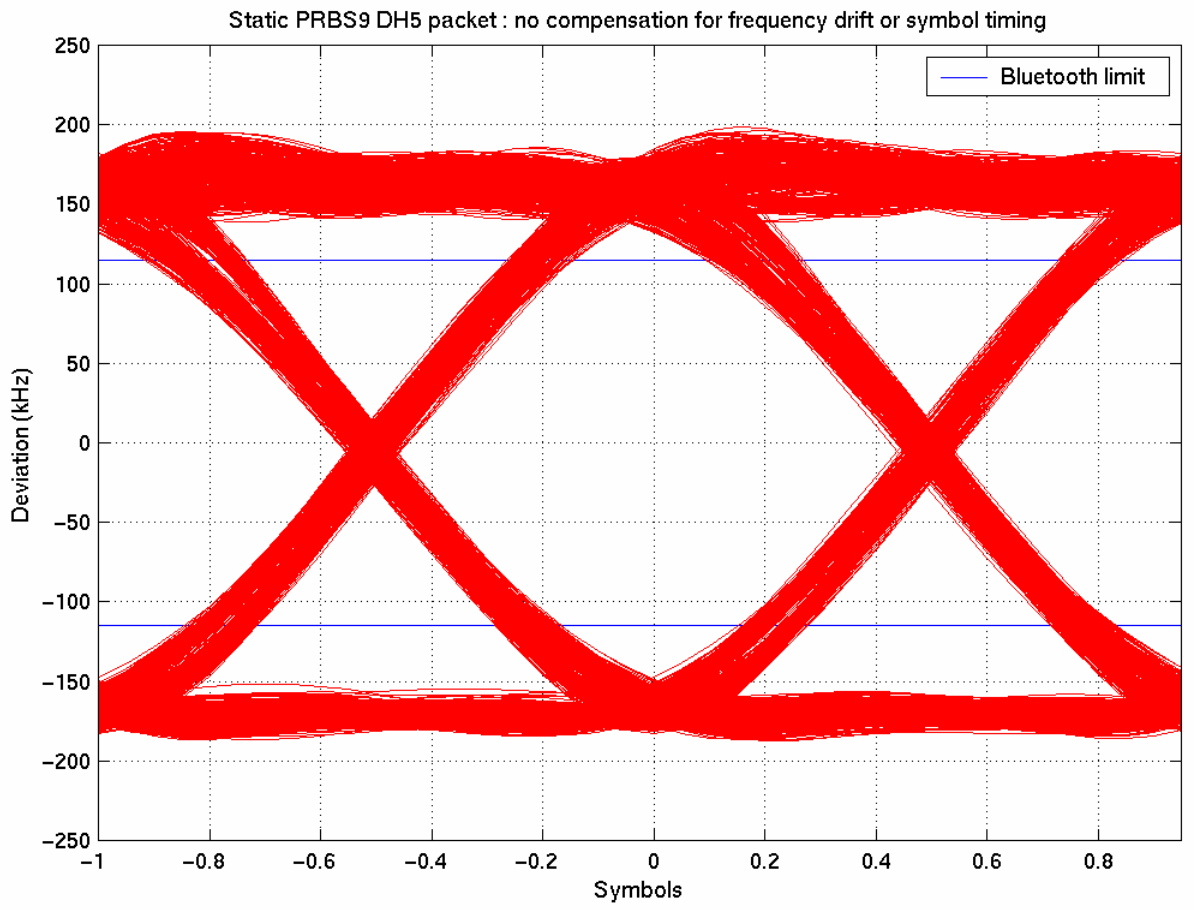


Figure 10.6: Transmitter Eye Diagram

Notes:

Results obtained using CSR's evaluation circuit shown in Figure 10.63.

Data: complete DH5 packet including pre amble

Temperature: 20°C

Output power at maximum

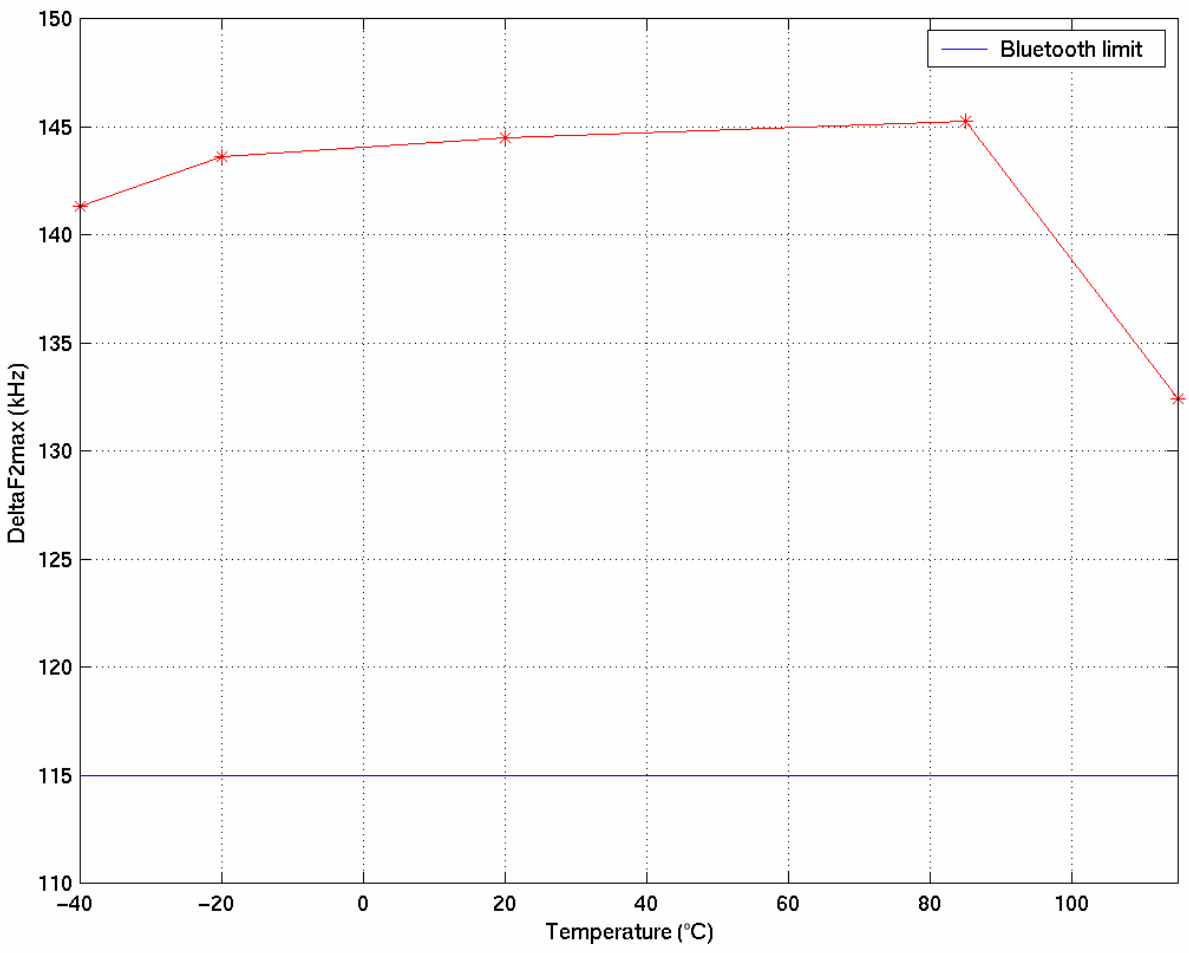


Figure 10.7: Minimum Modulation vs. Temperature

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63.

Minimum allowed modulation depth

Temperature: 20°C

Output power at maximum

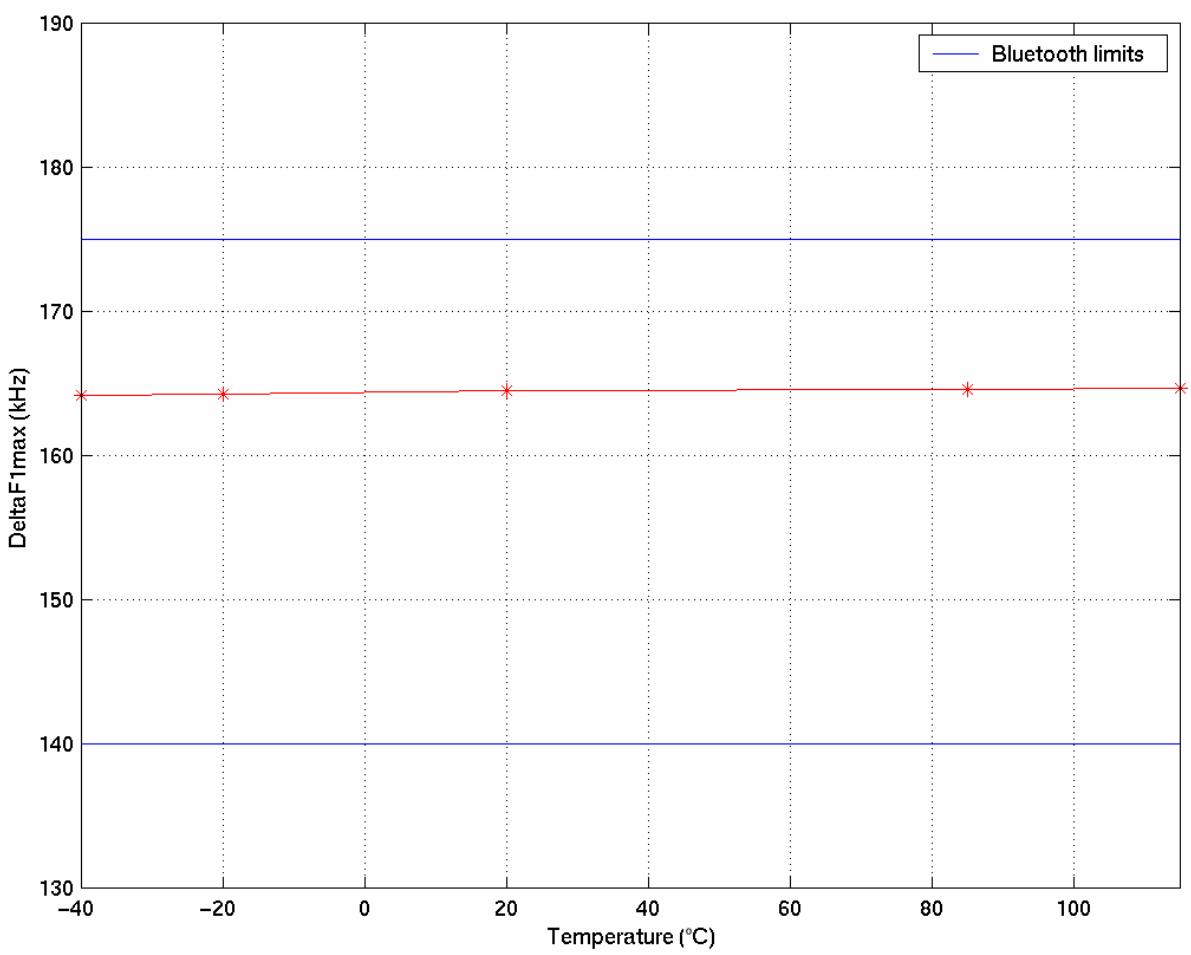


Figure 10.8: Maximum Modulation vs. Temperature

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63.

Average modulation depth over at least 1000 bits must be between 140 and 175kHz

BlueCore2-ROM average modulation depth over approximately 2500bits = 165kHz

Output power at maximum

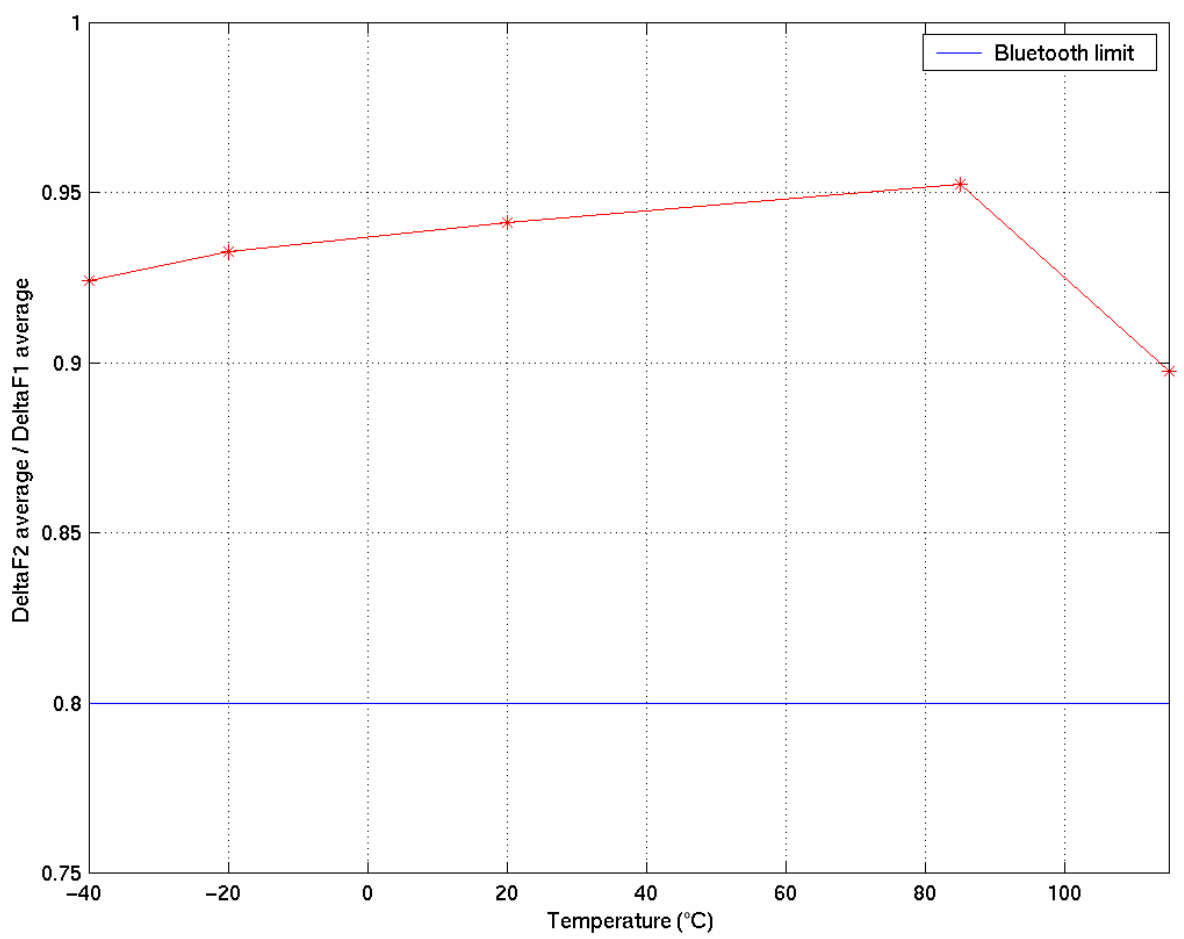


Figure 10.9: Ratio of Minimum to Maximum Modulation vs. Temperature

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63.

Output power at maximum

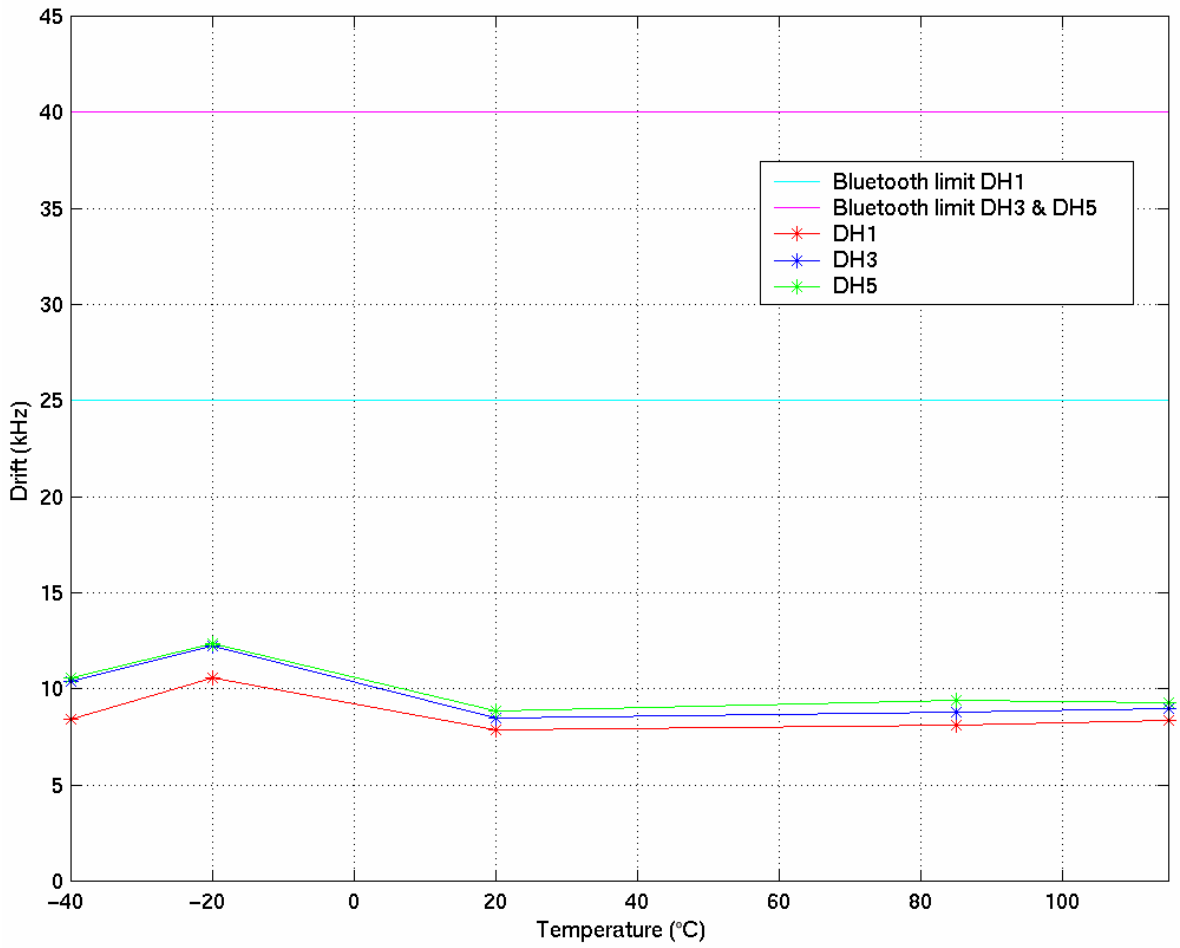


Figure 10.10: Carrier Frequency Drift vs. Temperature

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63.

Output power at maximum

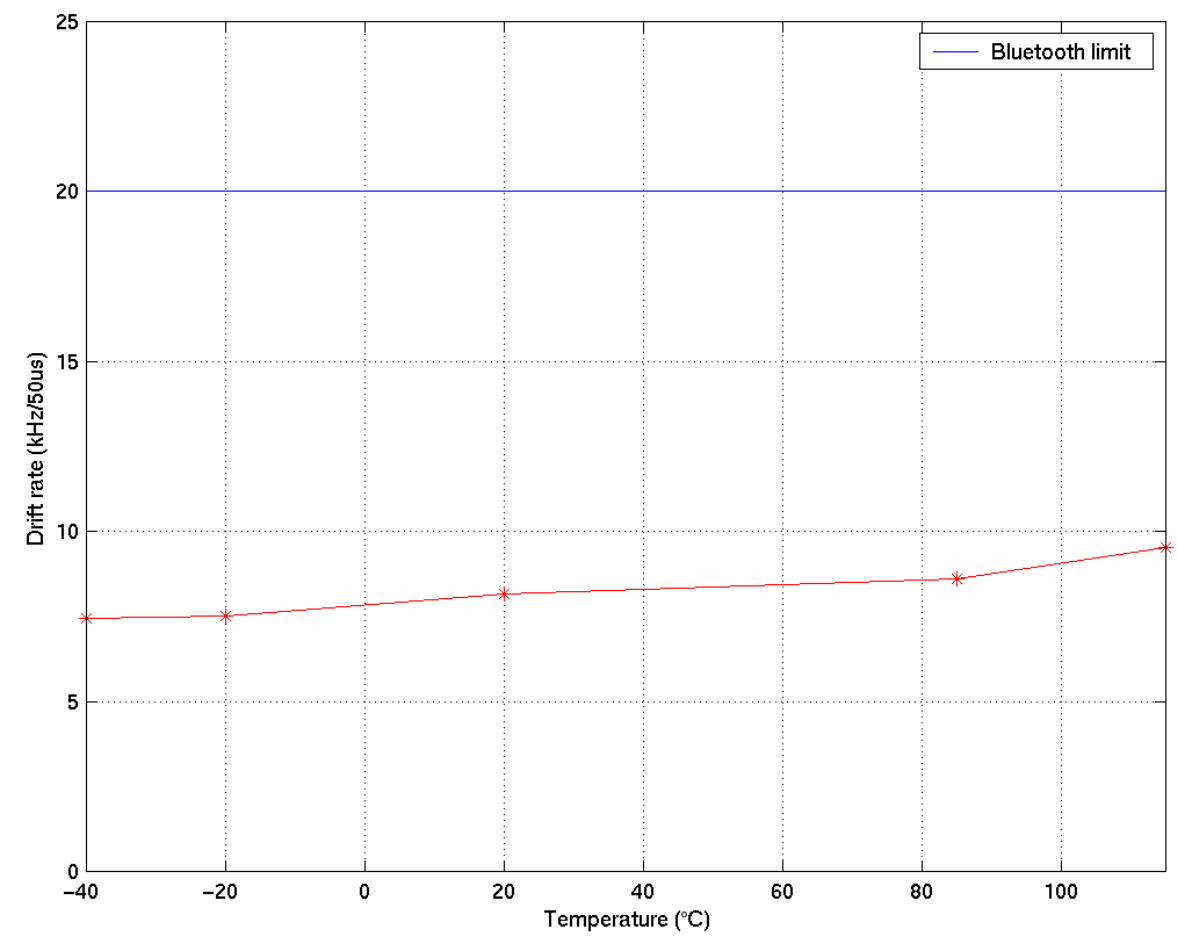


Figure 10.11: Carrier Drift Rate vs. Temperature

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63.

Output power at maximum

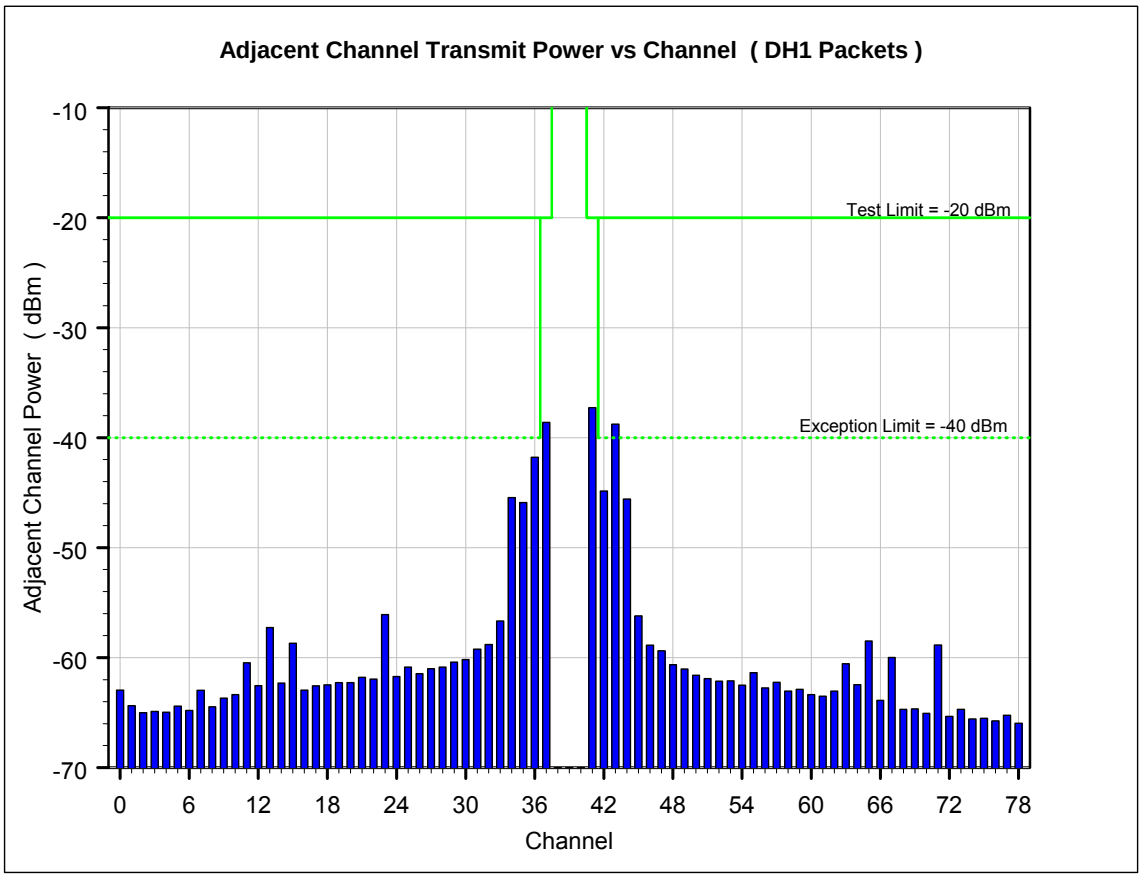


Figure 10.12: Adjacent Channel Power vs. Channel @ -40°C

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63.

Output power at maximum

Up to three exceptions are allowed

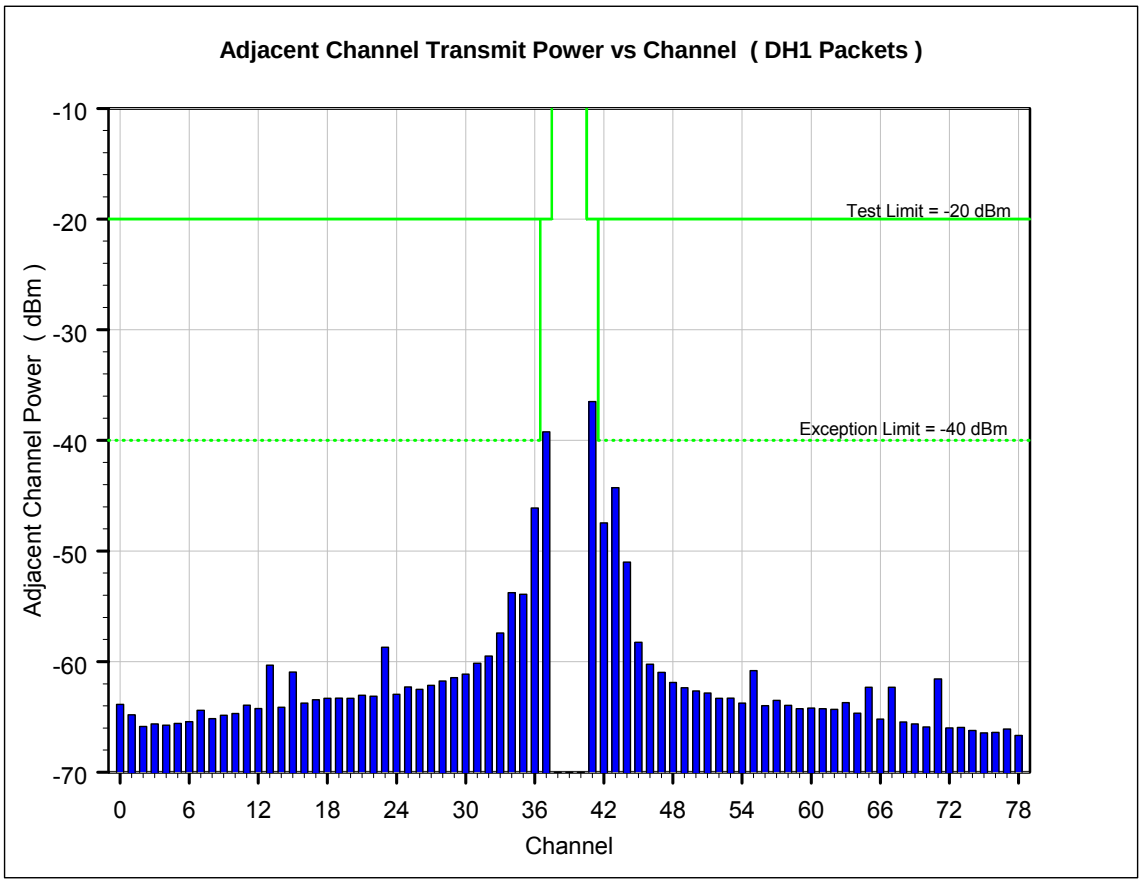


Figure 10.13: Adjacent Channel Power vs. Channel @ +20°C

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63.

Output power at maximum

Up to three exceptions are allowed

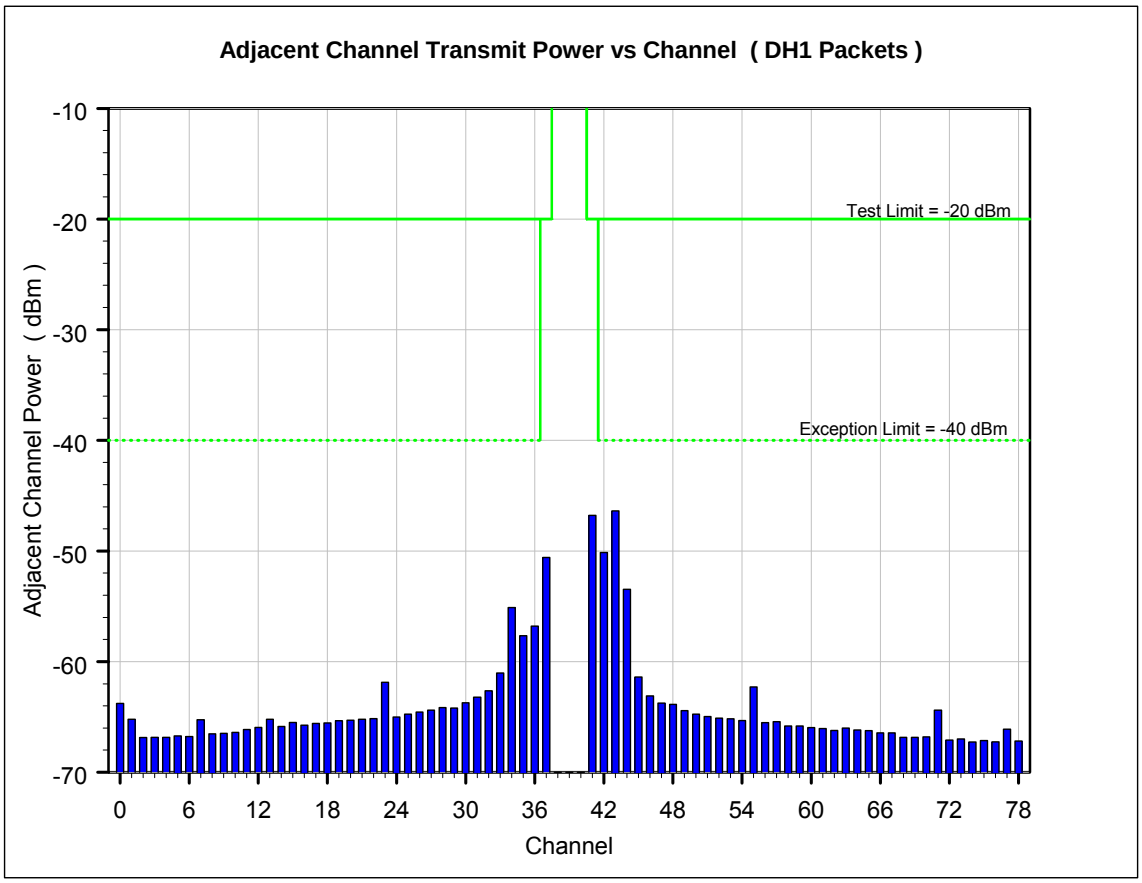


Figure 10.14: Adjacent Channel Power vs. Channel @ +105°C

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63.

Output power at maximum

Up to three exceptions are allowed

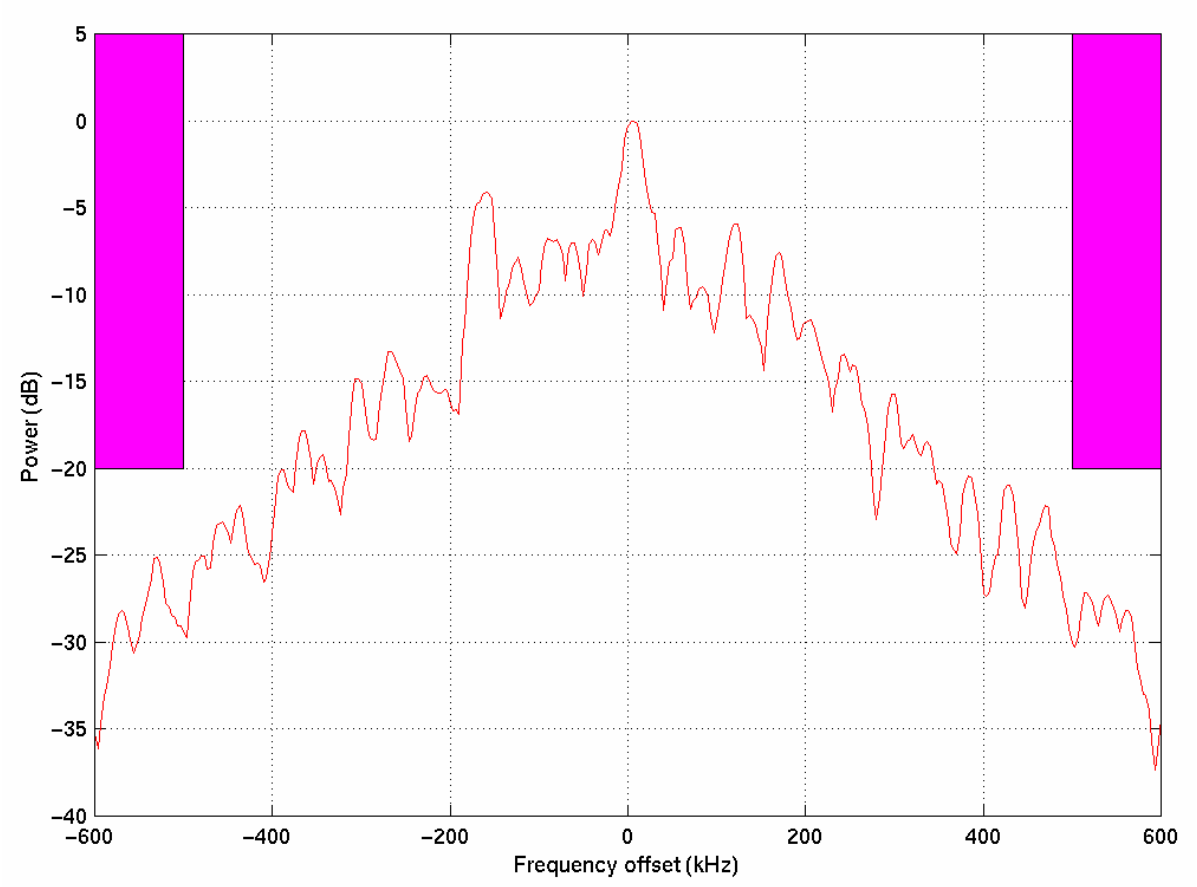


Figure 10.15: Narrowband Transmit Spectrum

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63.

Measurement resolution bandwidth = 10kHz

Temperature: 20°C

Output power at maximum

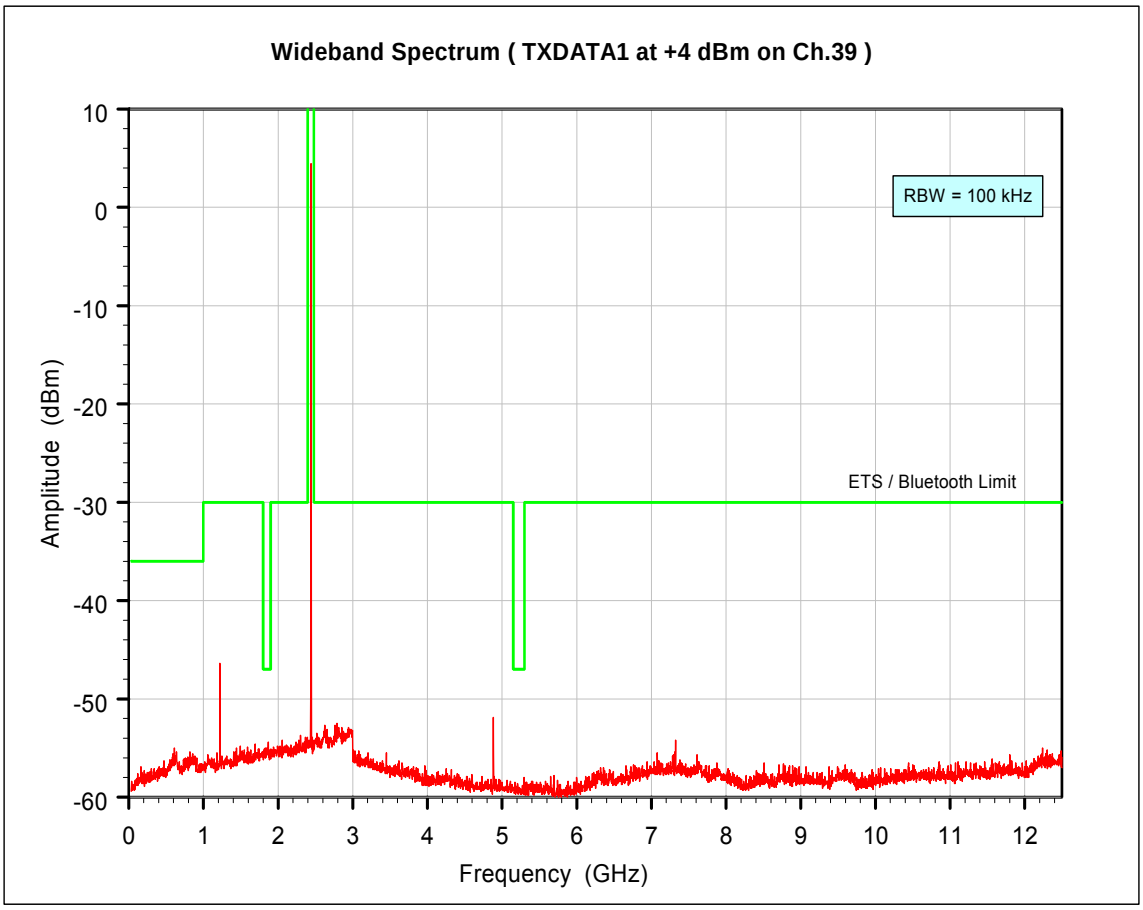


Figure 10.16: Wideband Spectrum (TXDATA1 @ +4 dBm on Channel 39)

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63.

Measurement performed without filter fitted.

Temperature: 20°C

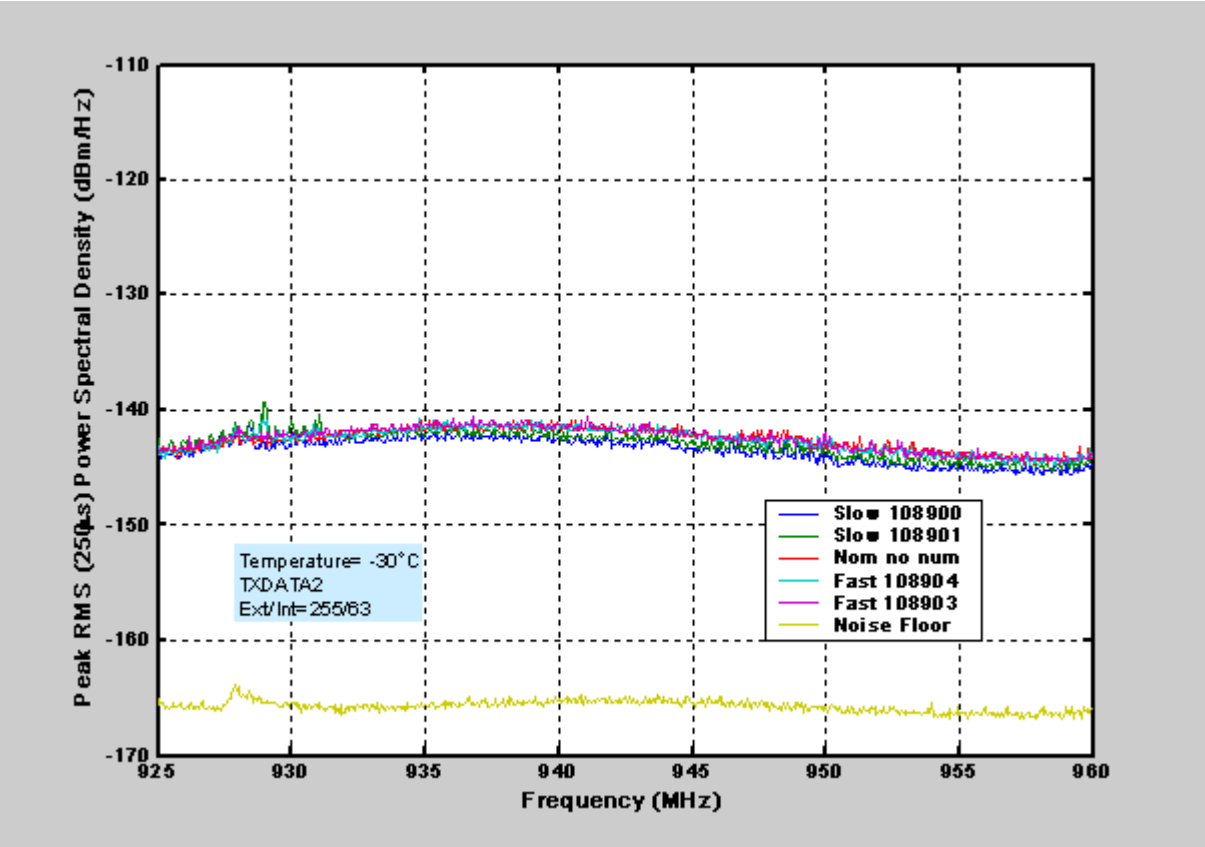


Figure 10.17: Emissions in 925-960MHz GSM Downlink Band at -30°C

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

DH1 packets, frequency hopping

RBW=200kHz

Output power at maximum

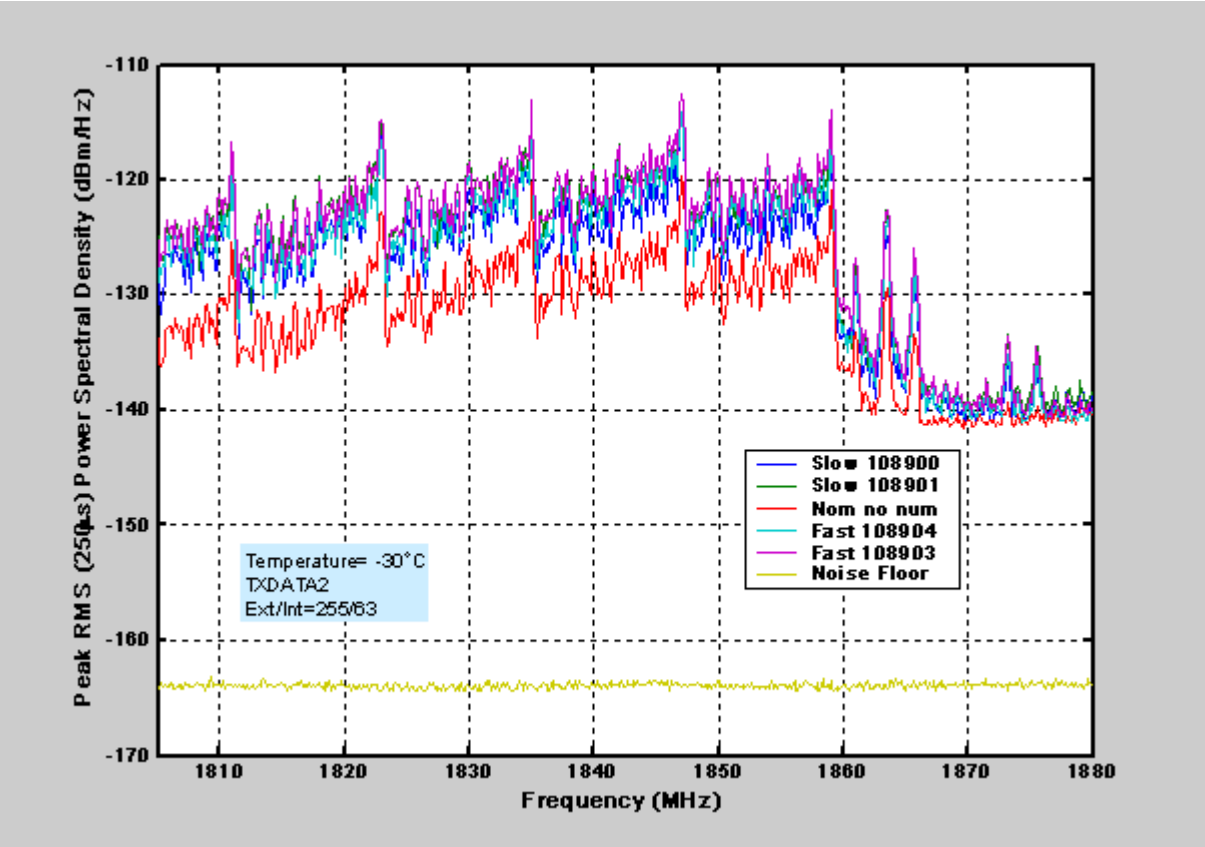


Figure 10.18: Emissions in 1805-1880MHz GSM Downlink Band at -30°C

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

DH1 packets, frequency hopping

RBW=200kHz

Output power at maximum

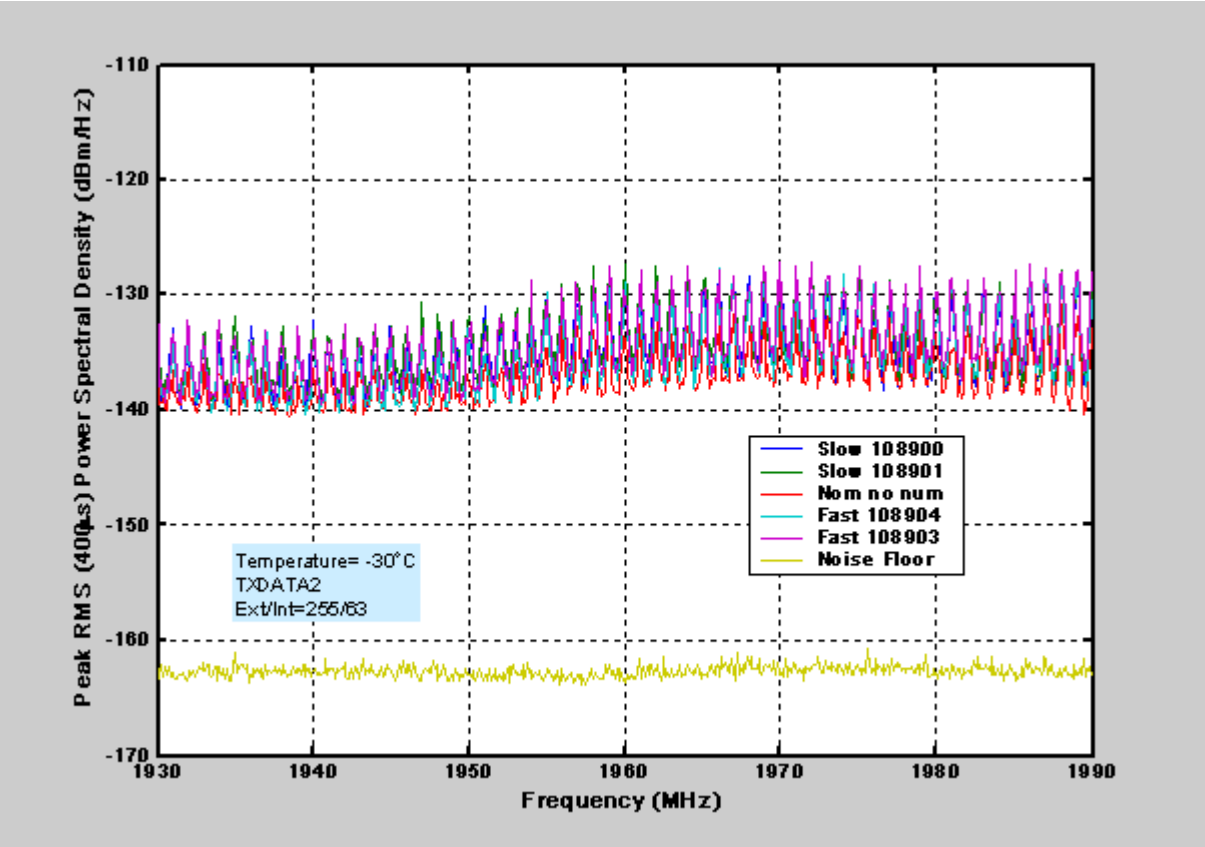


Figure 10.19: Emissions in 1930-1990MHz GSM Downlink Band at -30°C

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

DH1 packets, frequency hopping

RBW 30kHz

Output power at maximum

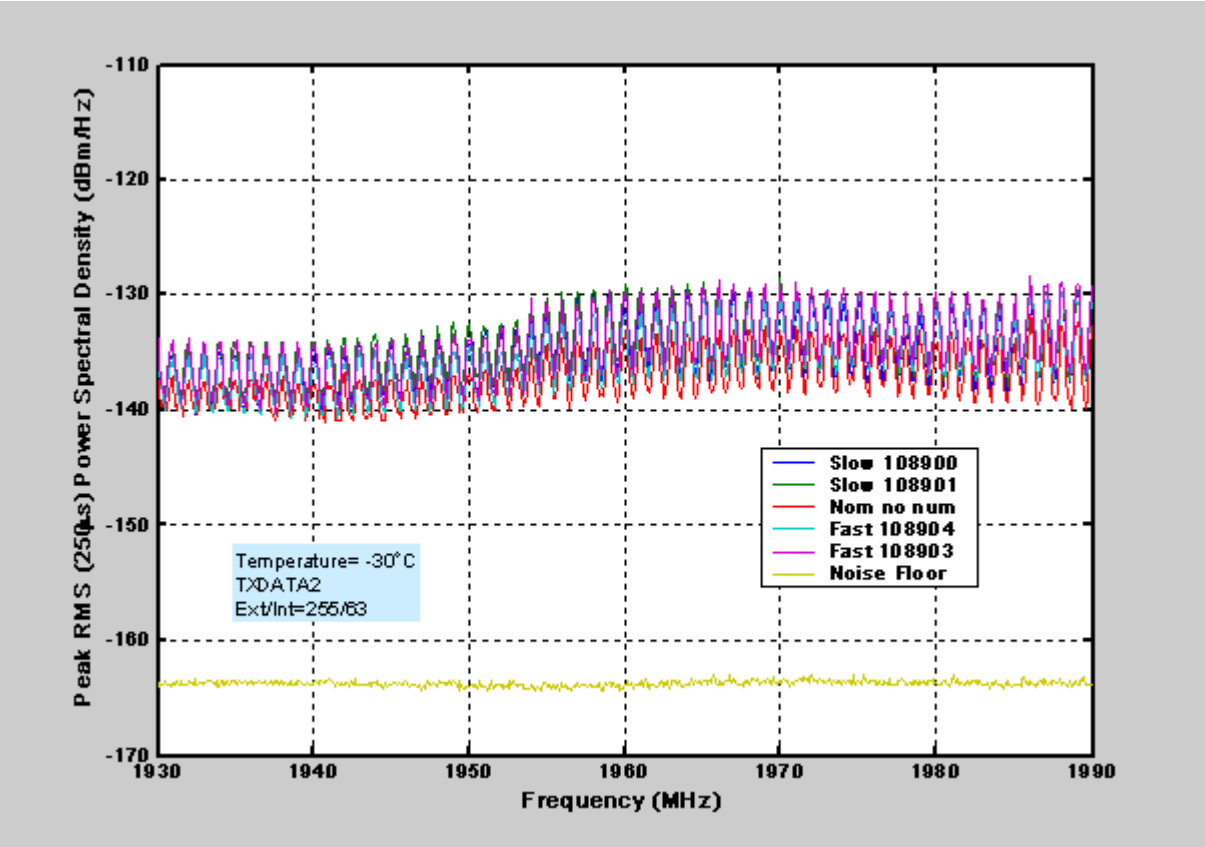


Figure 10.20: Emissions in 1930-1990MHz GSM Downlink Band at -30°C

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

DH1 packets, frequency hopping

RBW 200kHz

Output power at maximum

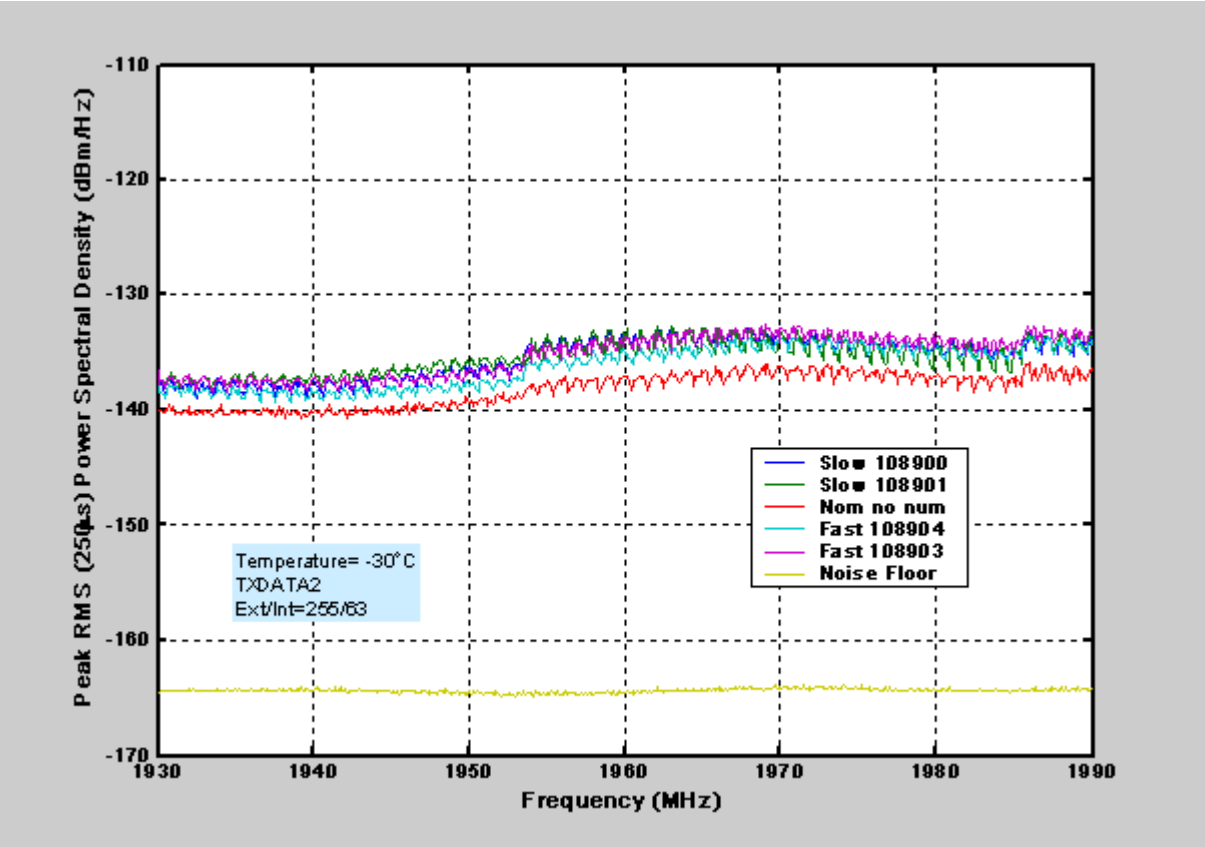


Figure 10.21: Emissions in 1930-1990MHz GSM Downlink Band at -30°C

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

DH1 packets, frequency hopping

RBW 1.2MHz

Output power at maximum

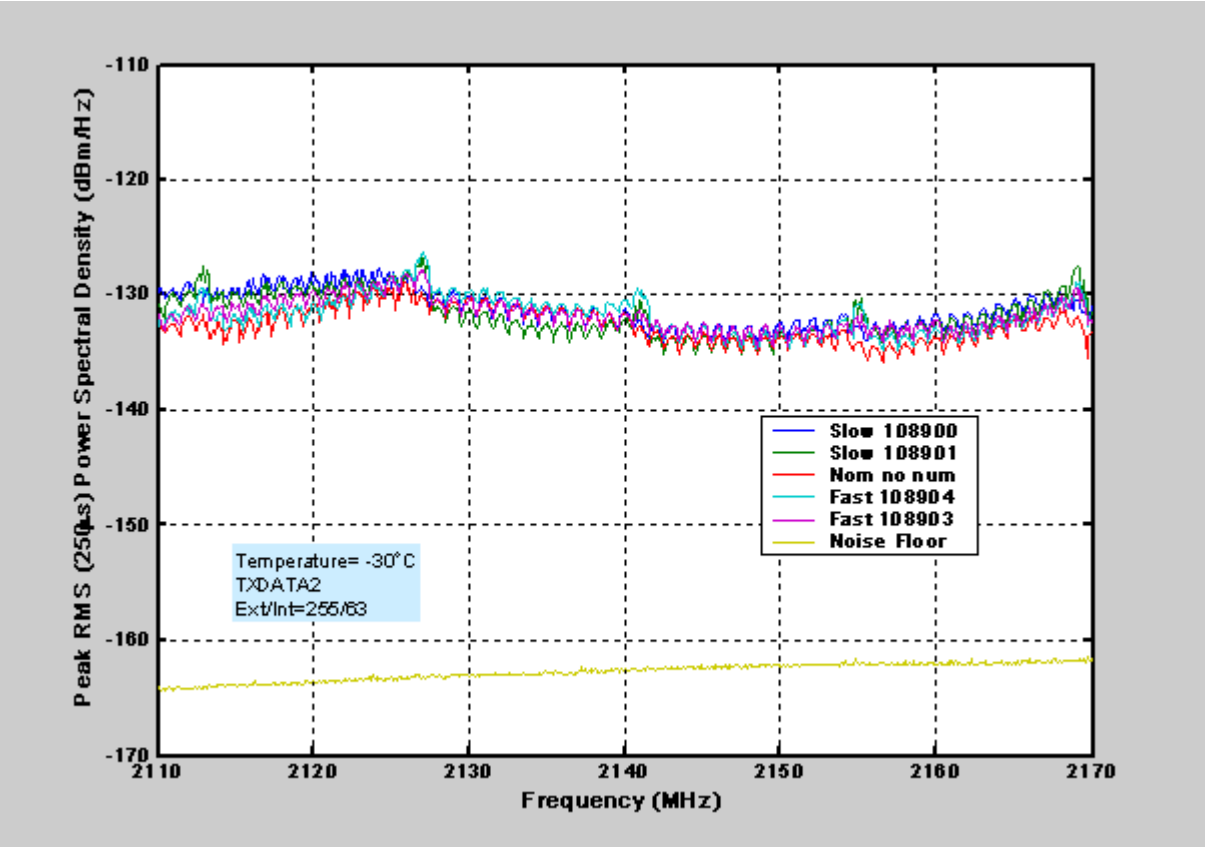


Figure 10.22: Emissions in 2110-2170MHz W-CDMA Downlink Band at -30°C

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

DH1 packets, frequency hopping

RBW 1.2MHz

Output power at maximum

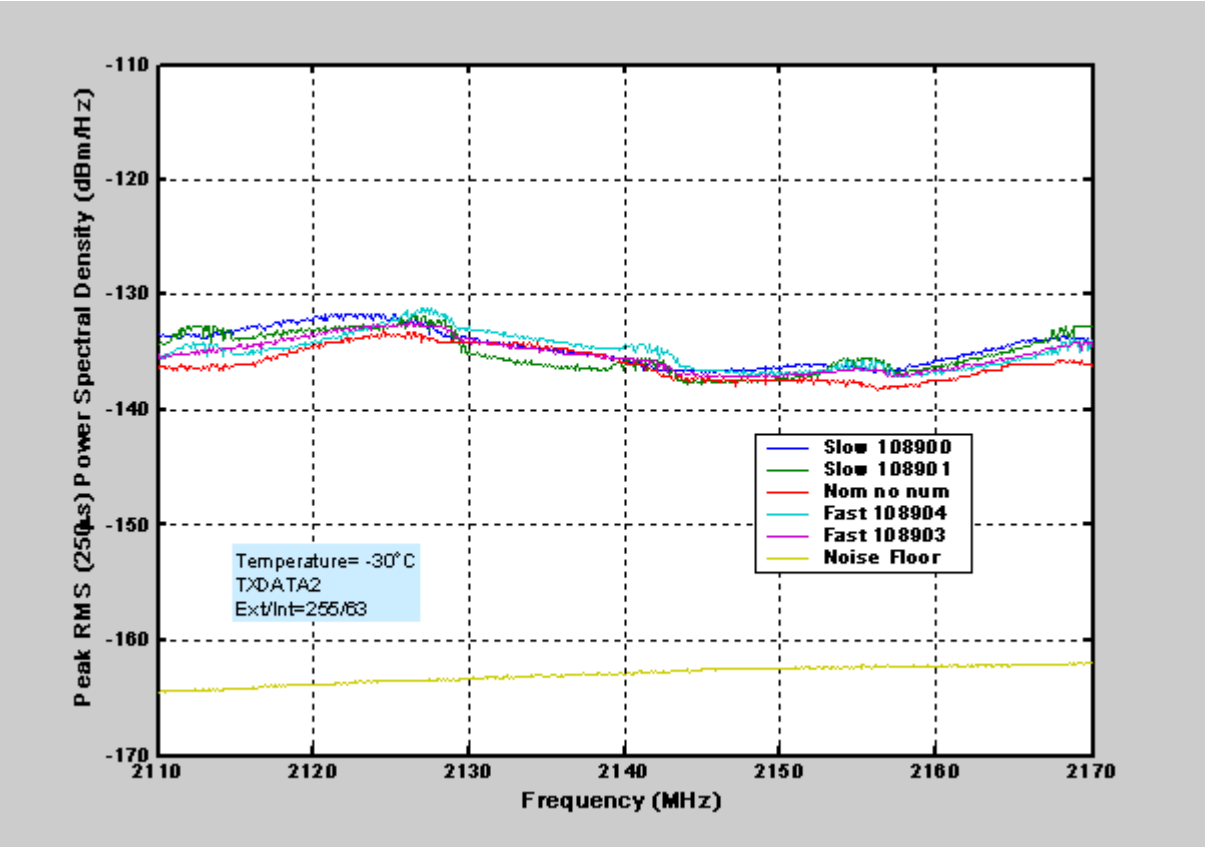


Figure 10.23: Emissions in 2110-2170MHz W-CDMA Downlink Band at -30°C

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

DH1 packets, frequency hopping

RBW 5MHz

Output power at maximum

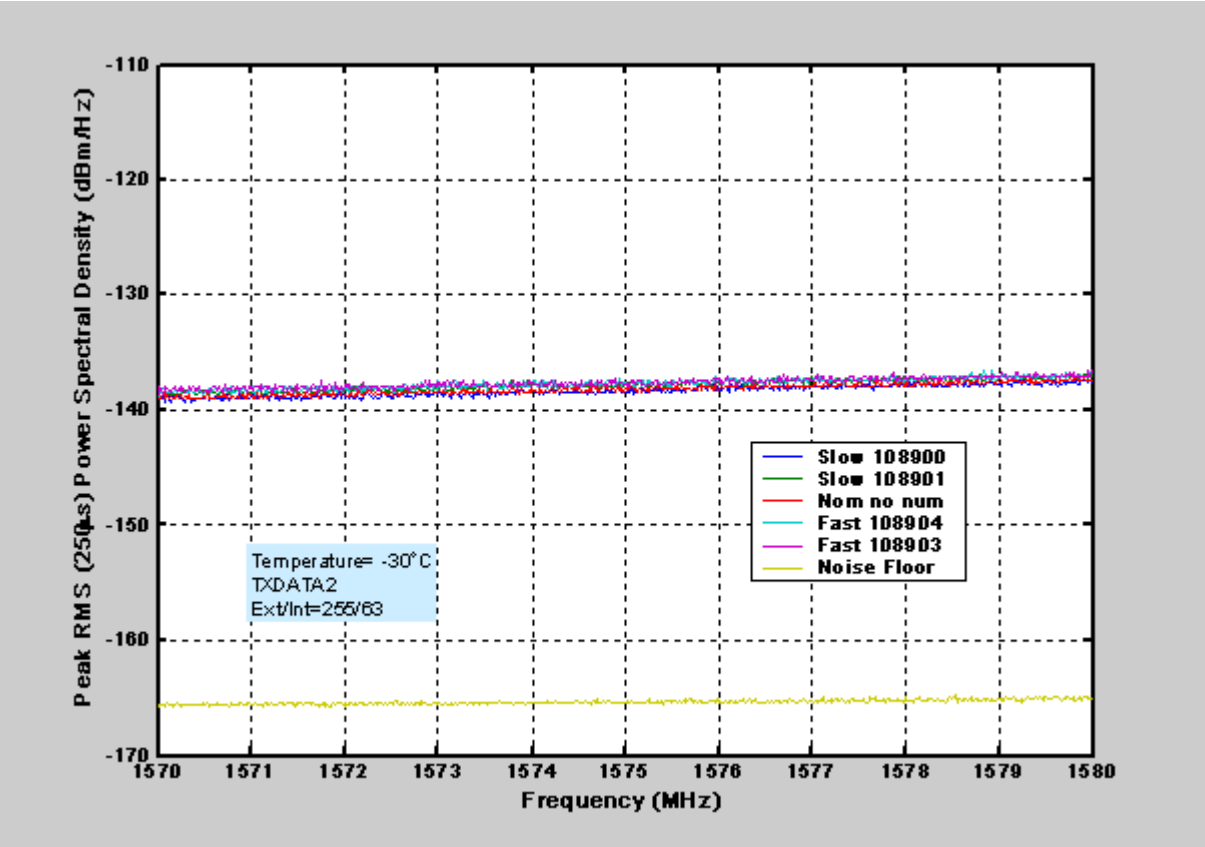


Figure 10.24: Emissions in Vicinity of GPS Downlink at -30°C

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

DH1 packets, frequency hopping

RBW 1MHz

Output power at maximum

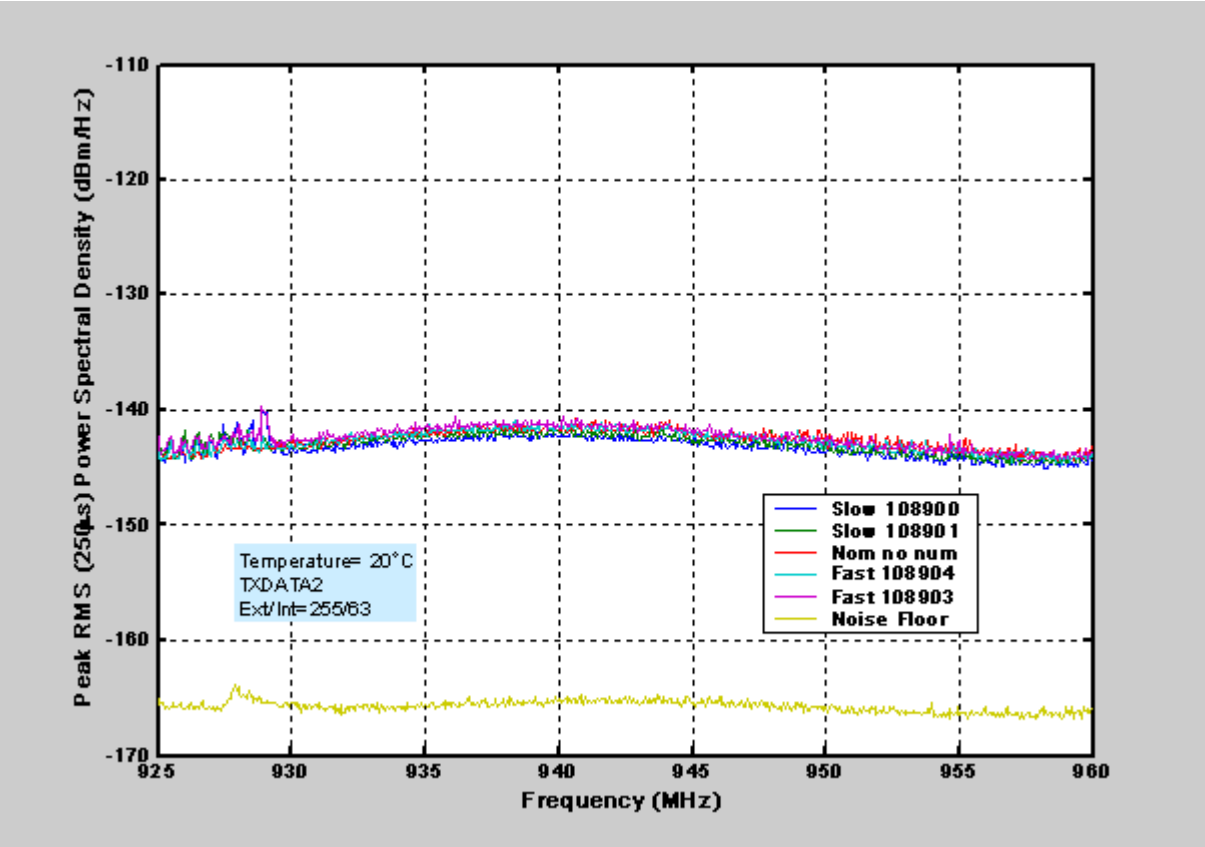


Figure 10.25: Emissions in 925-960MHz GSM Downlink Band at 20°C

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

DH1 packets, frequency hopping

RBW 200kHz

Output power at maximum

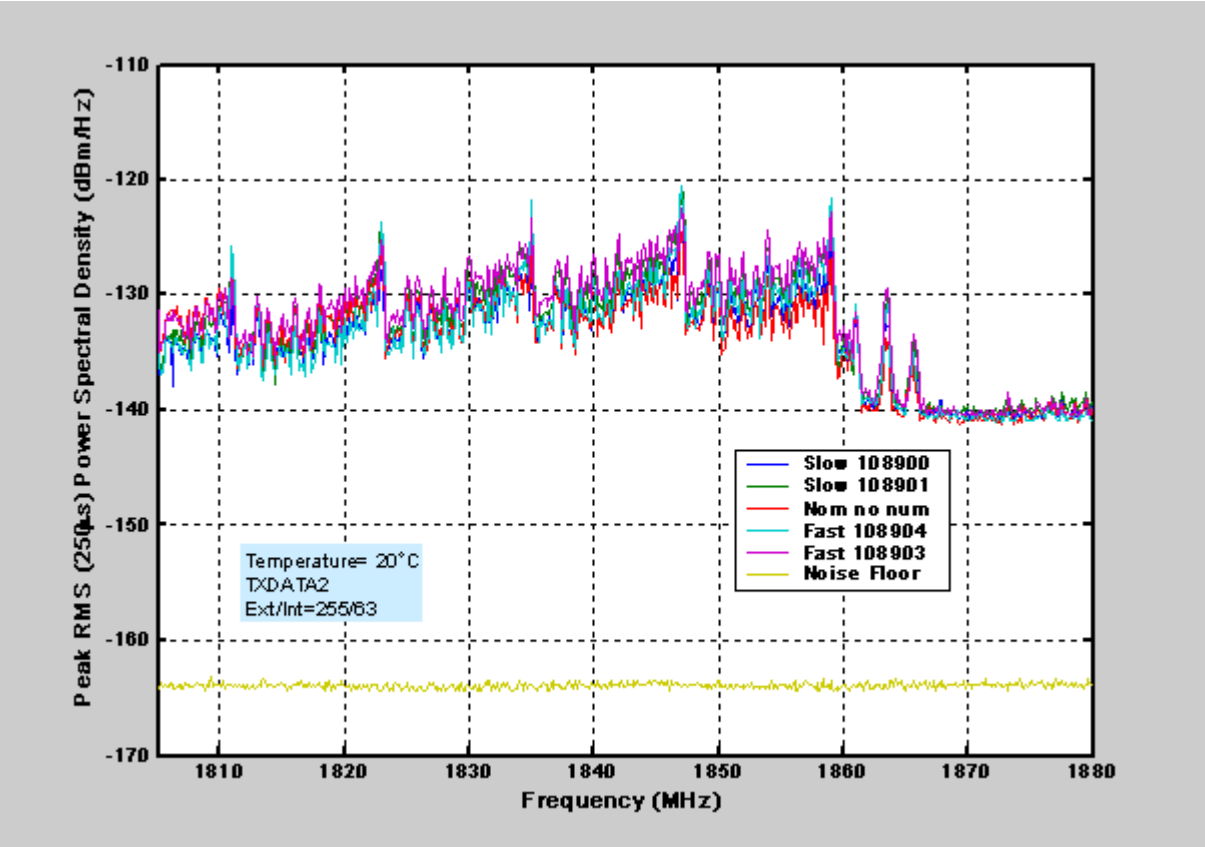


Figure 10.26: Emissions in 1805-1880MHz GSM Downlink Band at 20°C

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

DH1 packets, frequency hopping

RBW 200kHz

Output power at maximum

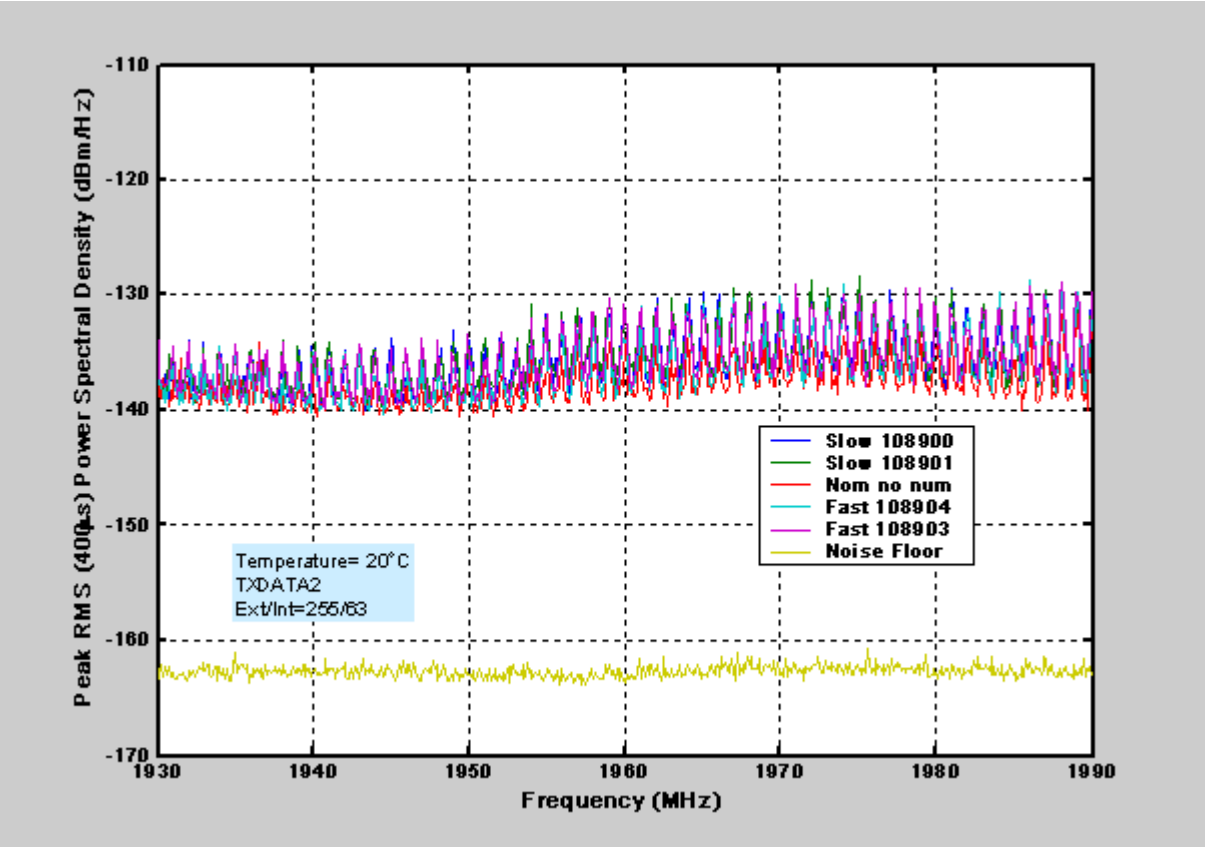


Figure 10.27: Emissions in 1930-1990MHz GSM Downlink Band at 20°C

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

DH1 packets, frequency hopping

RBW 30kHz

Output power at maximum

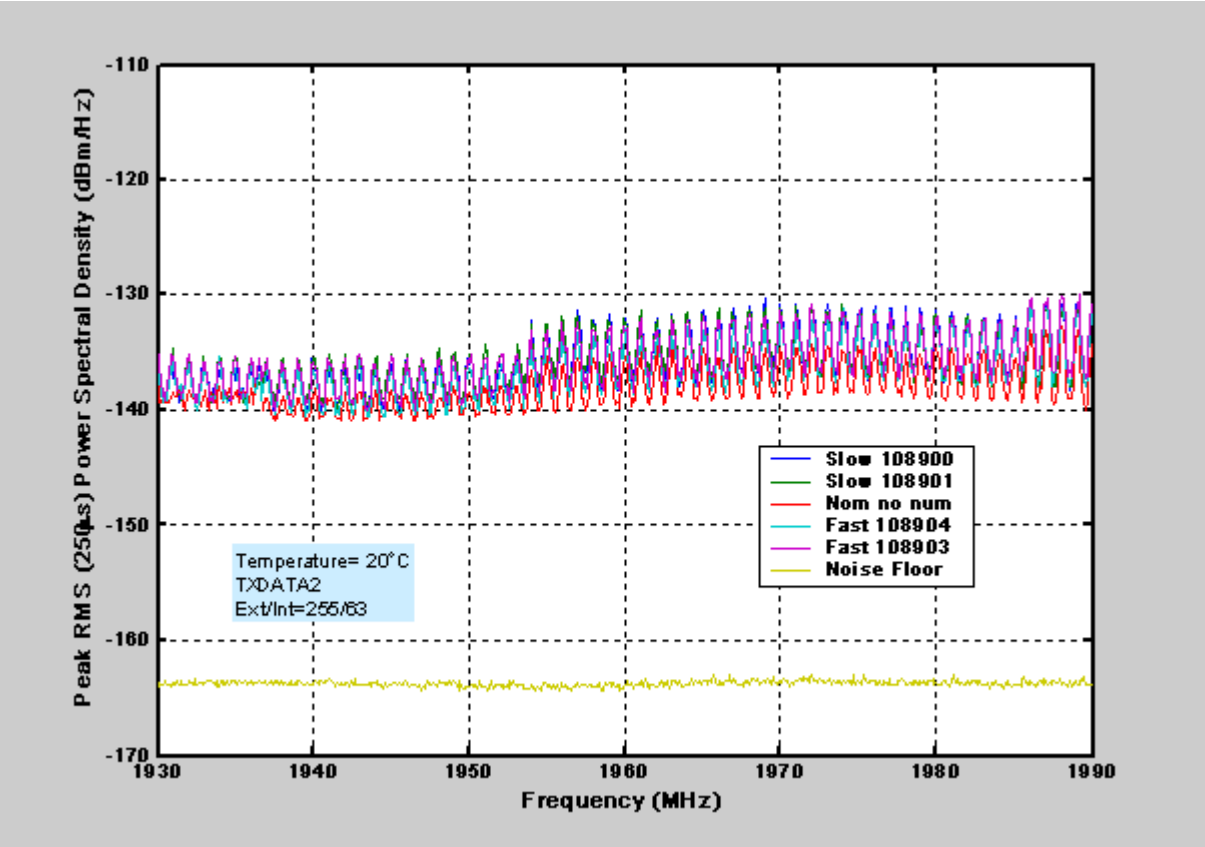


Figure 10.28: Emissions in 1930-1990MHz GSM Downlink Band at 20°C

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

DH1 packets, frequency hopping

RBW 200kHz

Output power at maximum

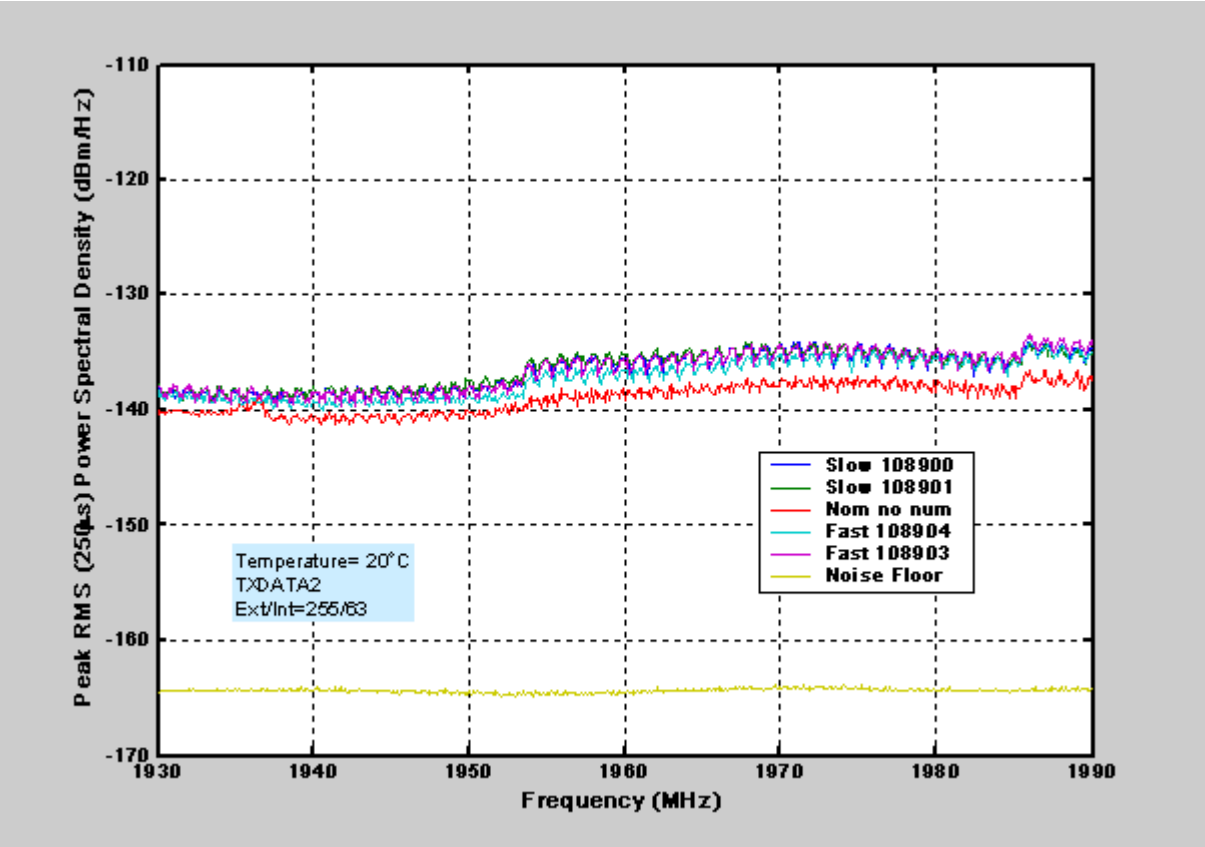


Figure 10.29: Emissions in 1930-1990MHz GSM Downlink Band at 20°C

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

DH1 packets, frequency hopping

RBW 1.2MHz

Output power at maximum

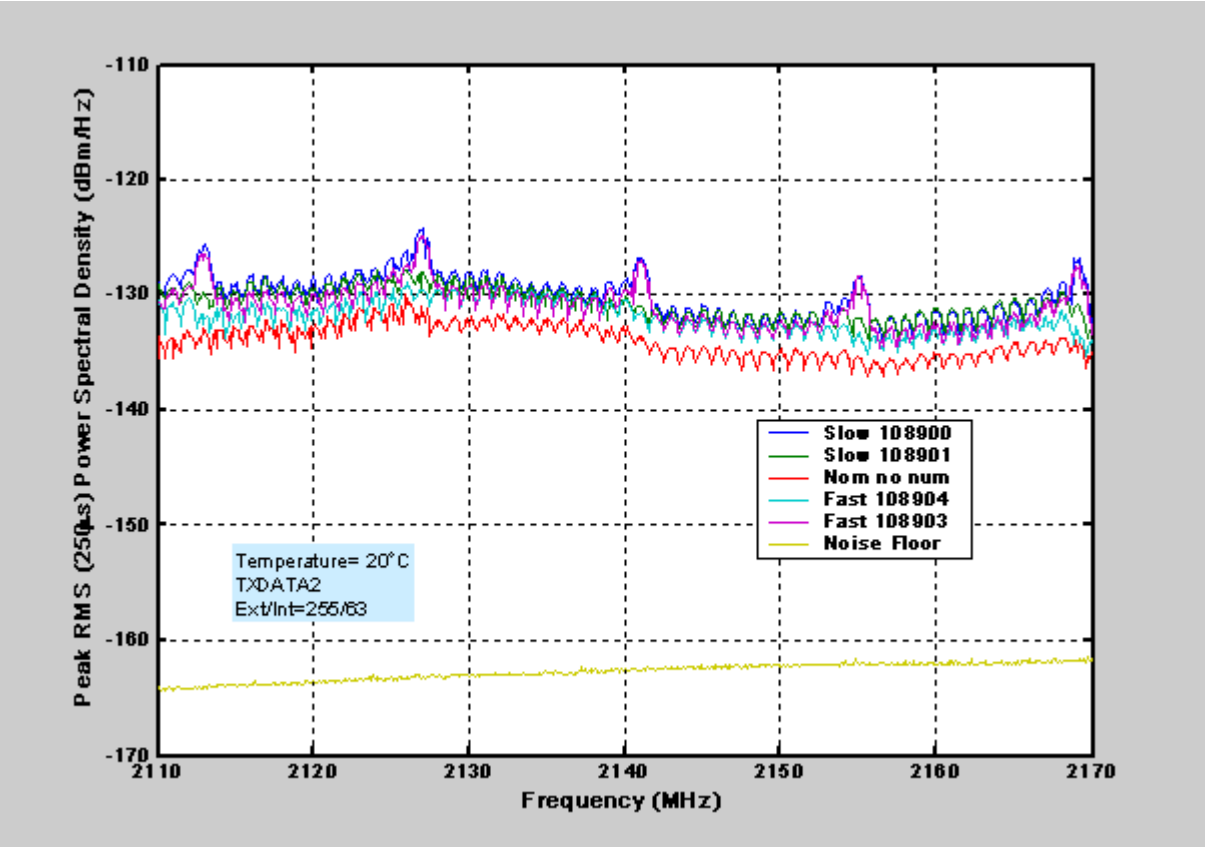


Figure 10.30: Emissions in 2110-2170MHz W-CDMA Downlink Band at 20°C

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

DH1 packets, frequency hopping

RBW 1.2MHz

Output power at maximum

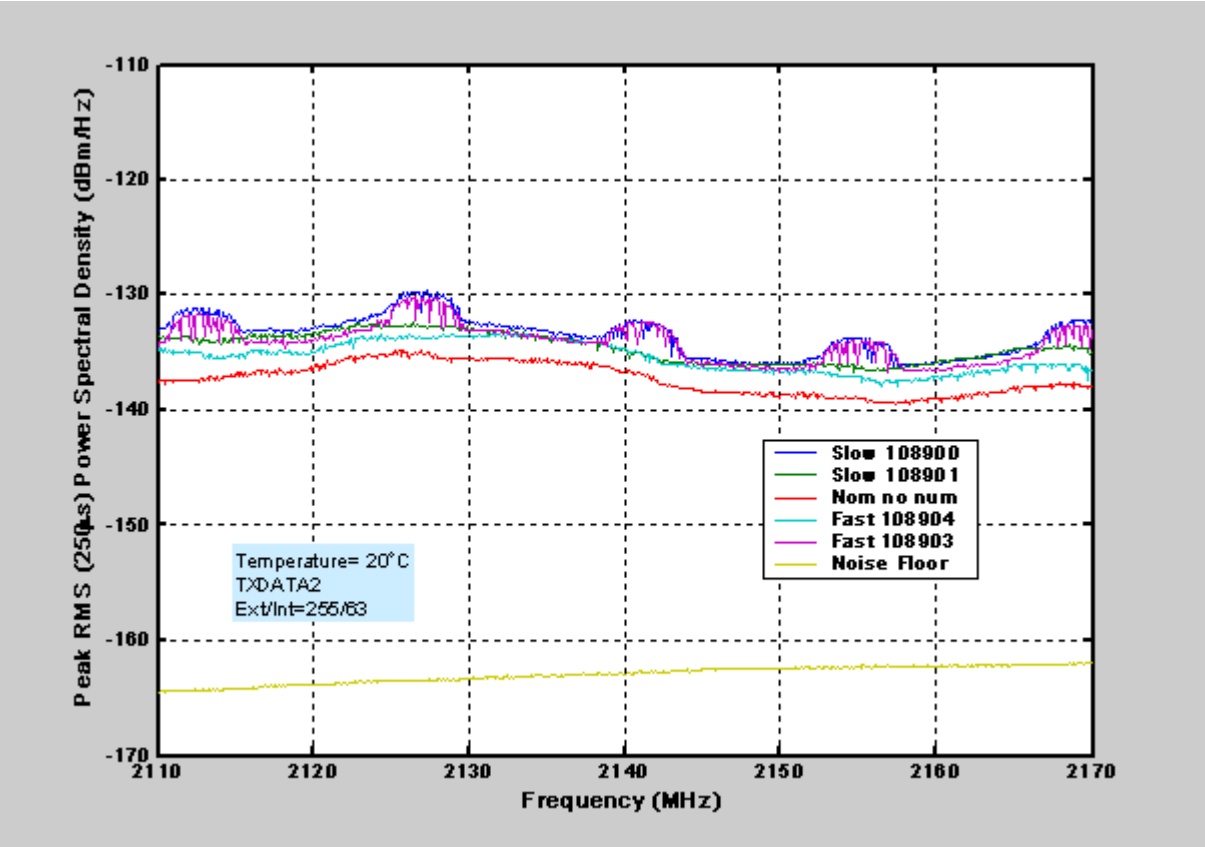


Figure 10.31: Emissions in 2110-2170MHz W-CDMA Downlink Band at 20°C

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

DH1 packets, frequency hopping

RBW 5MHz

Output power at maximum

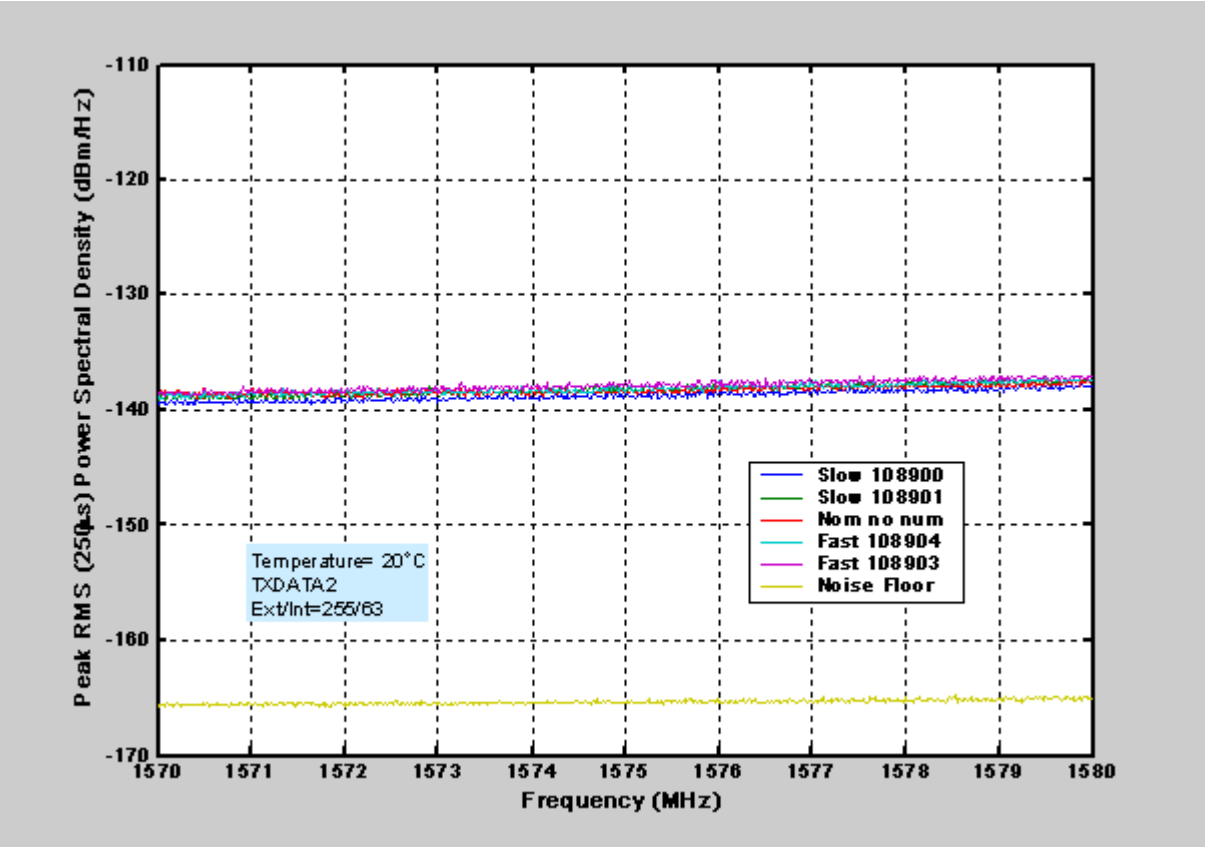


Figure 10.32: Emissions in Vicinity of the GPS Downlink at 20°C

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

DH1 packets, frequency hopping

RBW 1MHz

Output power at maximum

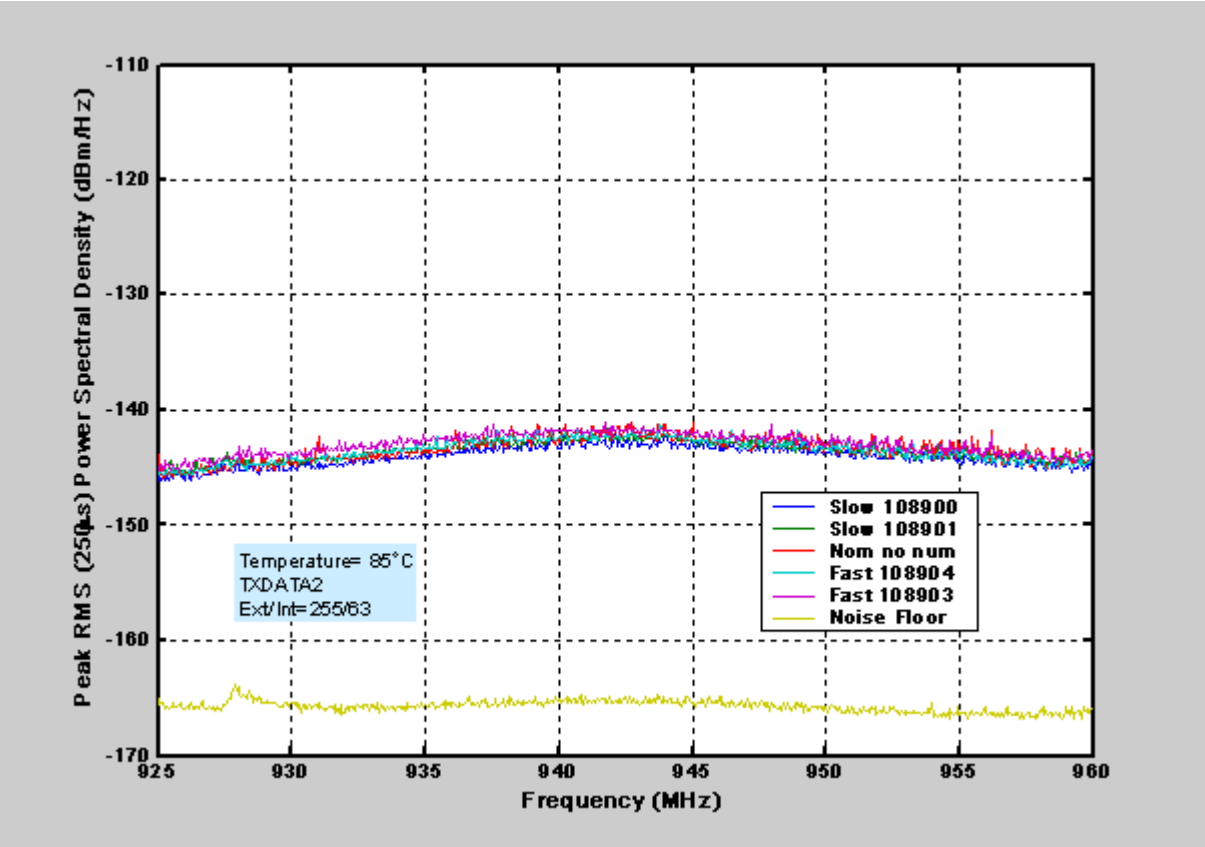


Figure 10.33: Emissions in 925-960MHz GSM Downlink Band at 85°C

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

DH1 packets, frequency hopping

RBW 200kHz

Output power at maximum

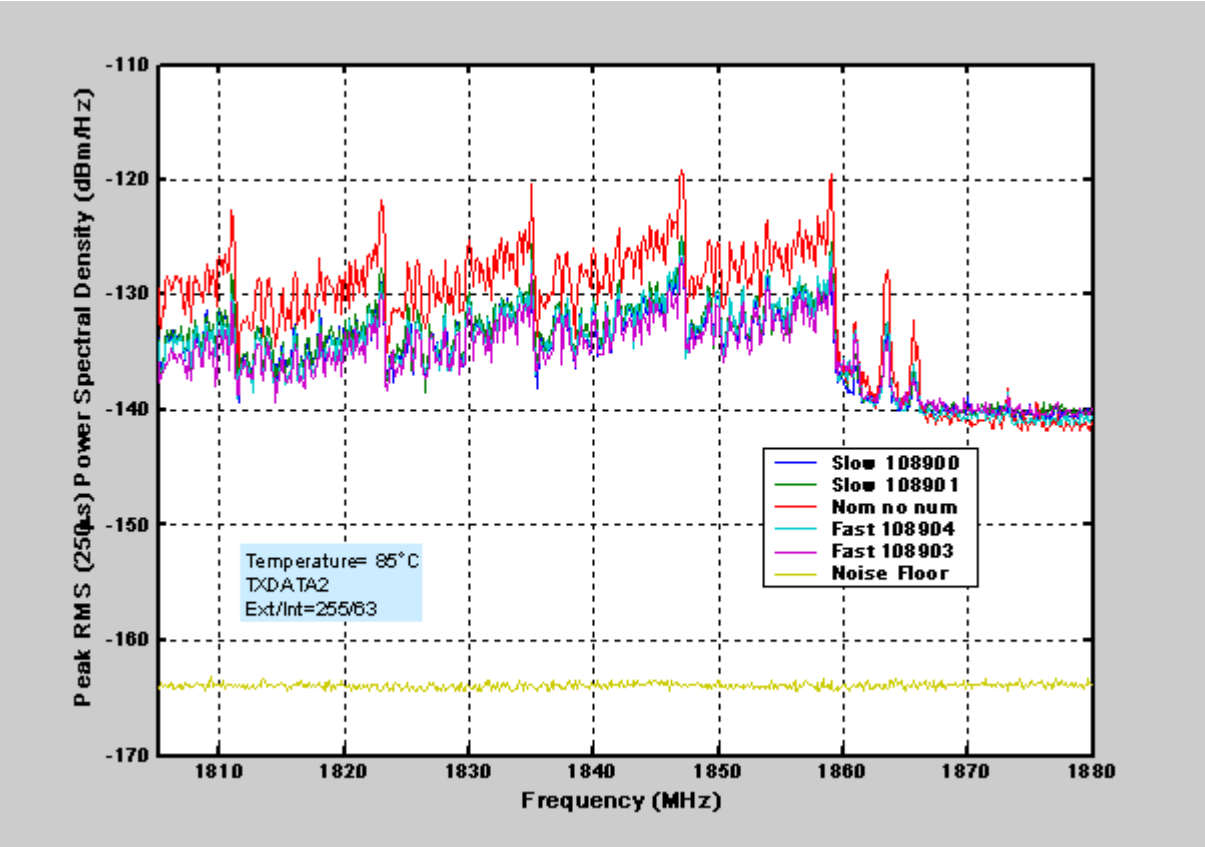


Figure 10.34: Emissions in 1805-1880MHz GSM Downlink Band at 85°C

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

DH1 packets, frequency hopping

RBW 200kHz

Output power at maximum

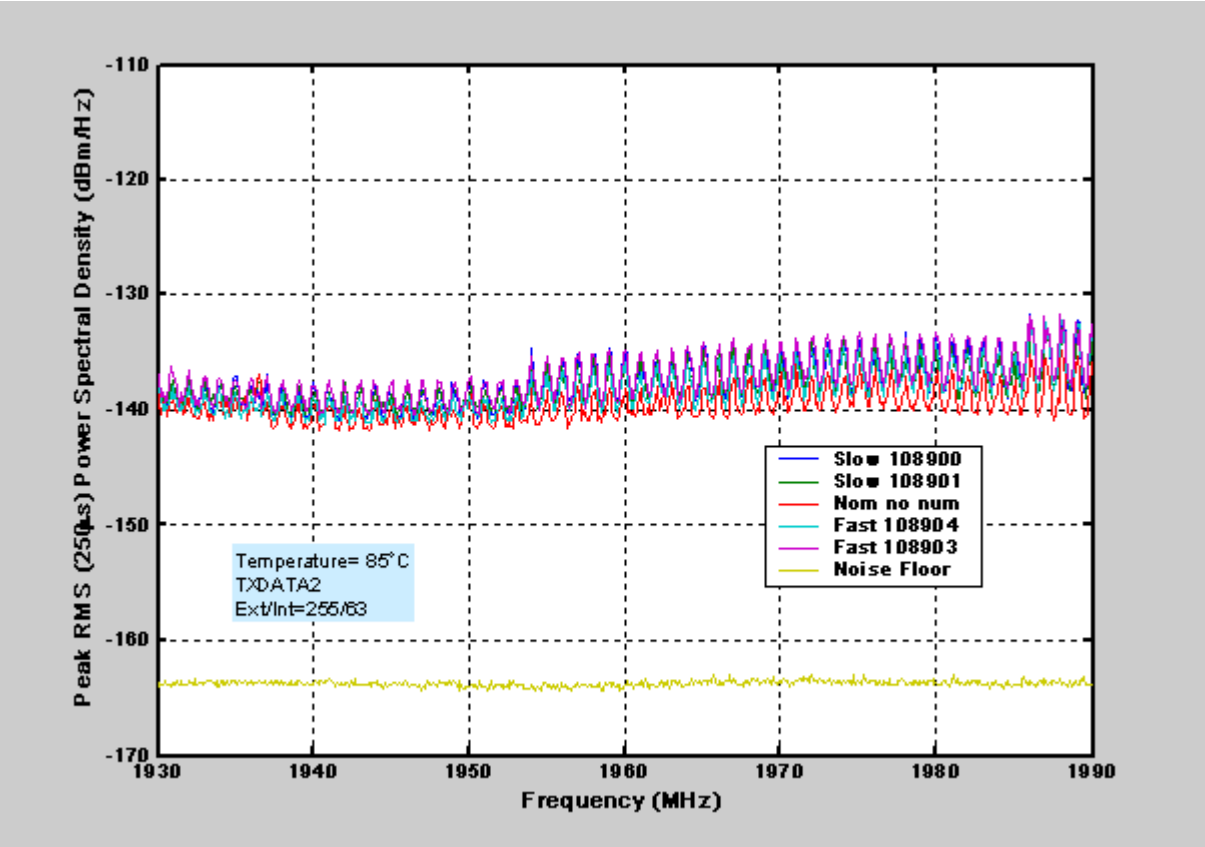


Figure 10.35: Emissions in 1930-1990MHz GSM Downlink Band at 85°C

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

DH1 packets, frequency hopping

RBW 30kHz

Output power at maximum

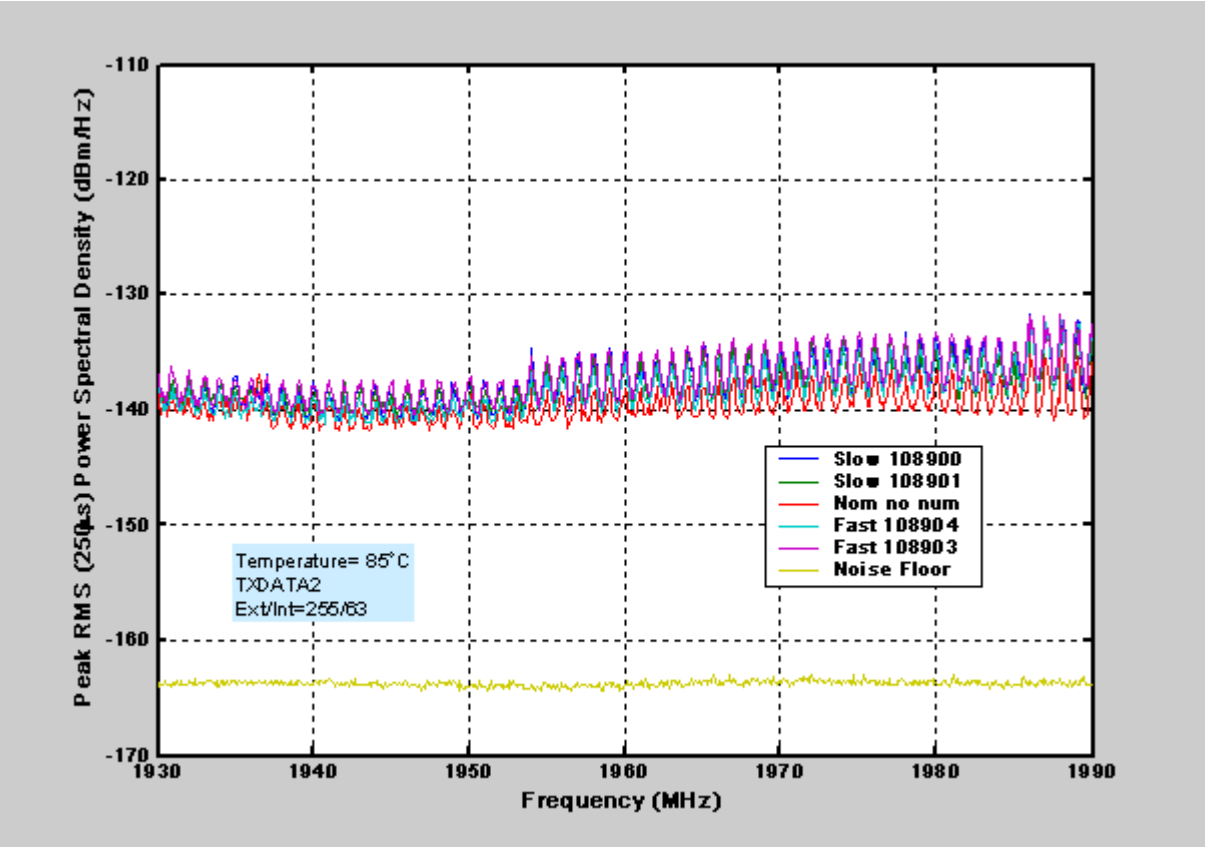


Figure 10.36: Emissions in 1930-1990MHz GSM Downlink Band at 85°C

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

DH1 packets, frequency hopping

RBW 200kHz

Output power at maximum

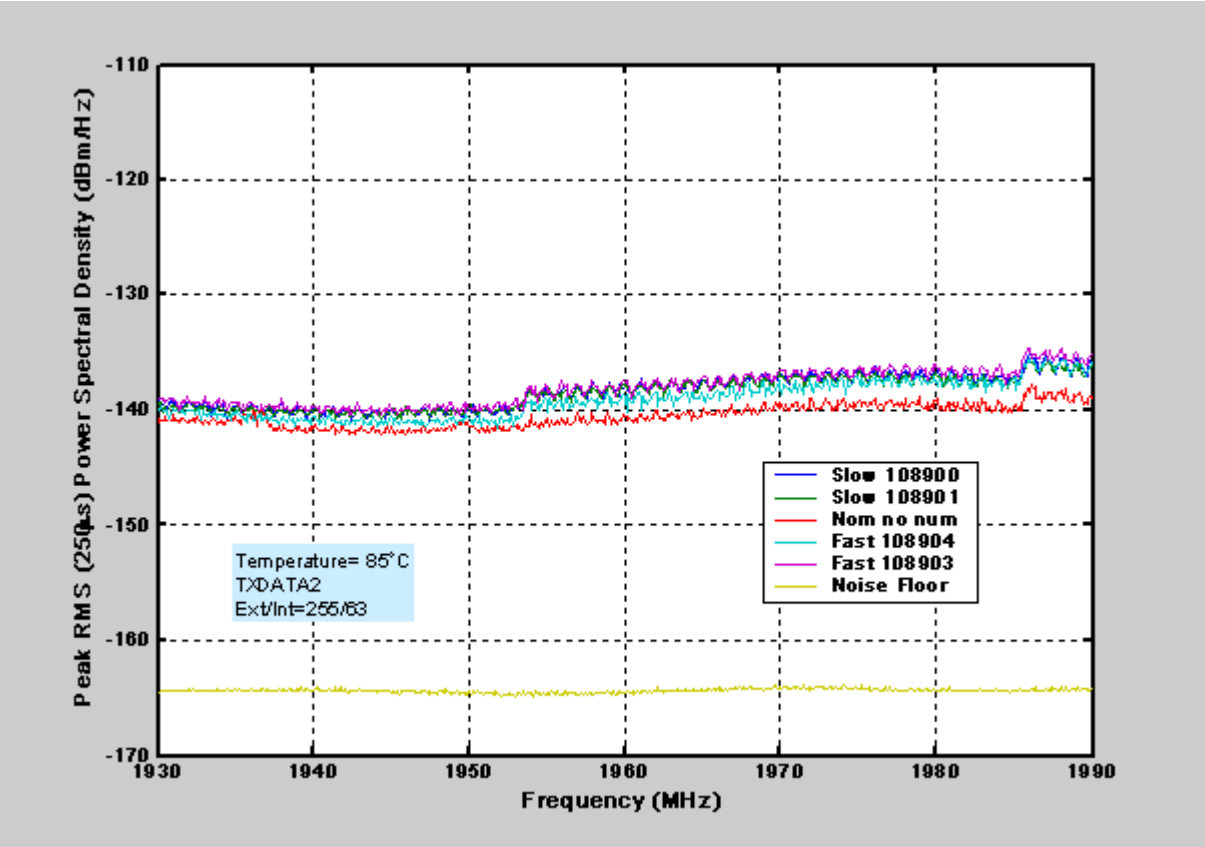


Figure 10.37: Emissions in 1930-1990MHz GSM Downlink Band at 85°C

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

DH1 packets, frequency hopping

RBW 1.2MHz

Output power at maximum

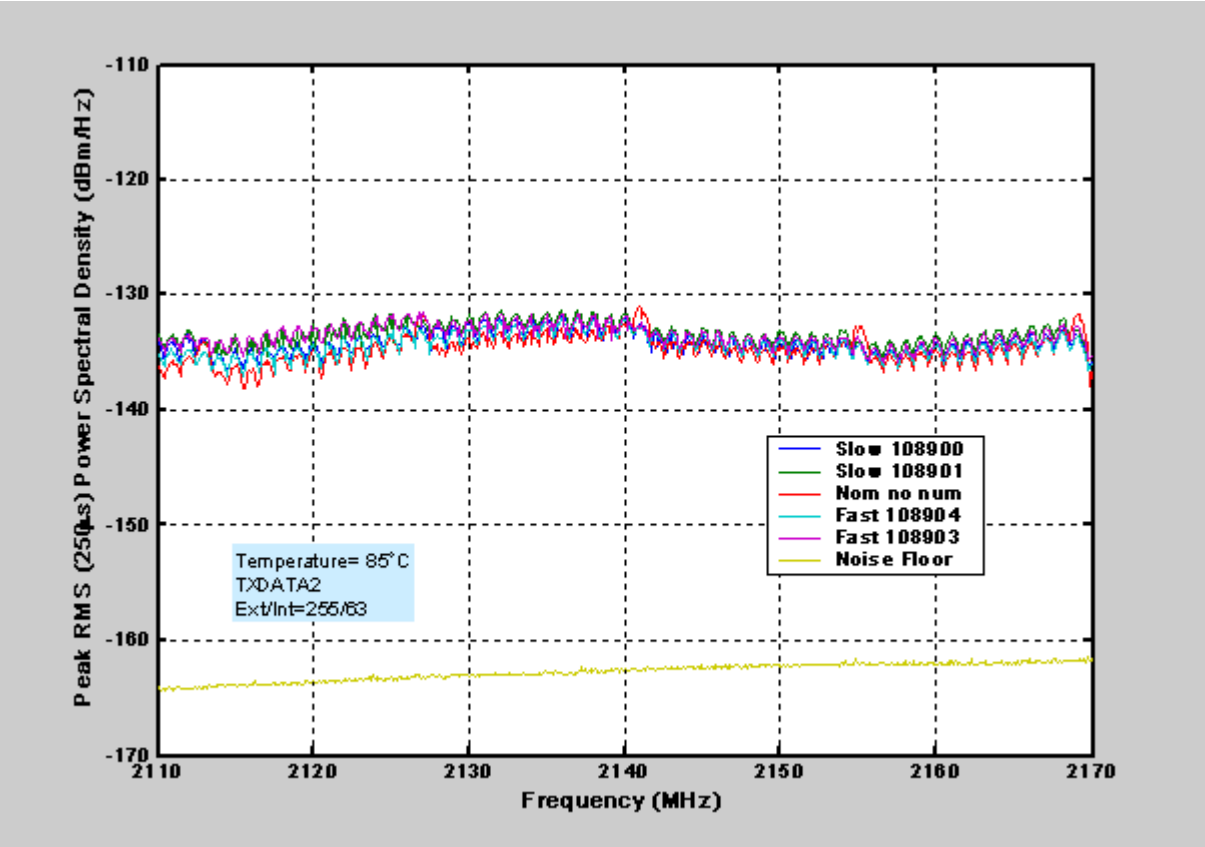


Figure 10.38: Emissions in 2110-2170MHz W-CDMA Downlink Band at 85°C

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

DH1 packets, frequency hopping

RBW 1.2MHz

Output power at maximum

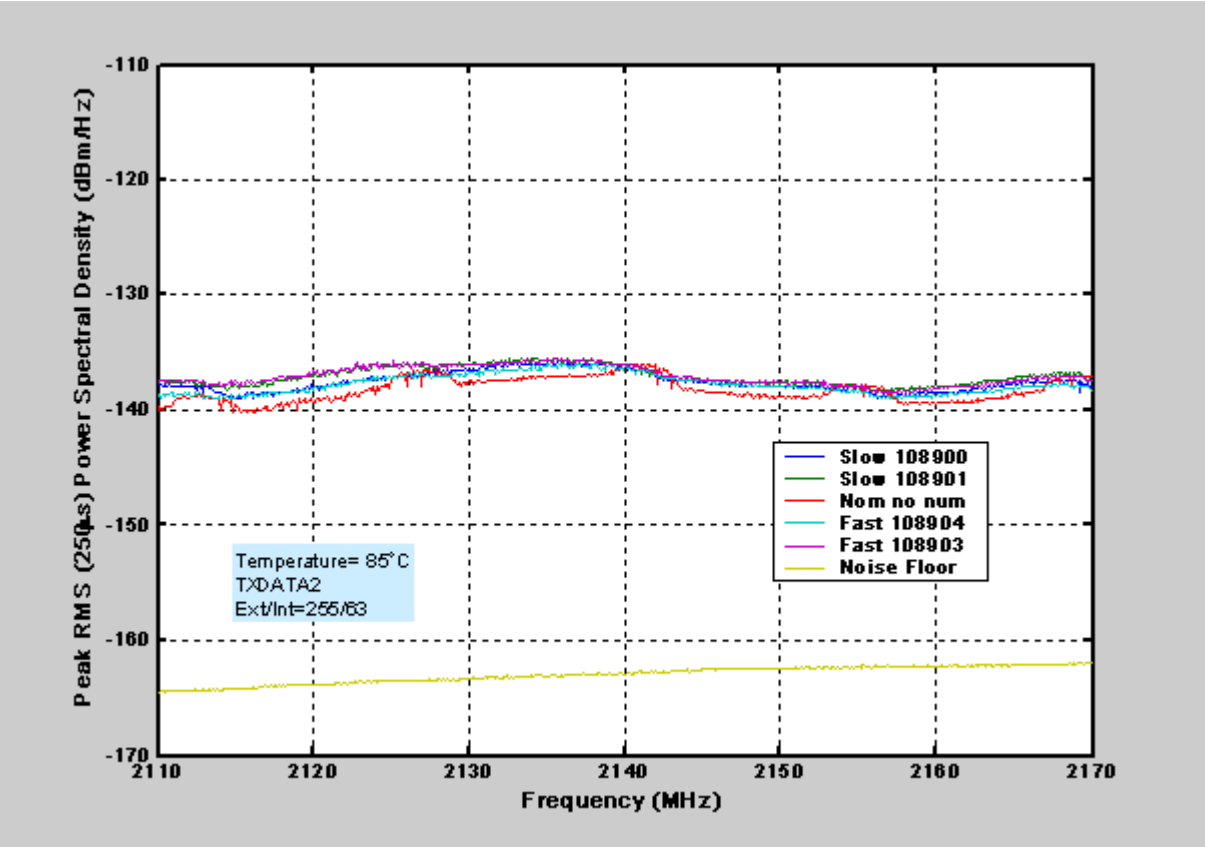


Figure 10.39: Emissions in 2110-2170MHz W-CDMA Downlink Band at 85°C

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

DH1 packets, frequency hopping

RBW 5MHz

Output power at maximum

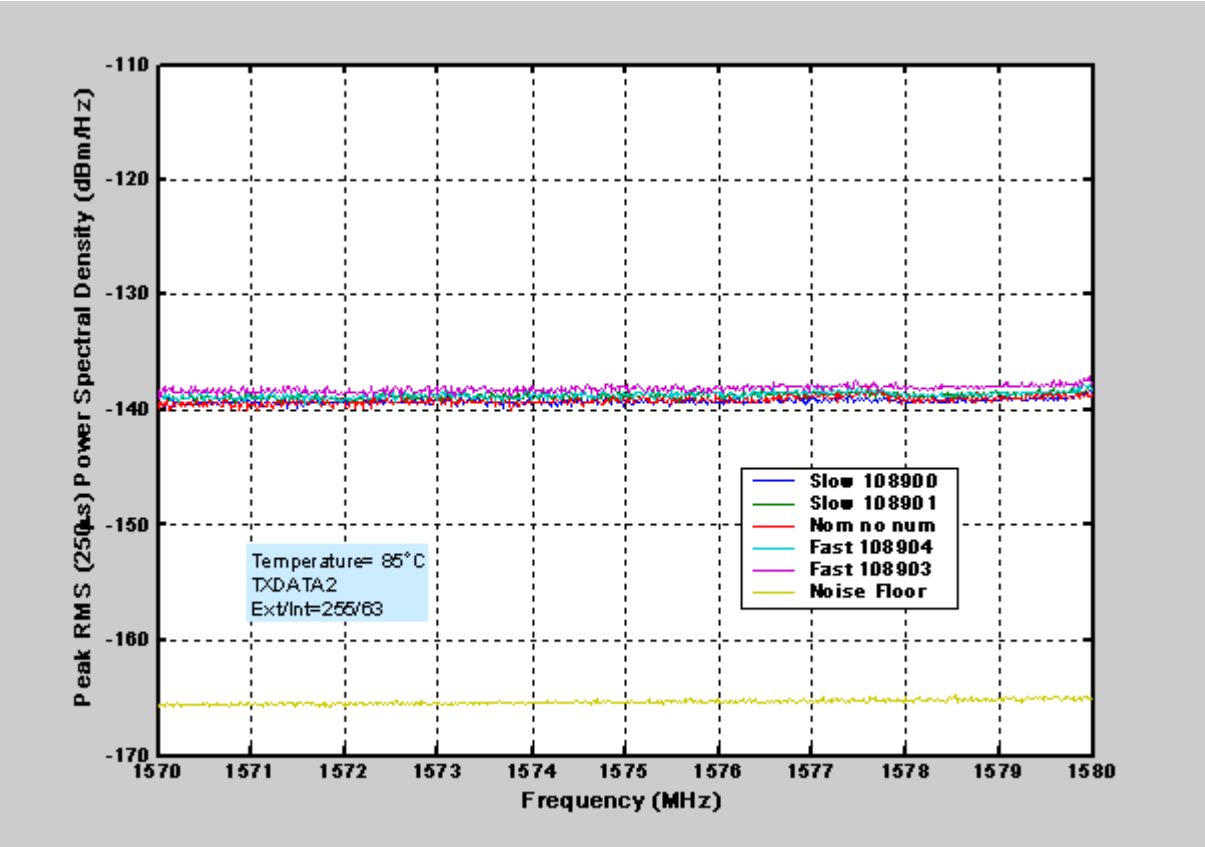


Figure 10.40: Emissions in Vicinity of GPS Downlink at 85°C

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

DH1 packets, frequency hopping

RBW 1MHz

Output power at maximum

10.2 Receiver Performance

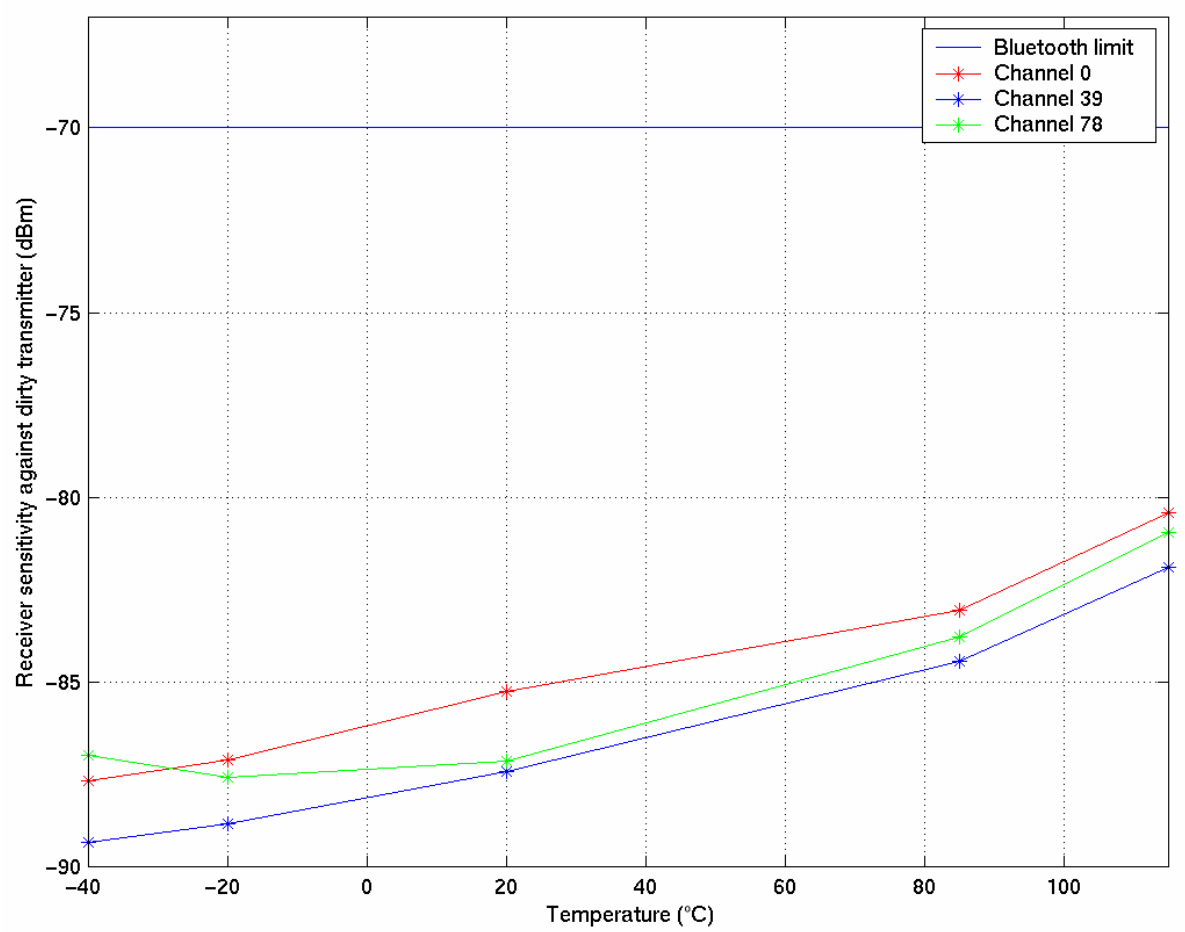


Figure 10.41: Receiver Sensitivity vs. Temperature

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63.

DH5 packets with dirty transmitter on.

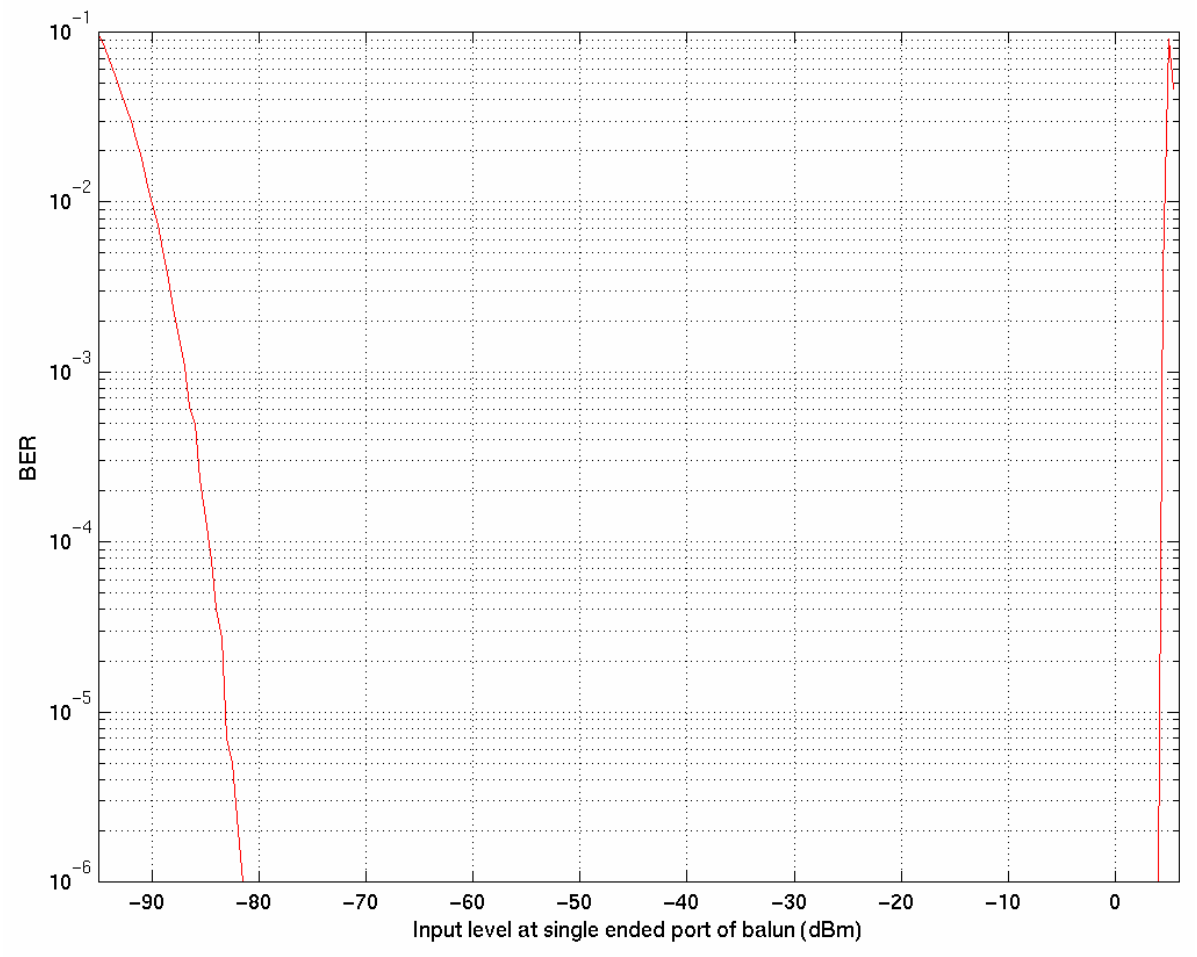


Figure 10.42: Bit Error Rate vs. Input Power

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63.

Temperature: 20°C

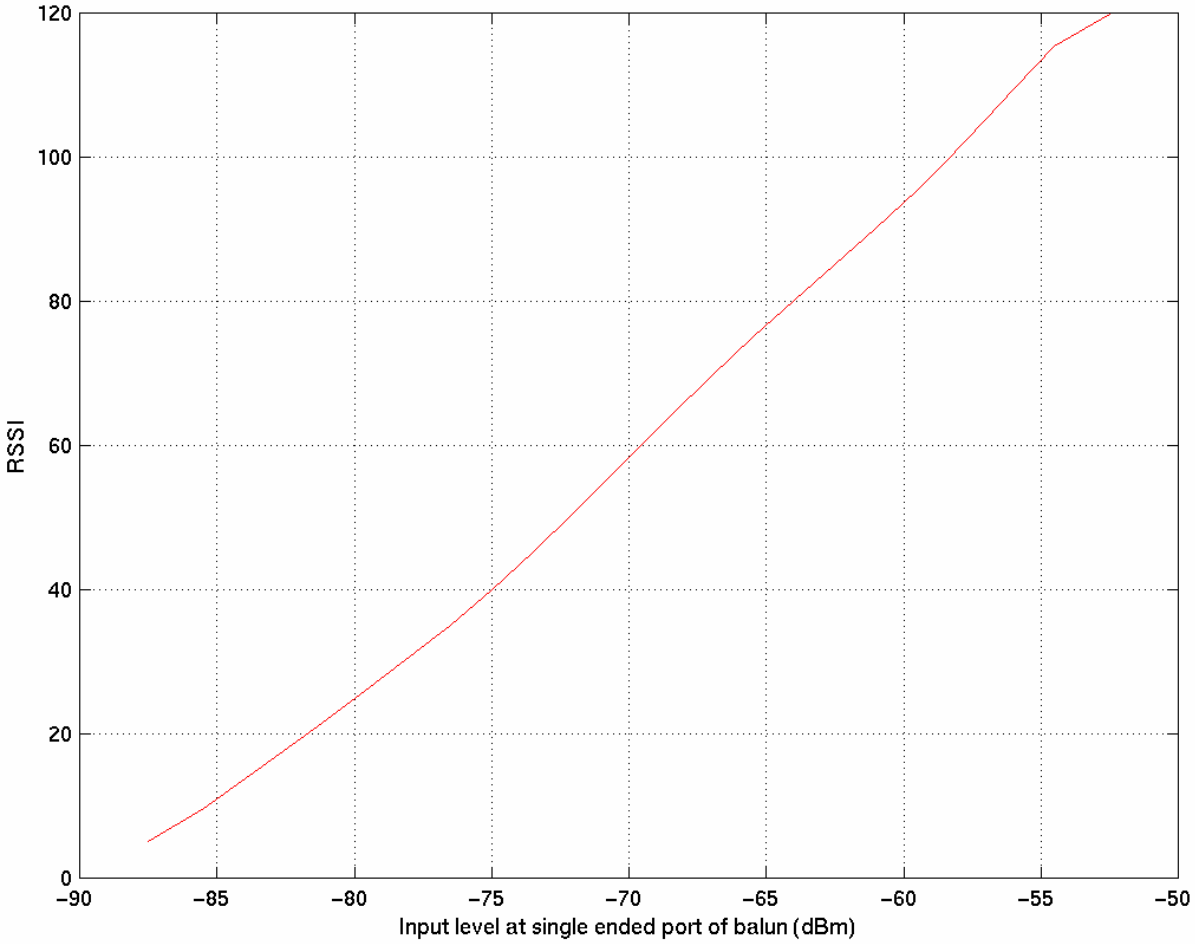


Figure 10.43: RSSI vs. Signal Input Level

Notes:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63.

Temperature: 20°C

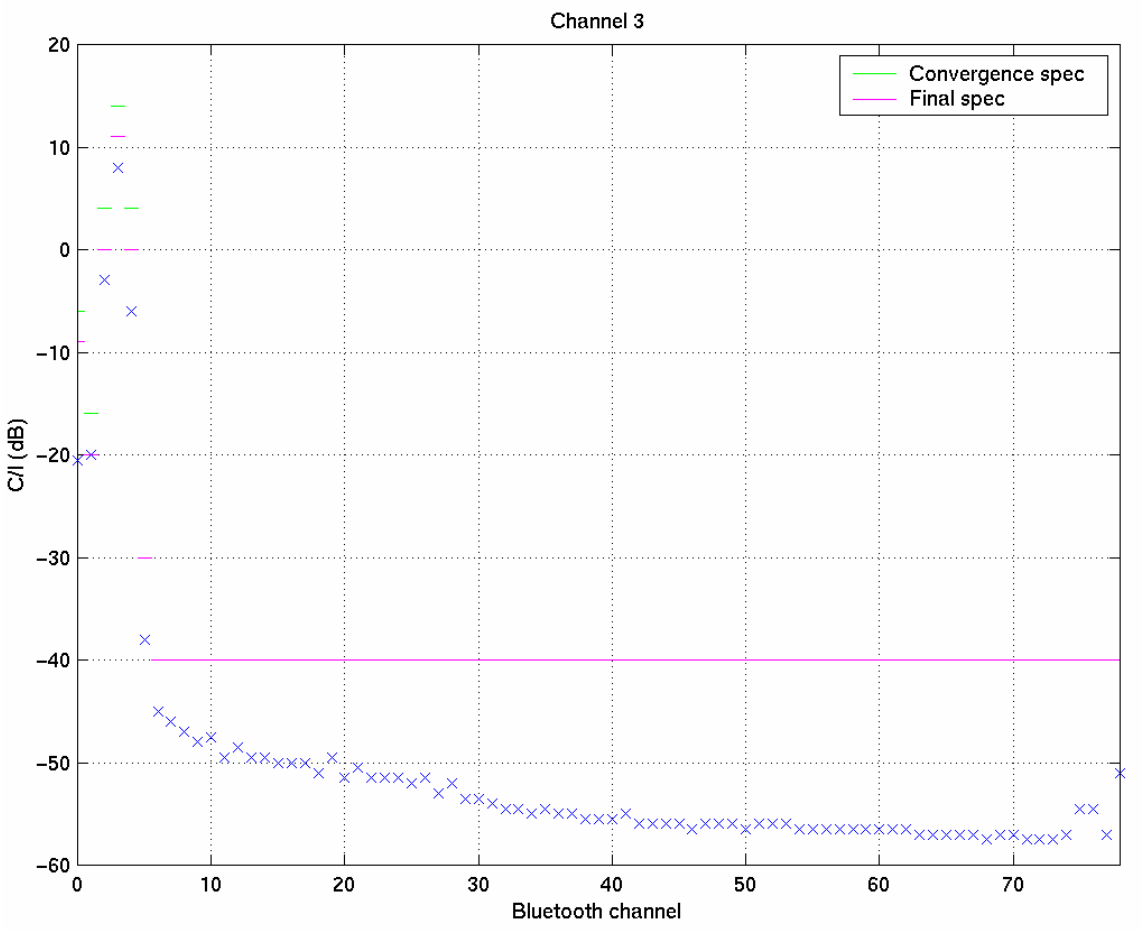


Figure 10.44: C/I Performance for Channel 3

Notes:

Frequency of wanted signal (f_0) = 2.405GHz

Image frequency (fimage) = f_0 –3MHz

Temperature = 20°C

Maximum allowed C/I ($f=f_0$) = 11dB

Maximum allowed C/I ($f=f_0 \pm 1$MHz) = 0dB

Maximum allowed C/I ($f=f_0 \pm 2$MHz) = -30dB

Maximum allowed C/I ($f=f_0 \pm \geq 3$MHz) = -40dB, with up to 5 exceptions allowed

Maximum allowed C/I ($f=f_{image}$) = -9dB

Maximum allowed C/I ($f=f_{image} \pm 1$MHz) = -20dB

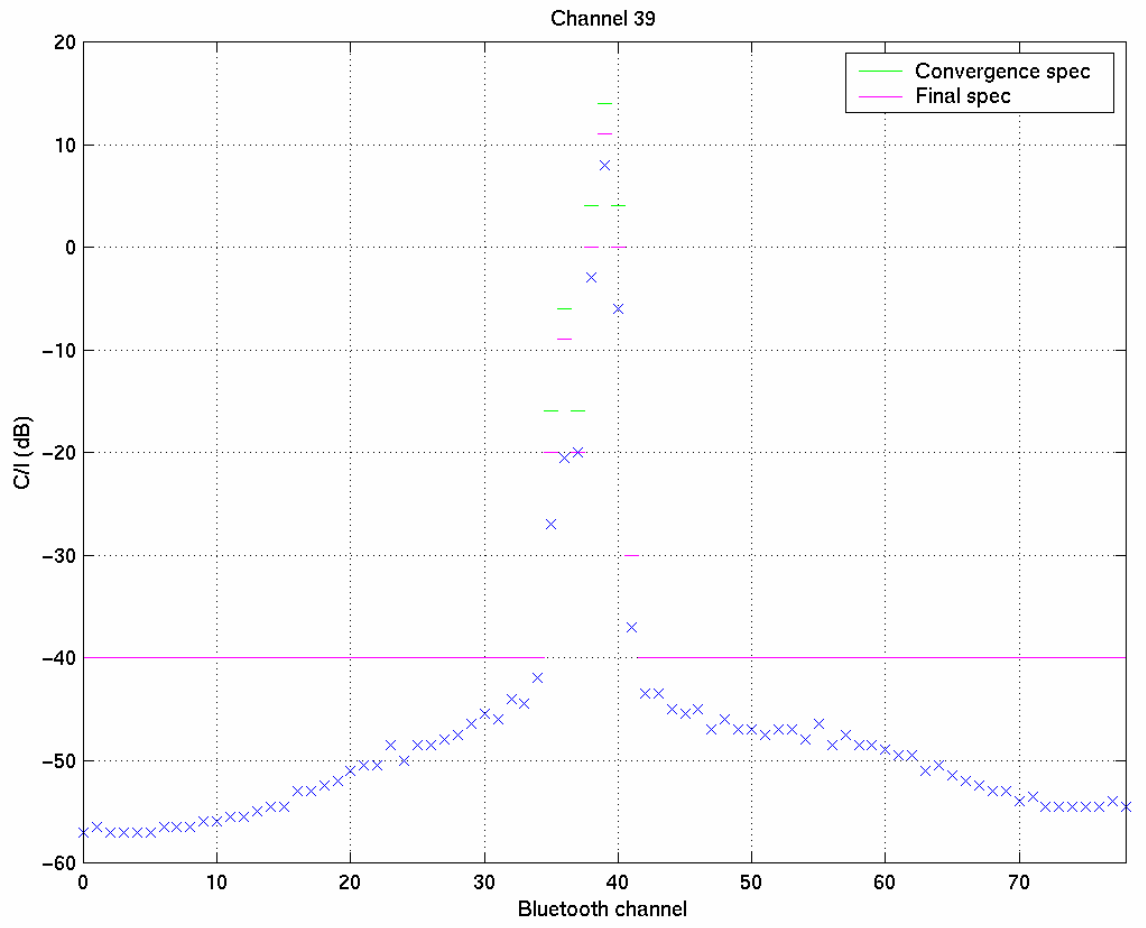


Figure 10.45: C/I Performance for Channel 39

Notes:

Frequency of wanted signal (f_0) = 2.441GHz

Image frequency (fimage) = f_0 –3MHz

Temperature = 20°C

Maximum allowed C/I ($f=f_0$) = 11dB

Maximum allowed C/I ($f=f_0 \pm 1$MHz) = 0dB

Maximum allowed C/I ($f=f_0 \pm 2$MHz) = -30dB

Maximum allowed C/I ($f=f_0 \pm \geq 3$MHz) = -40dB, with up to 5 exceptions allowed

Maximum allowed C/I ($f=f_{image}$) = -9dB

Maximum allowed C/I ($f=f_{image} \pm 1$MHz) = -20dB

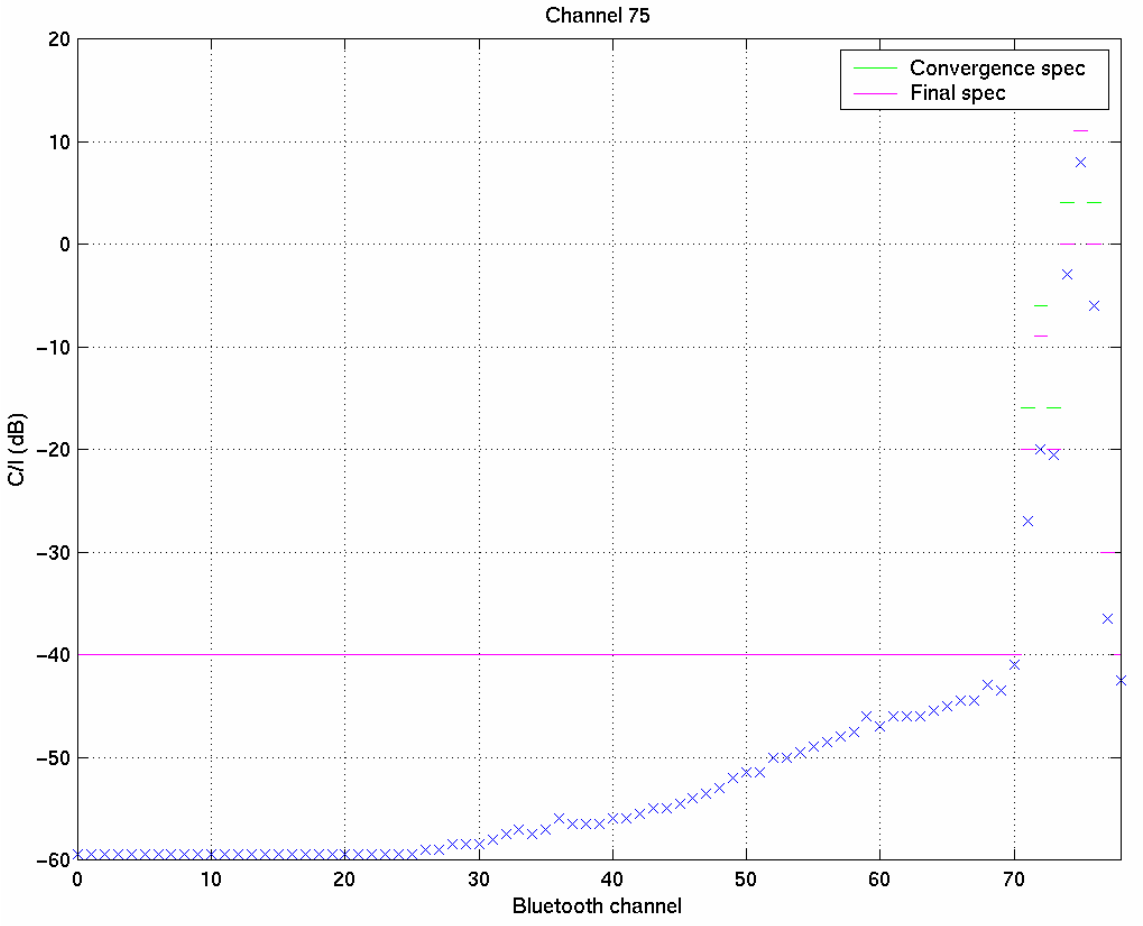


Figure 10.46: C/I Performance for Channel 75

Notes:

Frequency of wanted signal (f_0) = 2.477GHz

Image frequency (fimage) = f_0 –3MHz

Temperature = 20°C

Maximum allowed C/I ($f=f_0$) = 11dB

Maximum allowed C/I ($f=f_0 \pm 1$MHz) = 0dB

Maximum allowed C/I ($f=f_0 \pm 2$MHz) = -30dB

Maximum allowed C/I ($f=f_0 \pm \geq 3$MHz) = -40dB, with up to 5 exceptions allowed

Maximum allowed C/I ($f=f_{image}$) = -9dB

Maximum allowed C/I ($f=f_{image} \pm 1$MHz) = -20dB

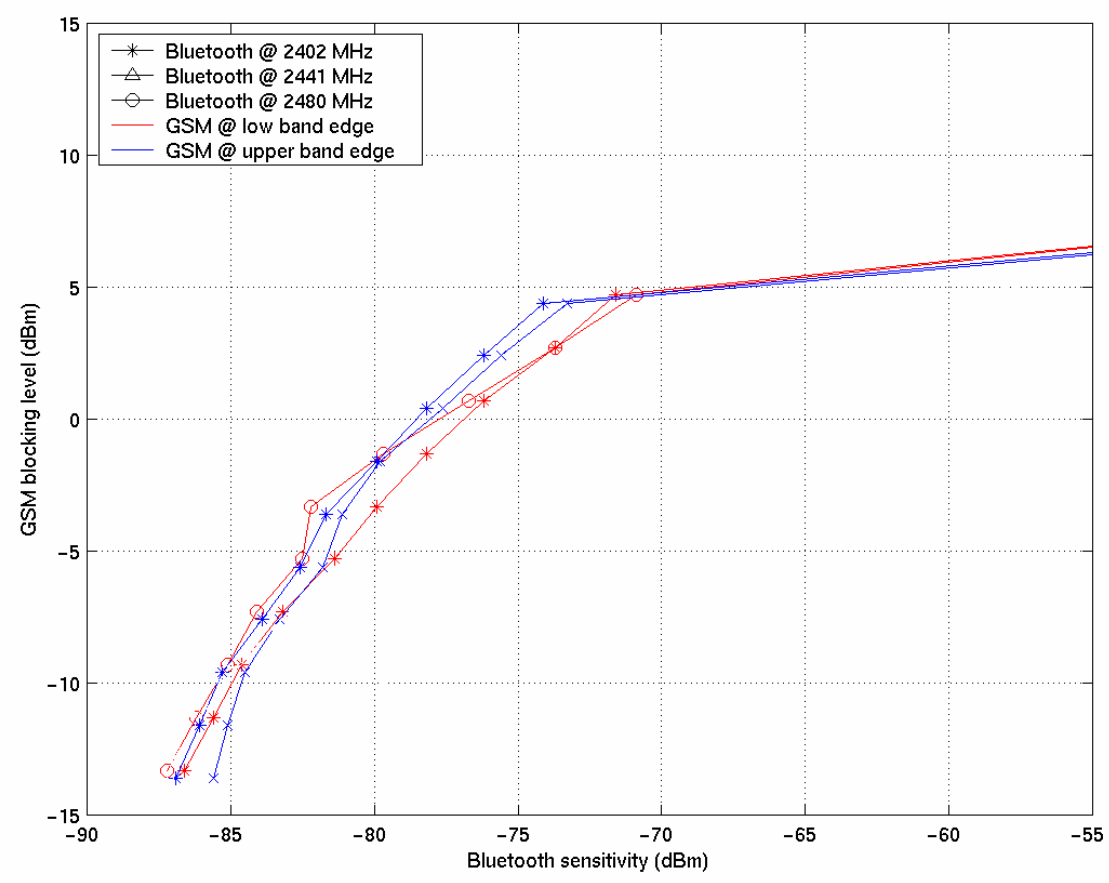


Figure 10.47: GSM Blocking in Band 880 to 915MHz at-30°C

Note:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

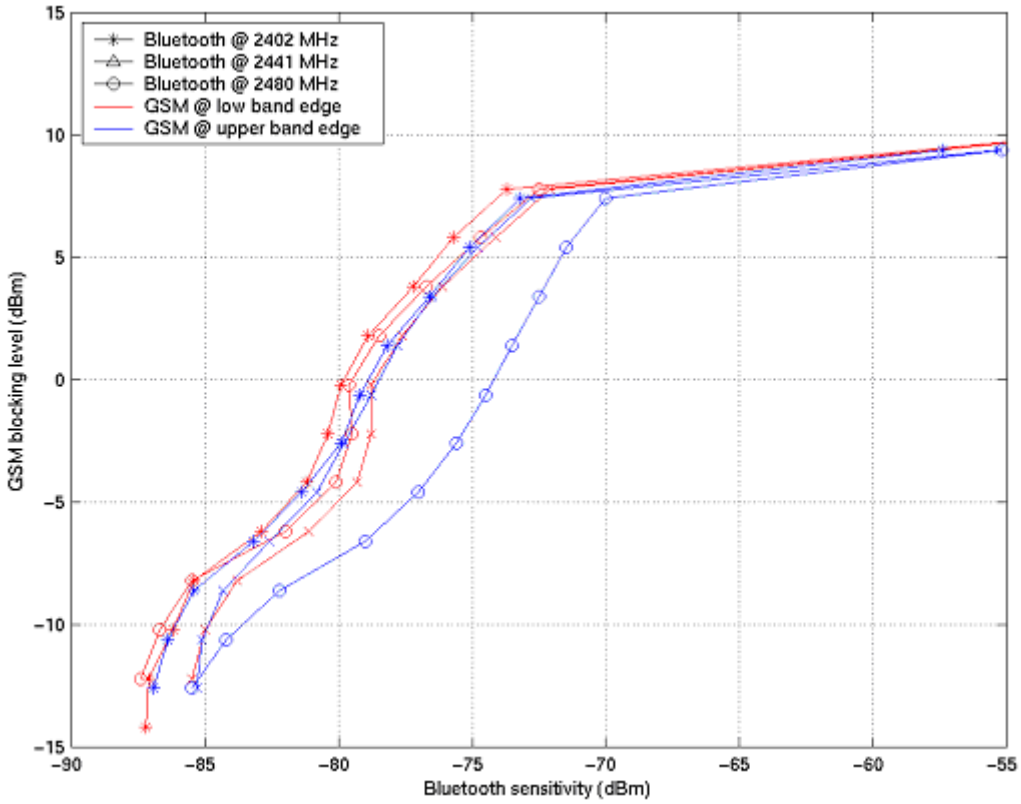


Figure 10.48: GSM Blocking in Band 1710 to 1785MHz at-30°C

Note:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

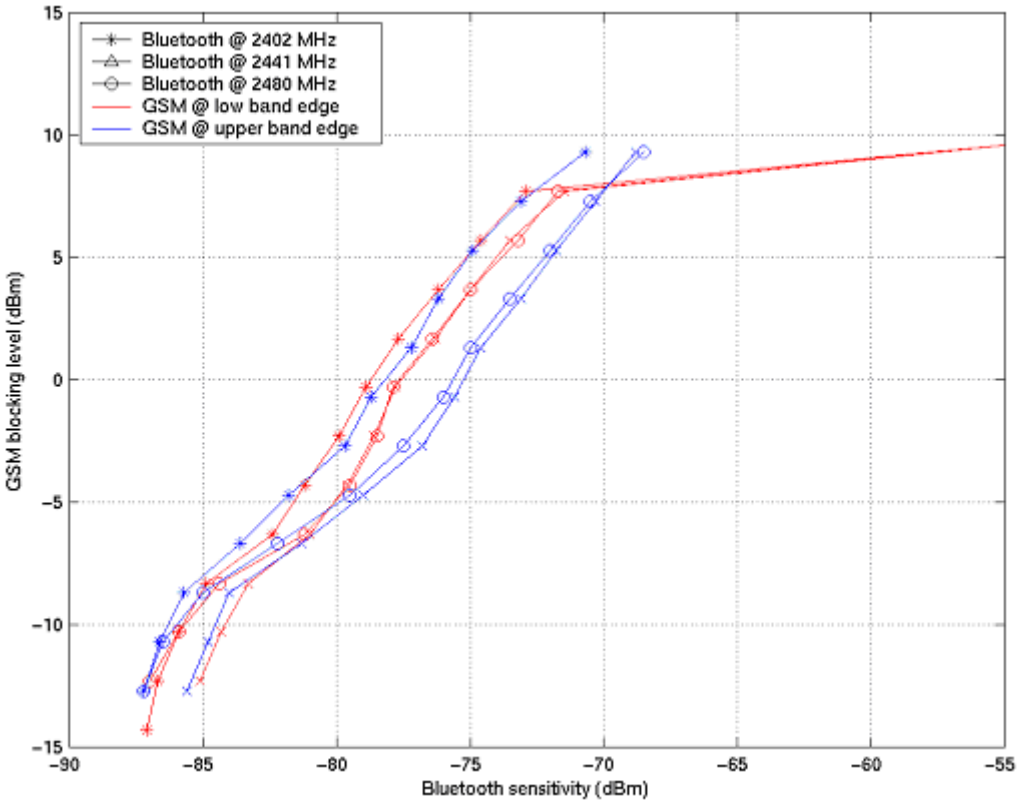


Figure 10.49: GSM Blocking in Band 1850 to 1910MHz at -30°C

Note:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

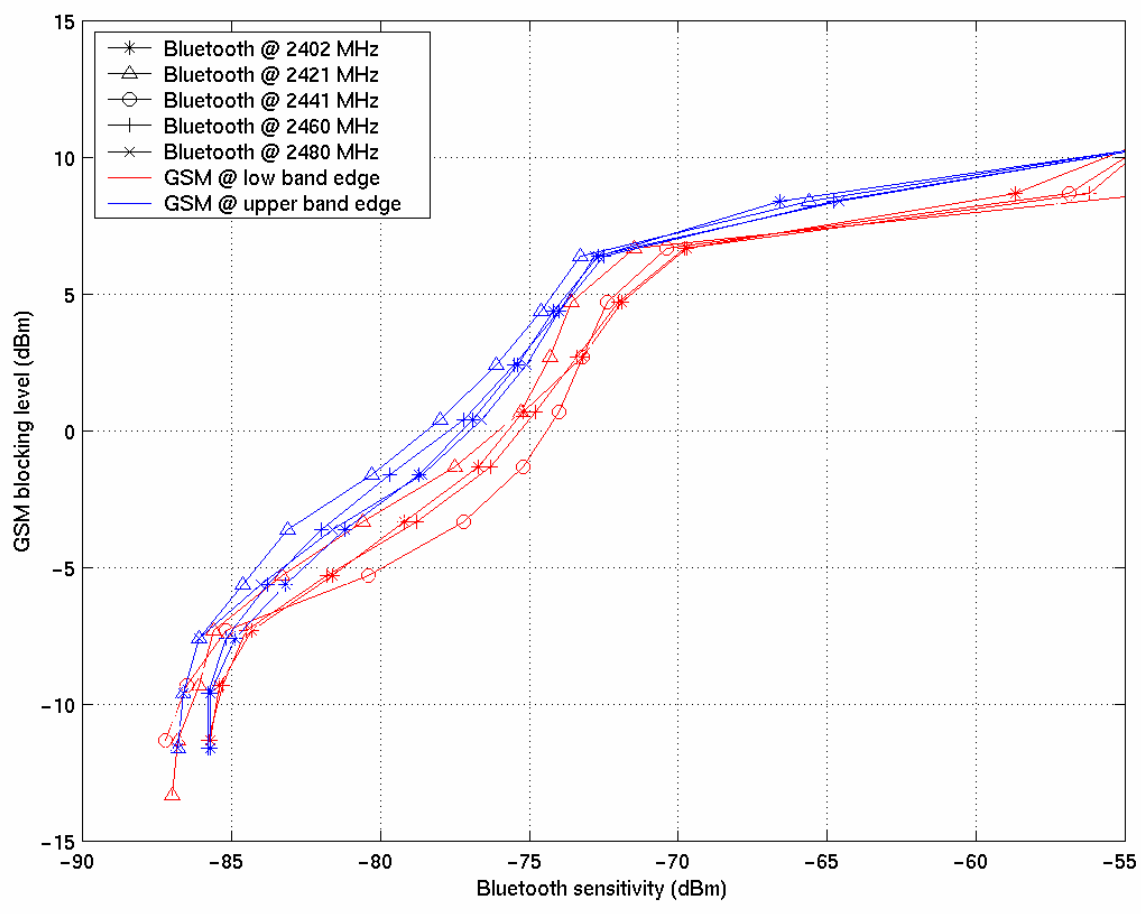


Figure 10.50: GSM Blocking in Band 880 to 915MHz at 23°C

Note:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

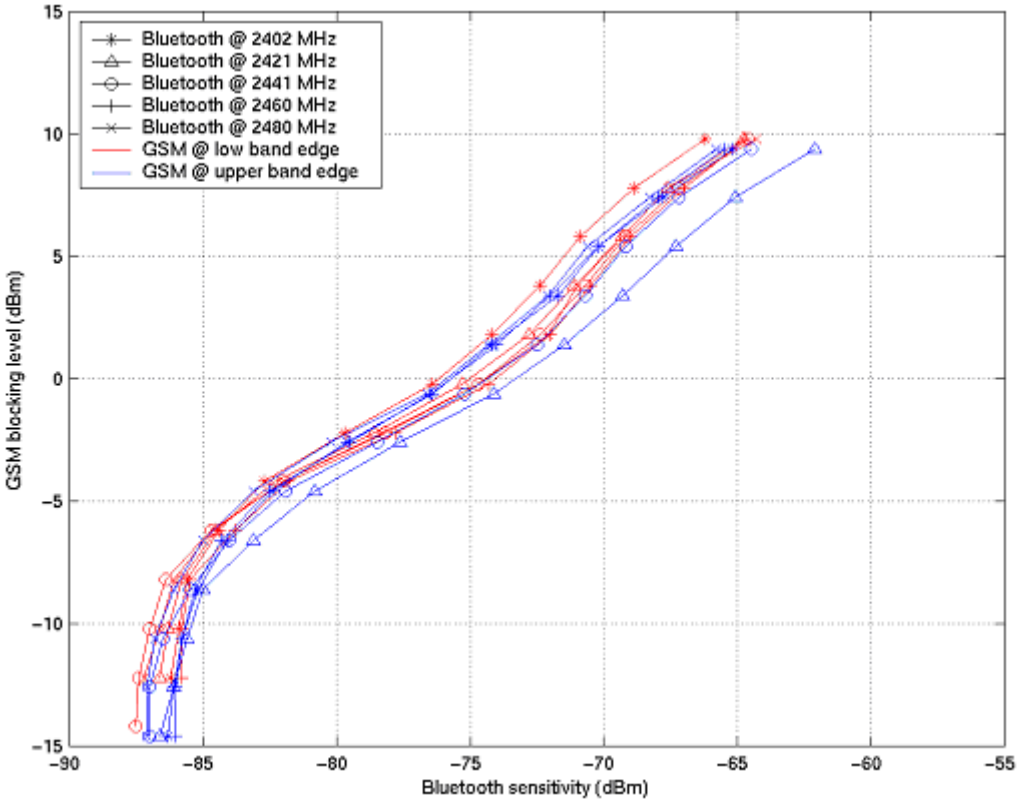


Figure 10.51: GSM Blocking in Band 1710 to 1785MHz at 23°C

Note:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

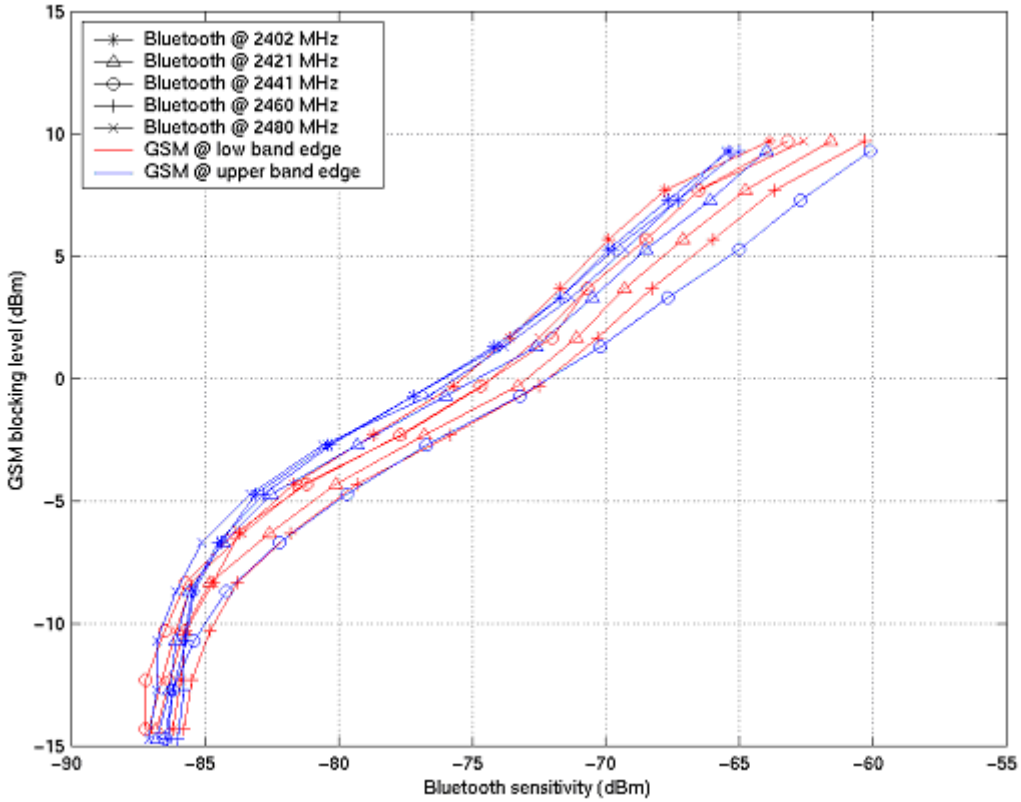


Figure 10.52: GSM Blocking in Band 1850 to 1910MHz at 23°C

Note:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

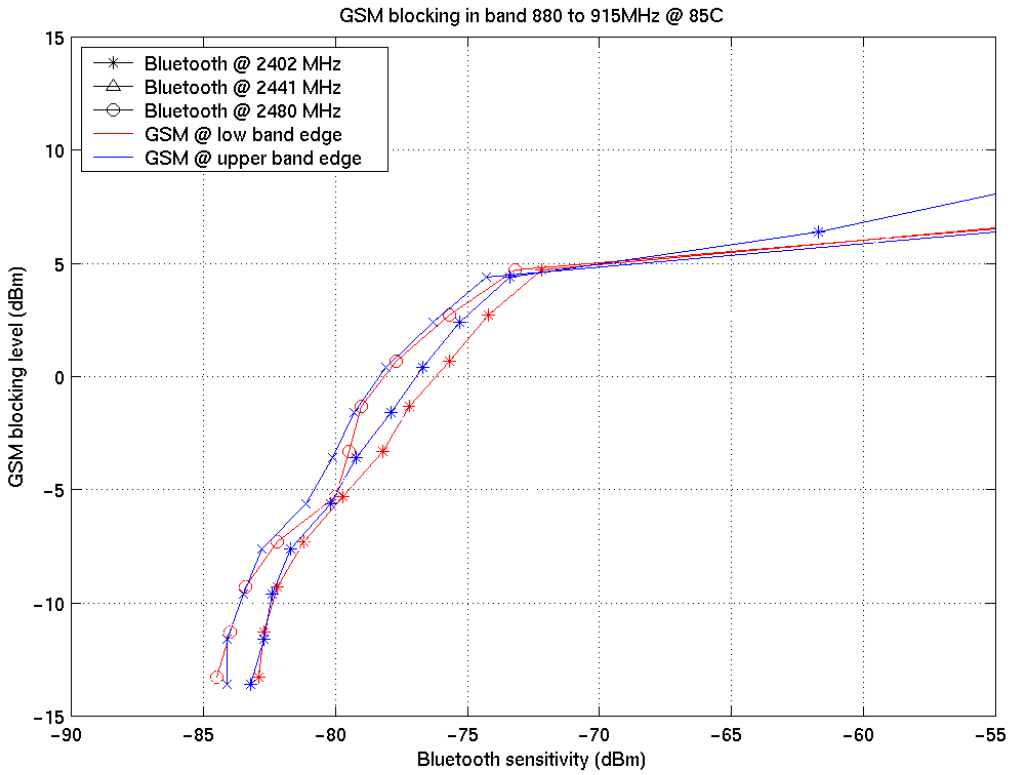


Figure 10.53: GSM Blocking in Band 880 to 915MHz at 85°C

Note:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

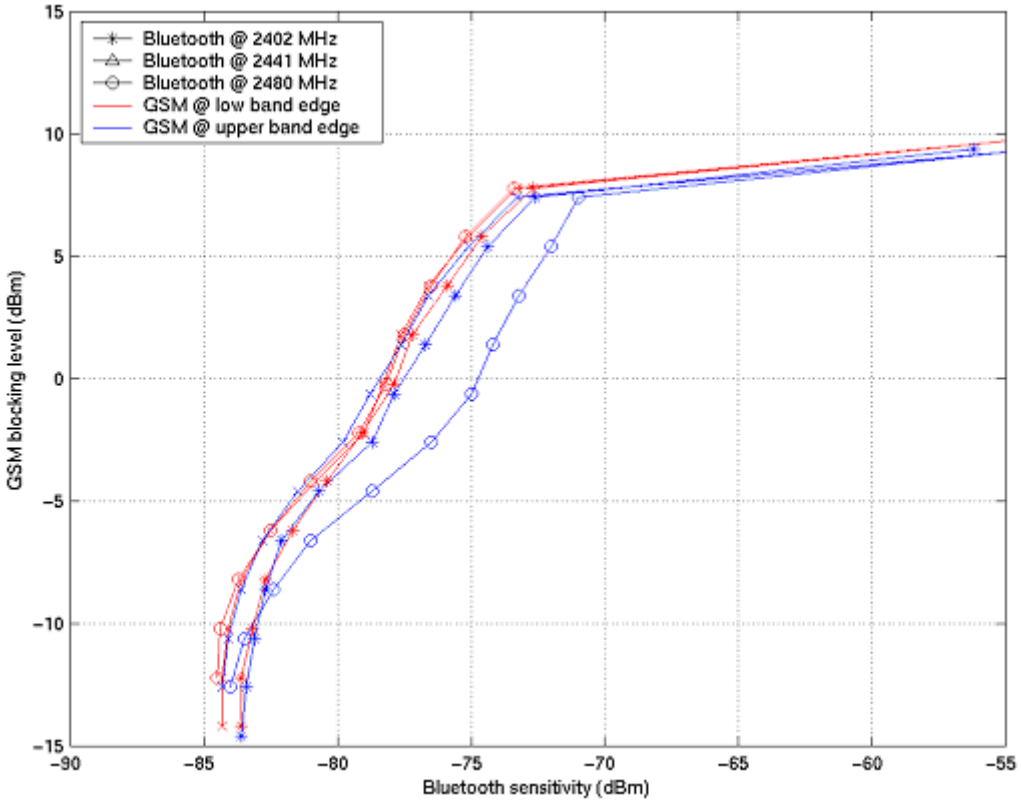


Figure 10.54: GSM Blocking in Band 1710 to 1785MHz at 85°C

Note:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

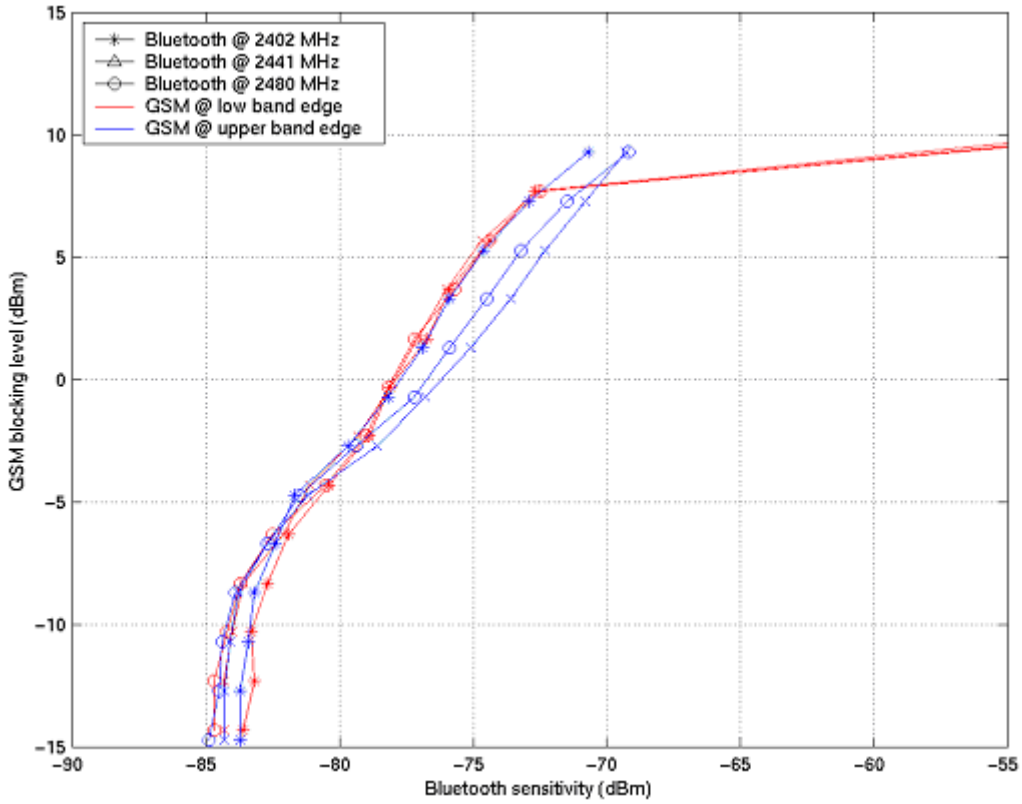


Figure 10.55: GSM Blocking in Band 1850 to 1910MHz at 85°C

Note:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

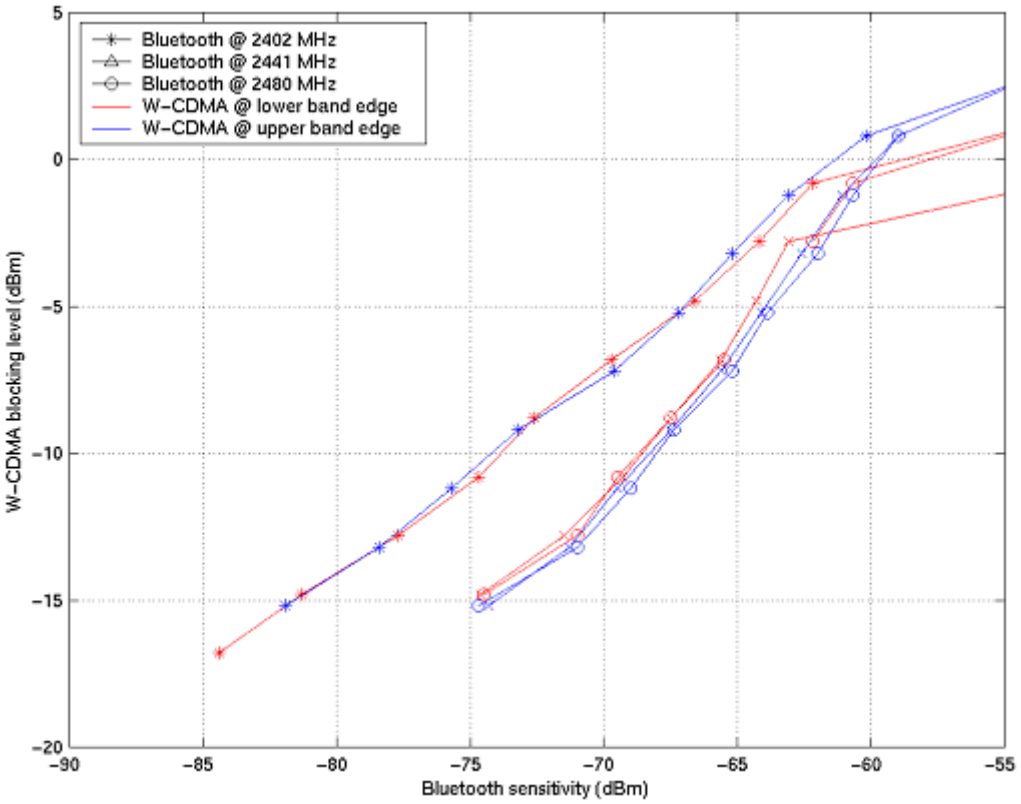


Figure 10.56: W-CDMA Blocking in Band 1920 to 1980MHz at -30°C

Note:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

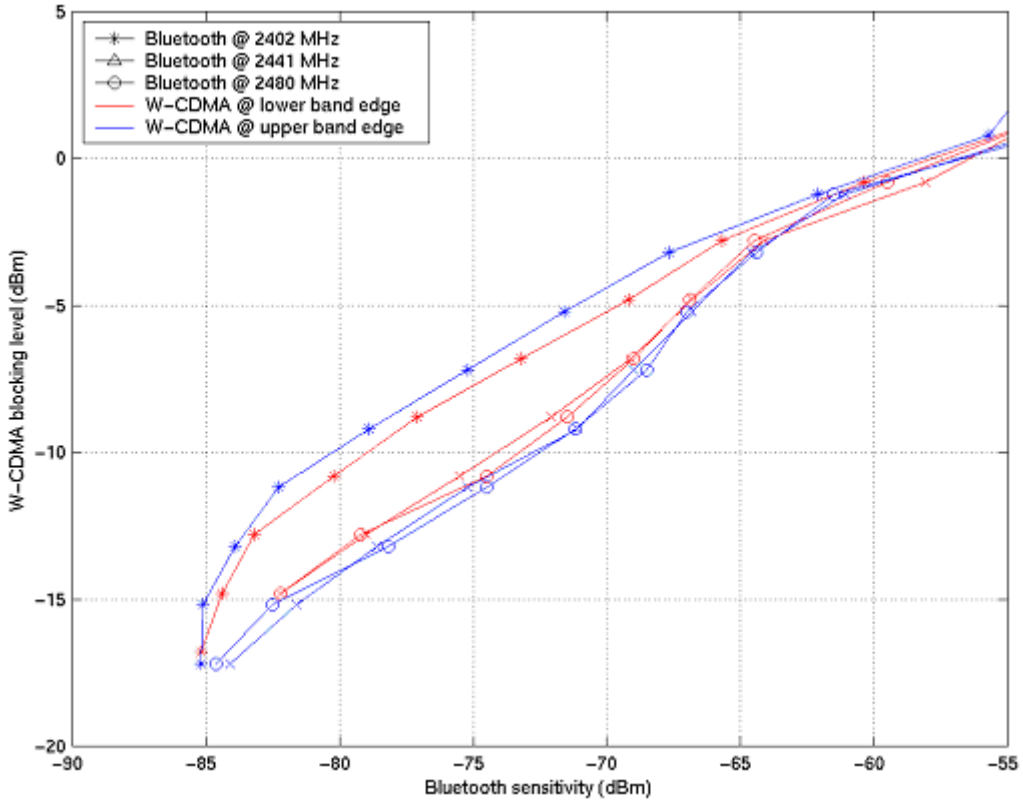


Figure 10.57: W-CDMA Blocking in Band 1920 to 1980MHz at 23°C

Note:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

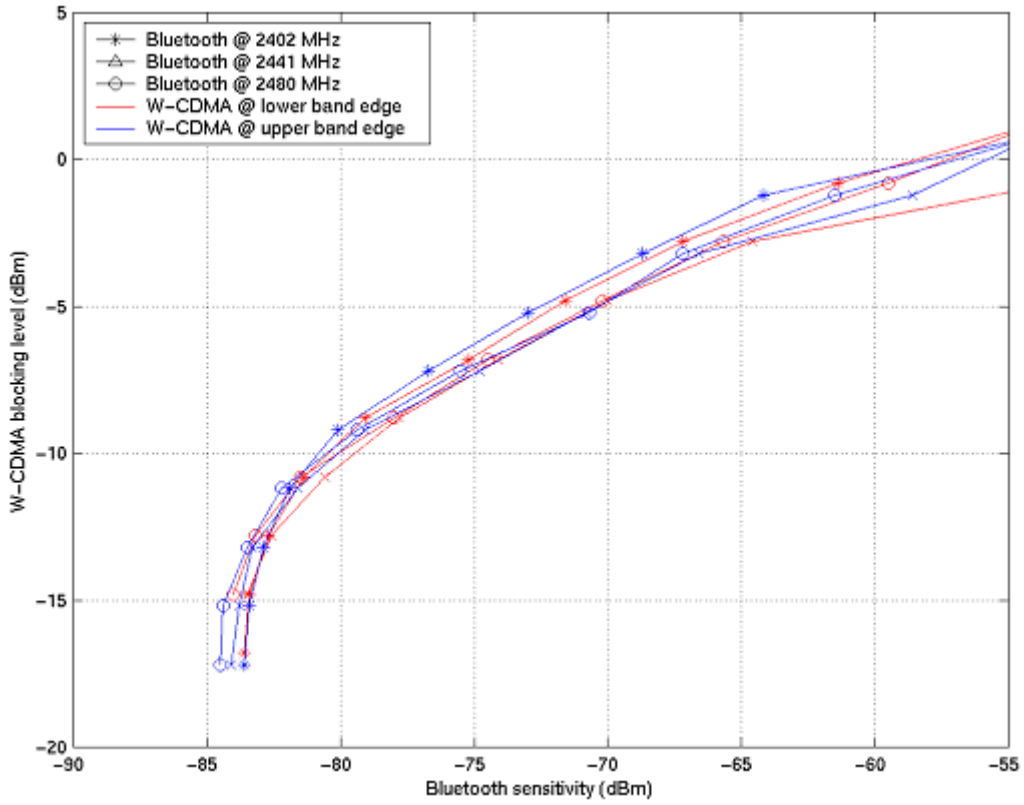


Figure 10.58: W-CDMA Blocking in Band 1920 to 1980MHz at 85°C

Note:

Results obtained using CSR's evaluation circuit as shown in Figure 10.63 with the ceramic filter bypassed.

10.3 Transmit and Receive Immunity to Power Line Disturbances

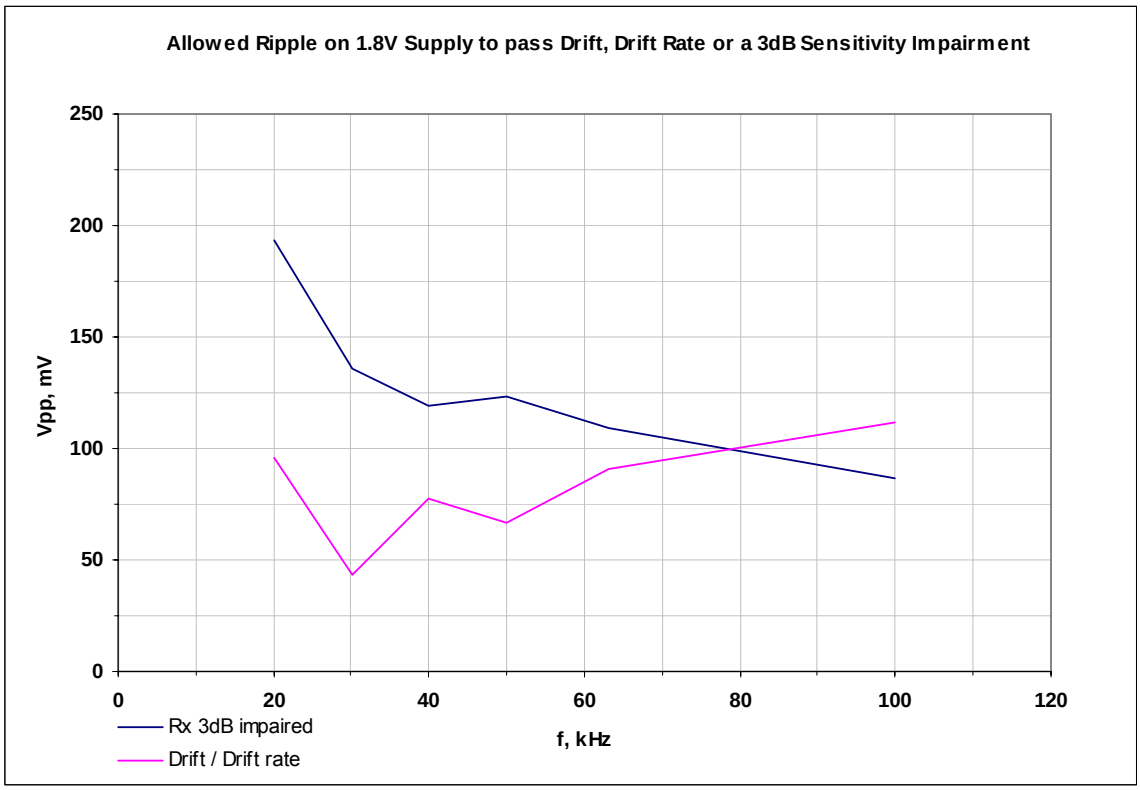


Figure 10.59: Allowed Ripple on 1.8V Supply (Up to 100kHz)

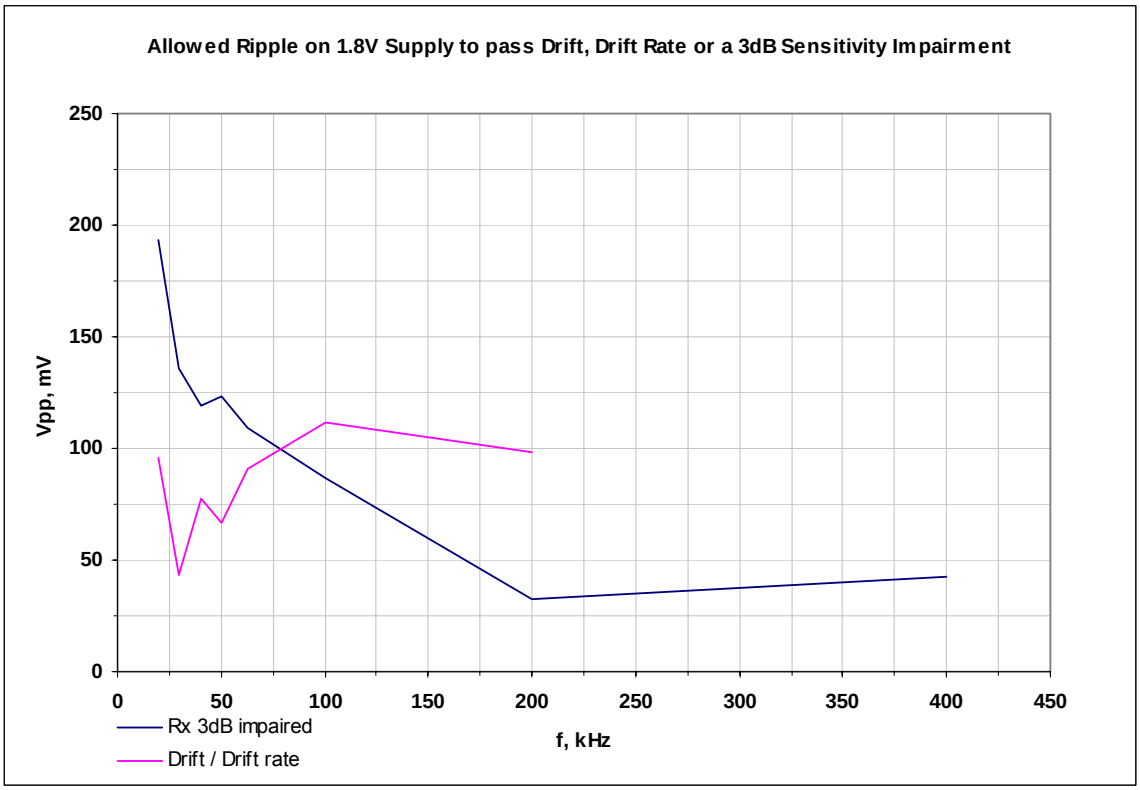


Figure 10.60: Allowed Ripple on 1.8V Supply (Wideband)

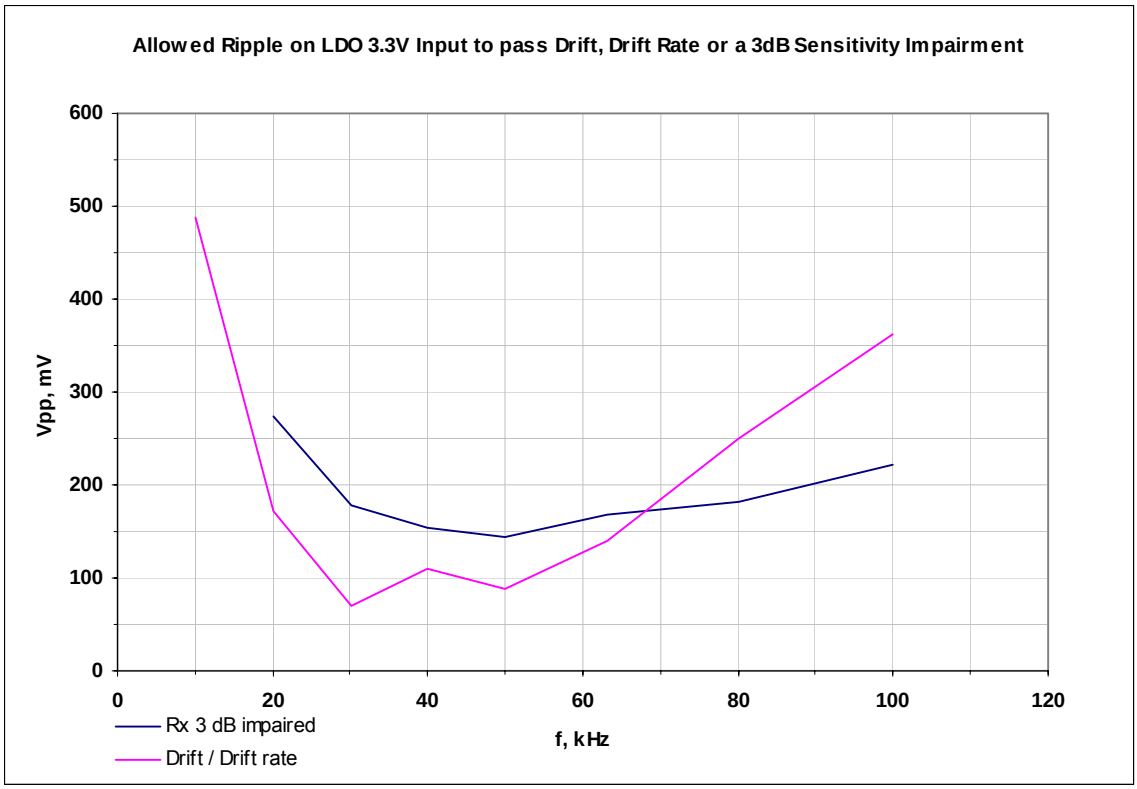


Figure 10.61: Allowed Ripple on LDO 3.3V Input (Up to 100kHz)

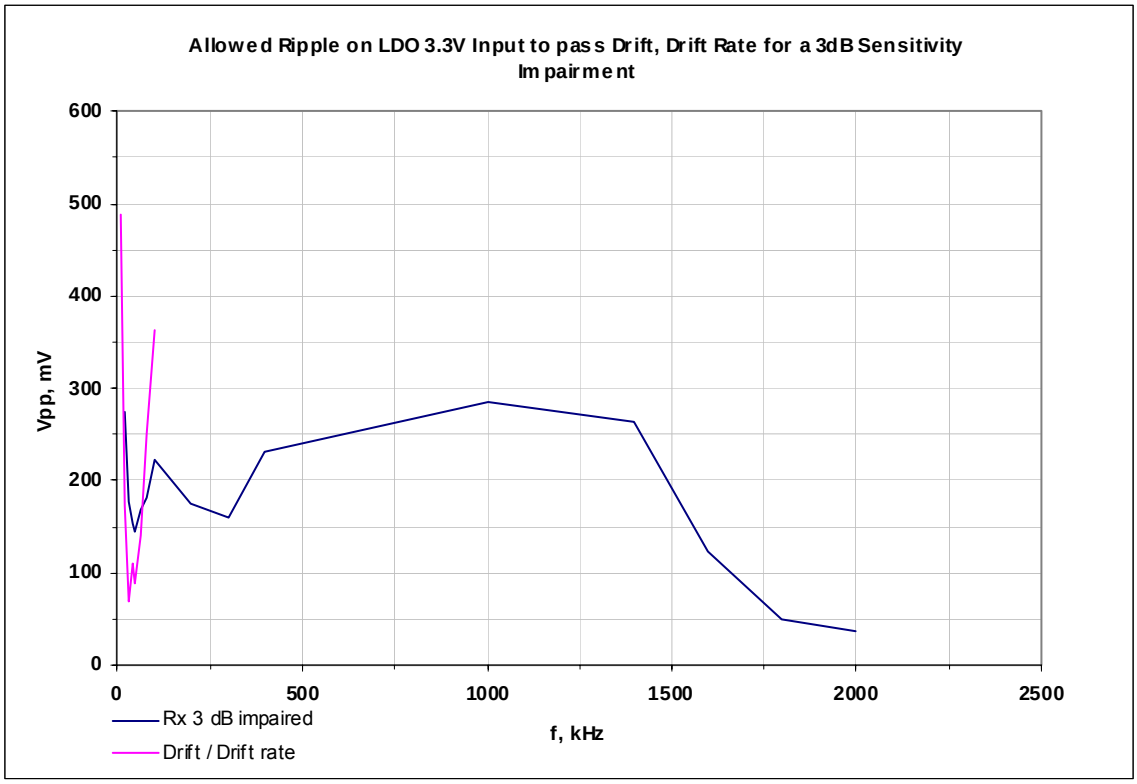


Figure 10.62: Allowed Ripple on LDO 3.3V Input (Wideband)

Notes:

The disturbance signal (a sine wave) from a signal generator was introduced into the supply lines through a series capacitor.

3dB Receive sensitivity impairment measurement method:

1. The minimum input signal level for 0.1% BER was first measured in the absence of a disturbance signal, using BER1 in Bluetest.
2. The level on the signal generator was then increased by 3 dB. This brings down the BER to levels of approximately 0.02%.
3. The disturbance signal amplitude was increased until the BER was again 0.1%. This disturbance level was measured at the relevant chip terminal and recorded as a function of the disturbance signal frequency.

Drift / drift rate measurement method:

1. 1. TXDATA3, power level 63 was set up in BlueTest.
2. 2. The demodulated signal was observed on the spectrum analyser in Bluetooth mode.
3. 3. A "pass" is considered to be 10 consecutive measurements with no errors reported.

Instruments used:

- HP 33120A 15 MHz Function/ Arbitrary Waveform Generator
- HP3585B 20 Hz - 40 MHz Spectrum Analyzer (with Bluetooth personality module)
- Agilent E4432B Signal Generator (with Bluetooth personality module)

10.4 RF Characterisation Circuit

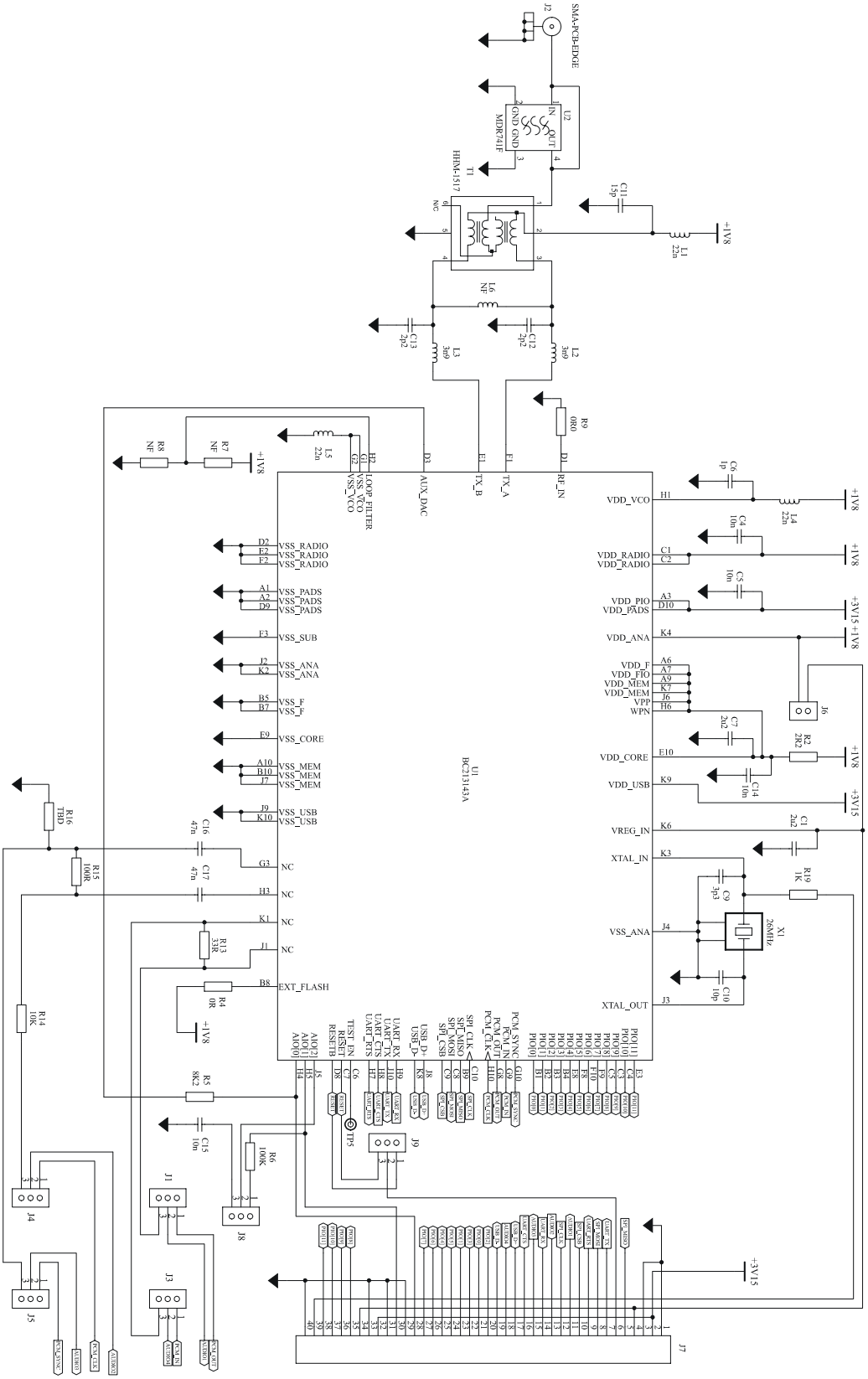


Figure 10.63: Circuit Showing Radio Characterisation

11 Application Schematics

11.1 6 x 6 VFBGA 84-Ball Package

11.1.1 Application Schematic using Separate Balun and Filter

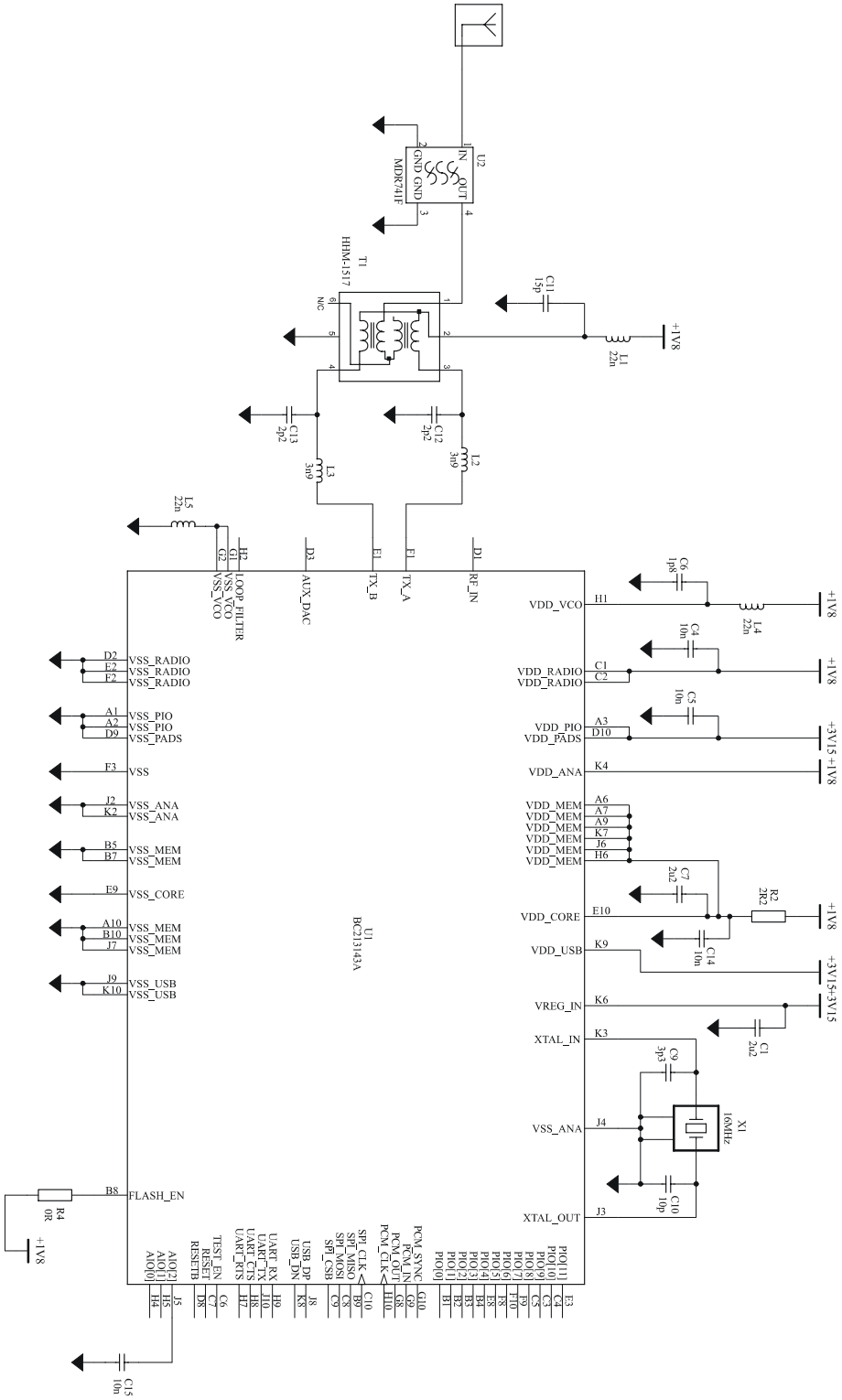


Figure 11.1: Application Circuit using Separate Balun and Filter for 6 x 6 VFBGA Package

11.1.2 Application Schematic using Epcos Combined Balun and Filter

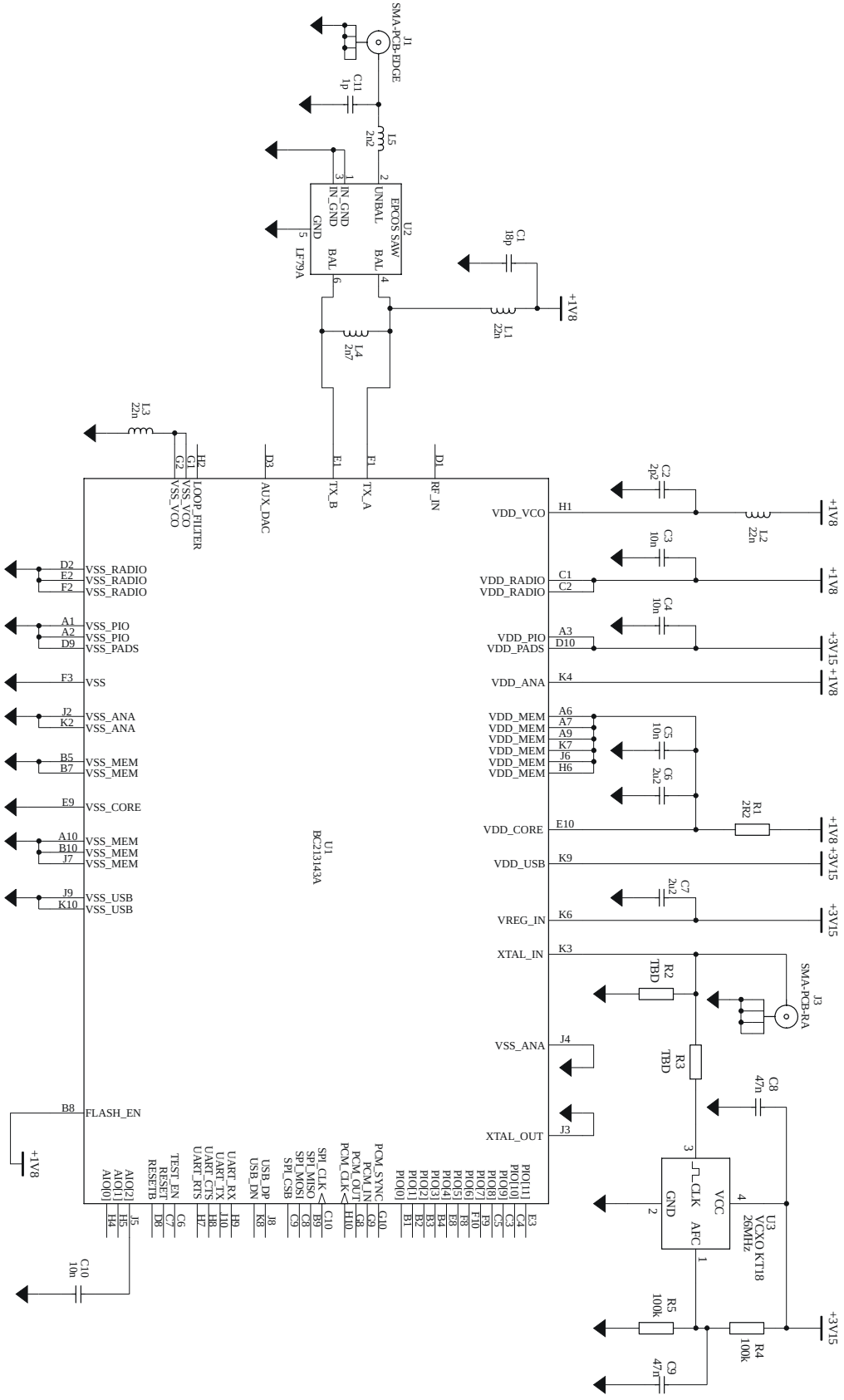


Figure 11.2: Application Circuit using Epcos Balun and Filter for 6 x 6 VFBGA Package

11.1.3 Application Schematic using Soshin Combined Balun and Filter

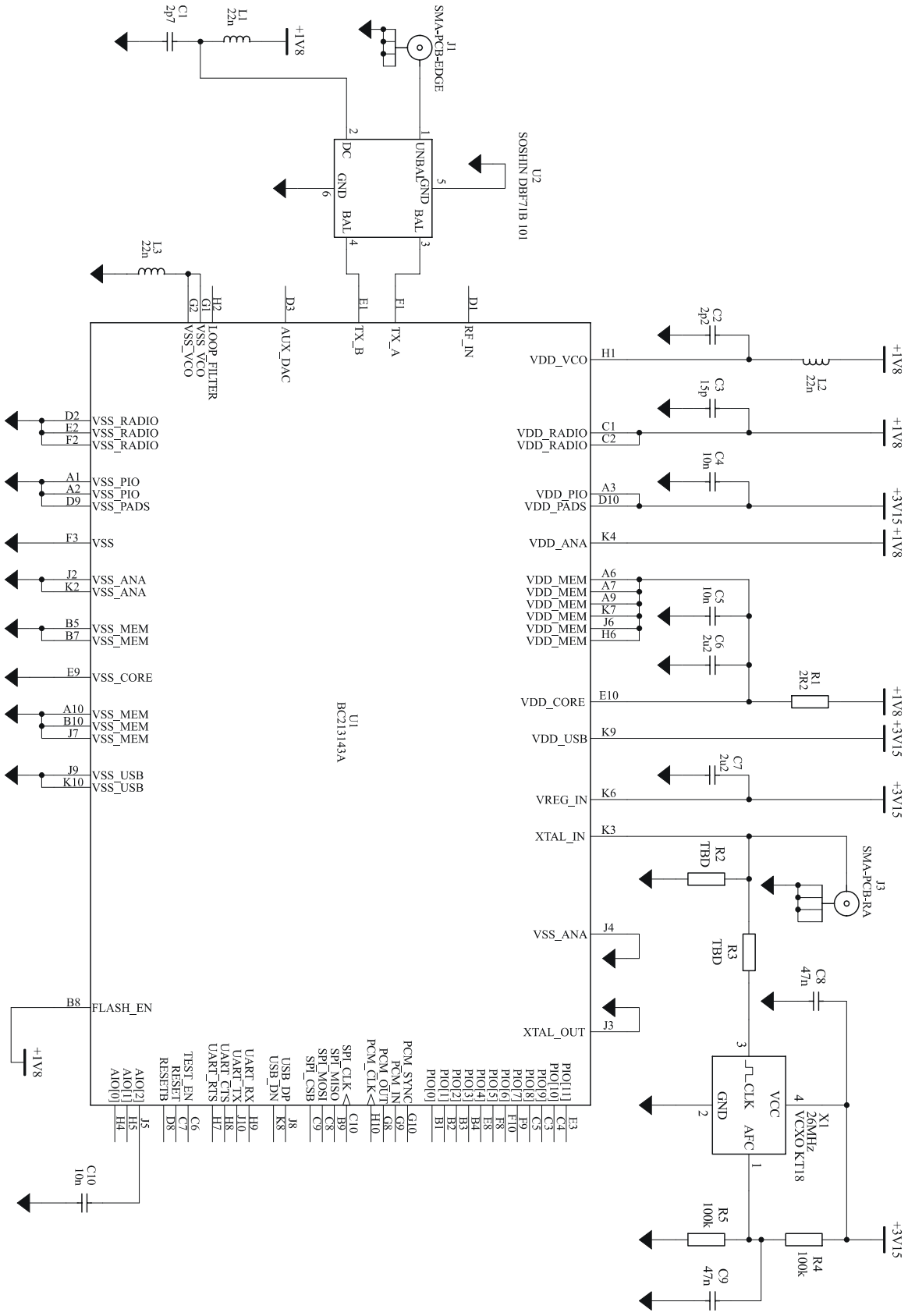


Figure 11.3: Application Circuit using Soshin Balun and Filter for 6 x 6 VFBGA Package

11.2 4 x 4 CSP 47-Ball Package

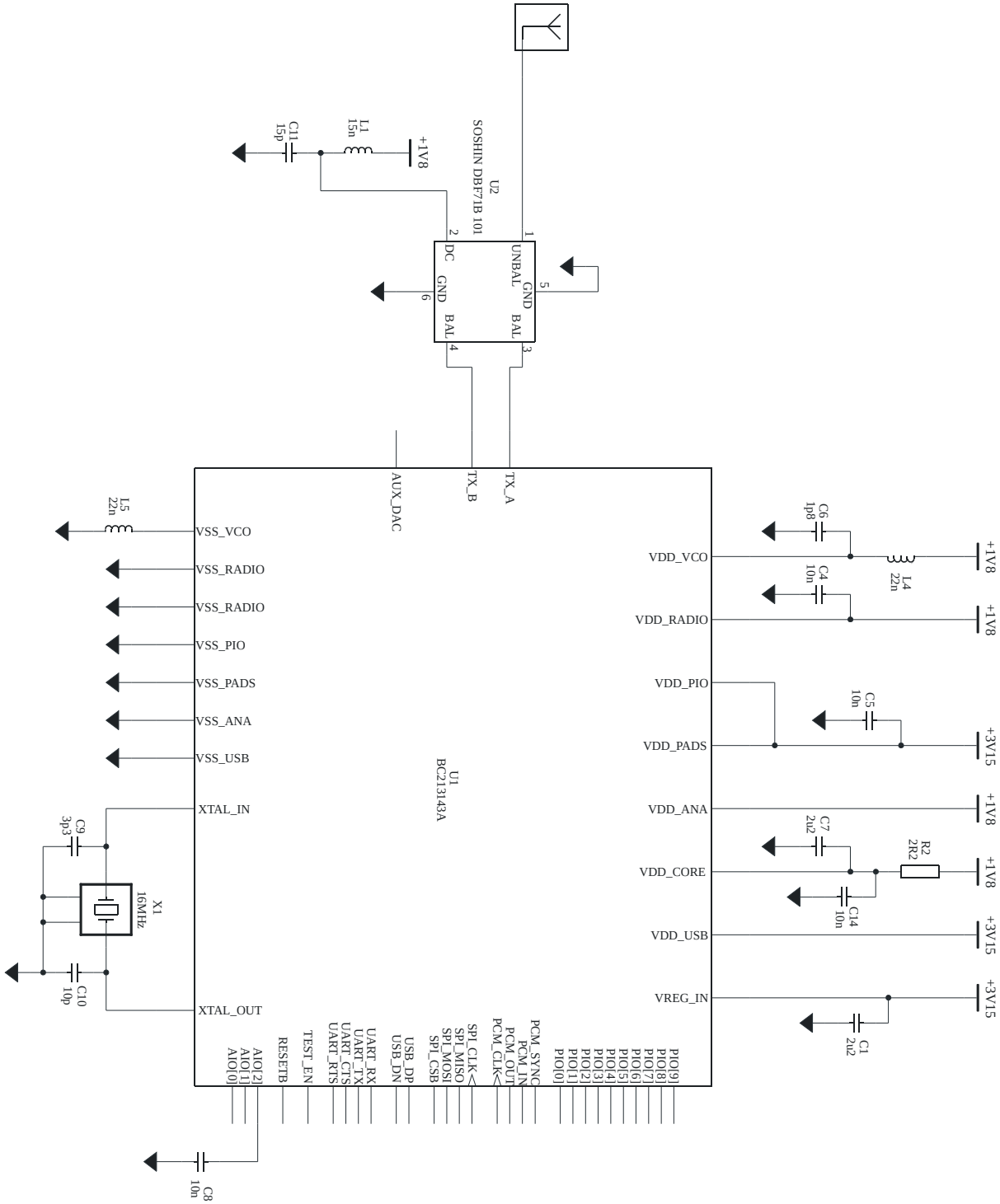
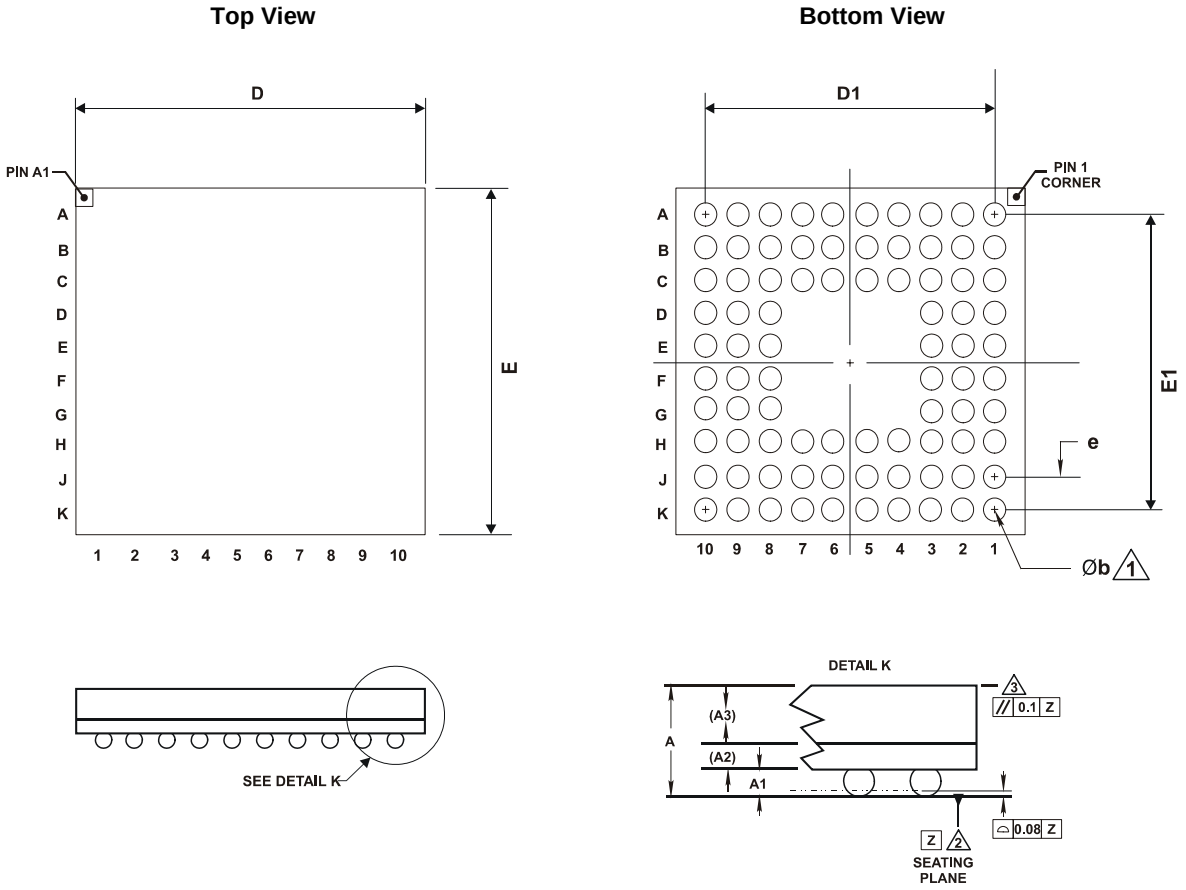


Figure 11.4: Application Circuit for 4 x 4 CSP Package

12 Package Dimensions

12.1 6 x 6 VFBGA 84-Ball Package



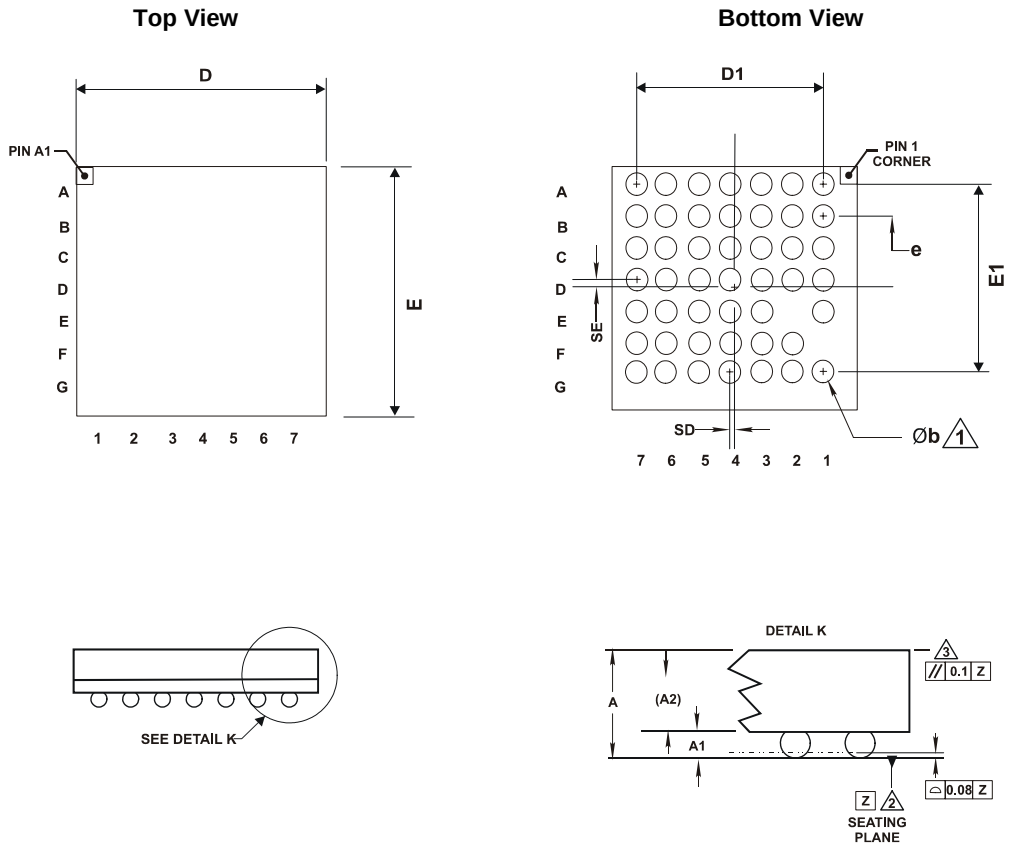
BC213143AXX-EK and BC213143AXX-RK 84-Ball 6x6x1mm VFBGA				
DIM	MIN	TYP	MAX	NOTES
A	0.8		1	
A1	0.2		0.3	
A2		0.22		
A3		0.45		
b	0.25	0.30	0.35	
D	5.90	6	6.10	
E	5.90	6	6.10	
e		0.50		
D1		4.50		
E1		4.50		

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM PLANE Z.
2. DATUM Z IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

84-Ball VFBGA 6X6X1 mm (JEDEC MO-225)	UNIT
	MM

Figure 12.1: BlueCore2-ROM VFBGA Package Dimensions

12.2 4 x 4 CSP 47-Ball Package



BC213143AXX-XB 47-Ball 4.2 x 4.4 x 0.7mm CSP				
DIM	MIN	TYP	MAX	NOTES
A	0.55	0.57	0.70	
A1	0.21	0.24	0.27	
A2		0.33		
b	0.25	0.30	0.35	
D	4.10	4.20	4.30	
E	4.25	4.35	4.45	
e		0.50		
D1		3.00		
E1		3.00		
SD		0.04		
SE		0.10		

NOTES

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM PLANE Z.
2. DATUM Z IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

47-Ball CSP 4.2 x 4.4 x 0.7mm (JEDEC MO-211)	UNIT
	MM

Figure 12.2: BlueCore2-ROM CSP Package Dimensions

13 Solder Profiles

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder re-flow. There are four zones:

1. Preheat Zone: This zone raises the temperature at a controlled rate, typically 1-2.5°C/s.
2. Equilibrium Zone: This zone brings the board to a uniform temperature and also activates the flux. The duration in this zone (typically 2-3 minutes) will need to be adjusted to optimise the out gassing of the flux.
3. Reflow Zone: The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint.
4. Cooling Zone: The cooling rate should be fast, to keep the solder grains small which will give a longer lasting joint. Typical rates will be 2-5°C/s.

13.1 Solder Re-flow Profile for Devices with Tin/Lead Solder Balls

Composition of the solder ball: Sn 62%, Pb 36.0%, Ag 2.0%

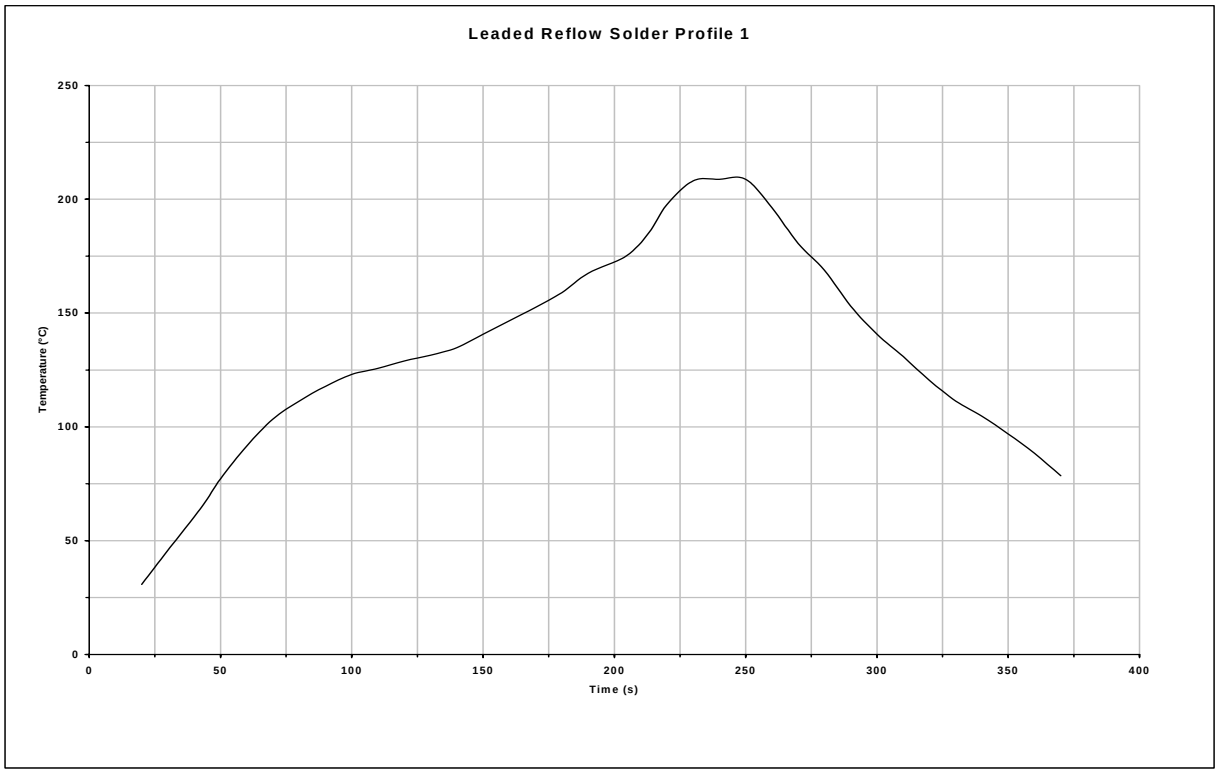


Figure 13.1: Typical Re-flow Solder Profile

Key features of the profile:

- Initial Ramp = 1-2.5°C/sec to 125°C±25°C equilibrium
- Equilibrium time = 60 to 120 seconds
- Ramp to Maximum temperature (210°C to 220°C) = 3°C/sec max.
- Time above liquidus (183°C): 45 to 90 seconds
- Device absolute maximum re-flow temperature 240°C

Devices will withstand the specified profile.

Lead-free devices will withstand up to 3 re-flows to a maximum temperature of 240°C.

Solder Re-flow Profile for Devices with Lead-Free Solder Balls

Composition of the solder ball: Sn 95.5%, Ag 4.0%, Cu 0.5%

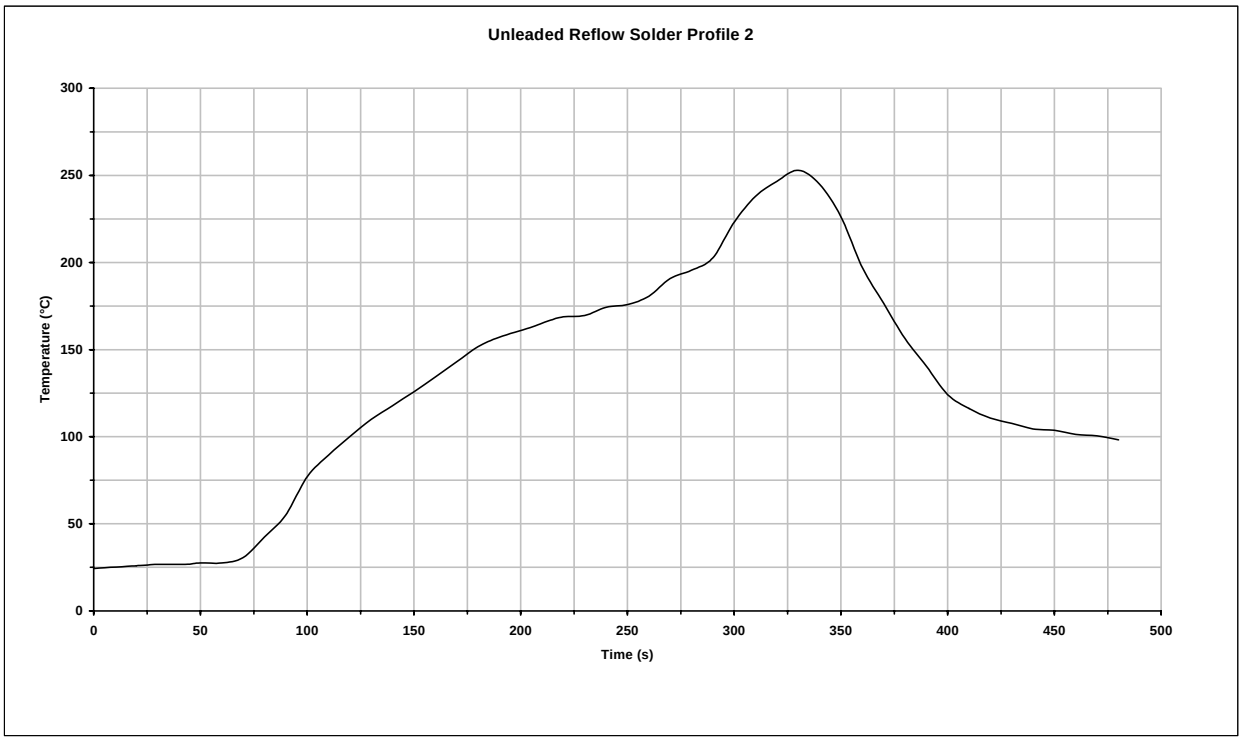


Figure 13.2: Typical Lead-Free Re-flow Solder Profile

Key features of the profile:

- Initial Ramp = 1-2.5°C/sec to 175°C±25°C equilibrium
- Equilibrium time = 60 to 180 seconds
- Ramp to Maximum temperature (250°C) = 3°C/sec max.
- Time above liquidus temperature (217°C): 45-90 seconds
- Device absolute maximum reflow temperature: 260°C

Devices will withstand the specified profile.

Lead-free devices will withstand up to 3 reflows to a maximum temperature of 260°C.

14 Product Reliability Tests

Die	Test Conditions	Specification	Sample Size
ESD	Human Body Model	JEDEC	30
Latch-up	±200mA	JEDEC	6
Early Life	125°C	48 – 168 hours	287
Hot Life Test	125°C	1000 hours	287 (41 FITs)

Package	Test Conditions	Specification	Sample Size
Moisture Sensitivity Precon JEDEC Level 3	(125°C 24 hours) 30°C/60%RH	192 hours five re-flow simulation cycles	308
Temperature Cycling	-65°C to +150°C	500 cycles	77 from Precon
AutoClave (Steam)	121°C at 100% RH	96 hours	77 from Precon
Temperature Humidity Bias	85°C/85% RH	1000 hours	77 from Precon
High Temperature Storage	150°C	1000 hours	77

15 Tape and Reel Information

Tape and reel is in accordance with EIA-481-2.

15.1 Tape Information

15.1.1 Tape Orientation

The general orientation of the BGA in the tape is as shown in Figure 15.1.

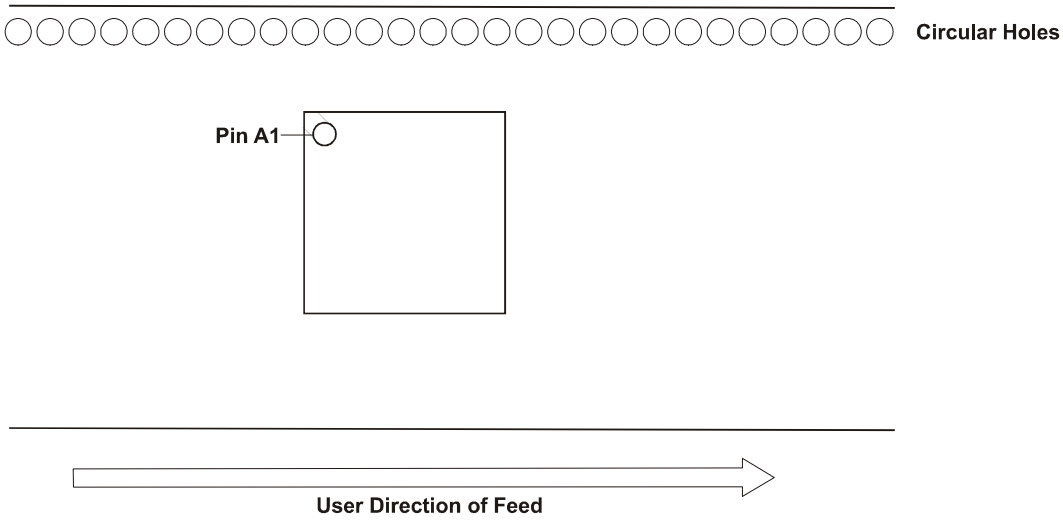
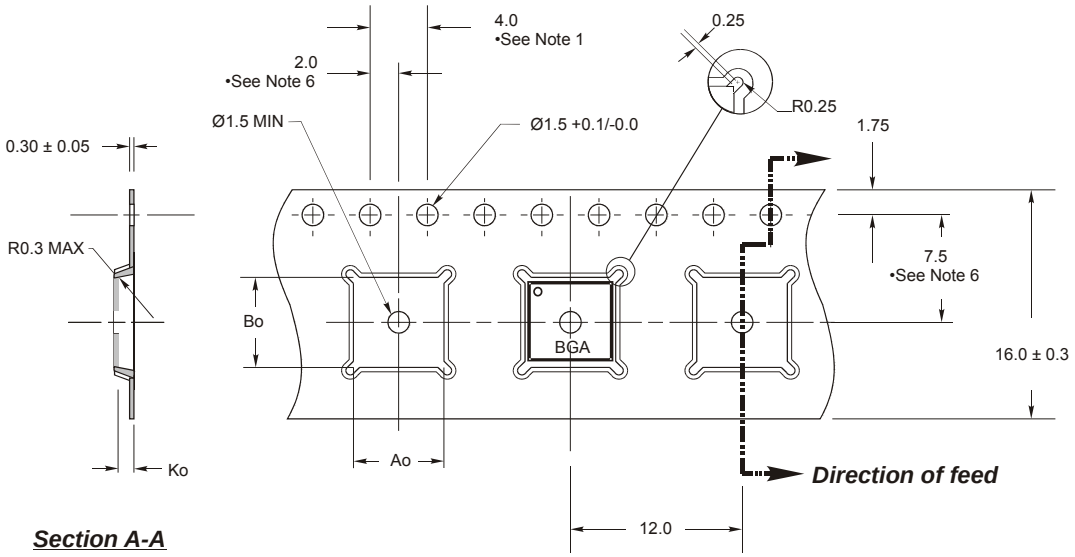


Figure 15.1: Tape and Reel Orientation

15.1.2 BGA Tape Dimensions

The diagram shown in Figure 15.2 outlines the dimensions of the tape used for 6mm x 6mm x 1mm VFBGA devices:



Notes:
1. 10 sprocket hole pitch cumulative tolerance ± 02.
2. Camber not to exceed 1mm in 100mm.
3. Material: PS + C.
4. Ao and Bo measured as indicated.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Ao = 6.3 mm
Bo = 6.3 mm
Ko = 1.1 mm

Figure 15.2: VFBGA Tape Dimensions

The cover tape has a total peel strength of 0.1N to 1.3N. The direction of the pull should be opposite the direction of the carrier tape such that the cover tape makes an angle of between 165° and 180° with the top of the carrier tape. The carrier and/or cover tape should be pulled with a velocity of 300±10mm during peeling.

Maximum component rotation inside the cavity is 10° in accordance with EIA-481-2. The cavity pitch tolerance (dimension P1) is ±0.1mm.

The reel is made of high impact injection molded polystyrene. The carrier tape is made of polystyrene with carbon. The cover tape is made of antistatic polyester film and an antistatic heat activated adhesive coating.

15.1.3 CSP Tape Dimensions

The diagram shown in Figure 15.3 outlines the dimensions of the tape used for 4mm x 4mm x 0.7mm CSP devices:

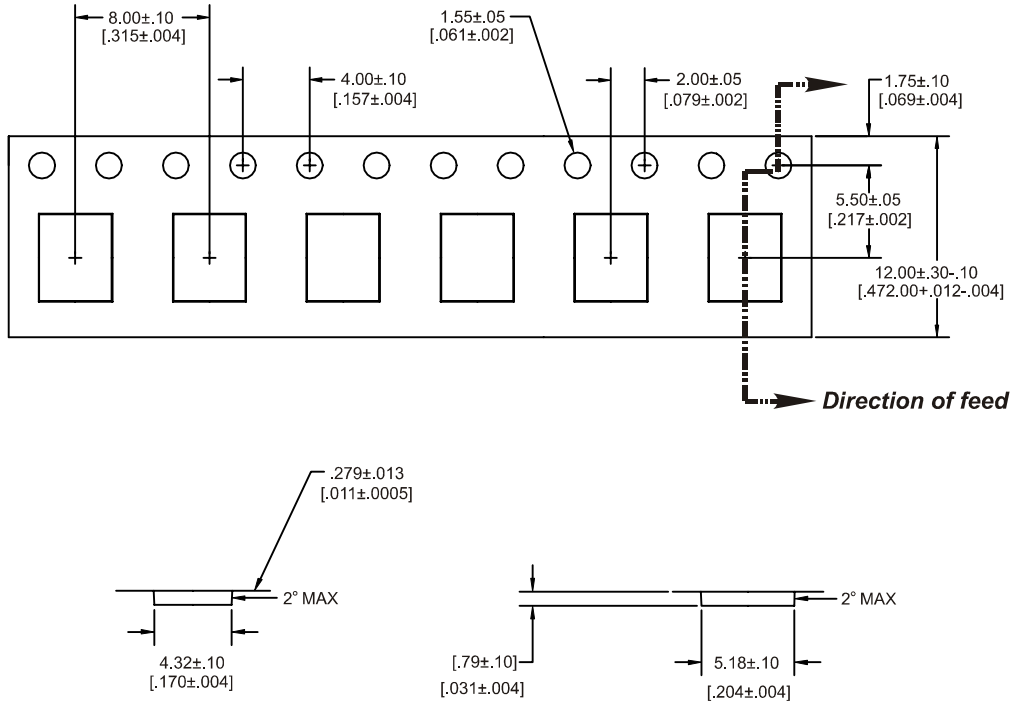


Figure 15.3: CSP Tape Dimensions

15.2 Reel Information

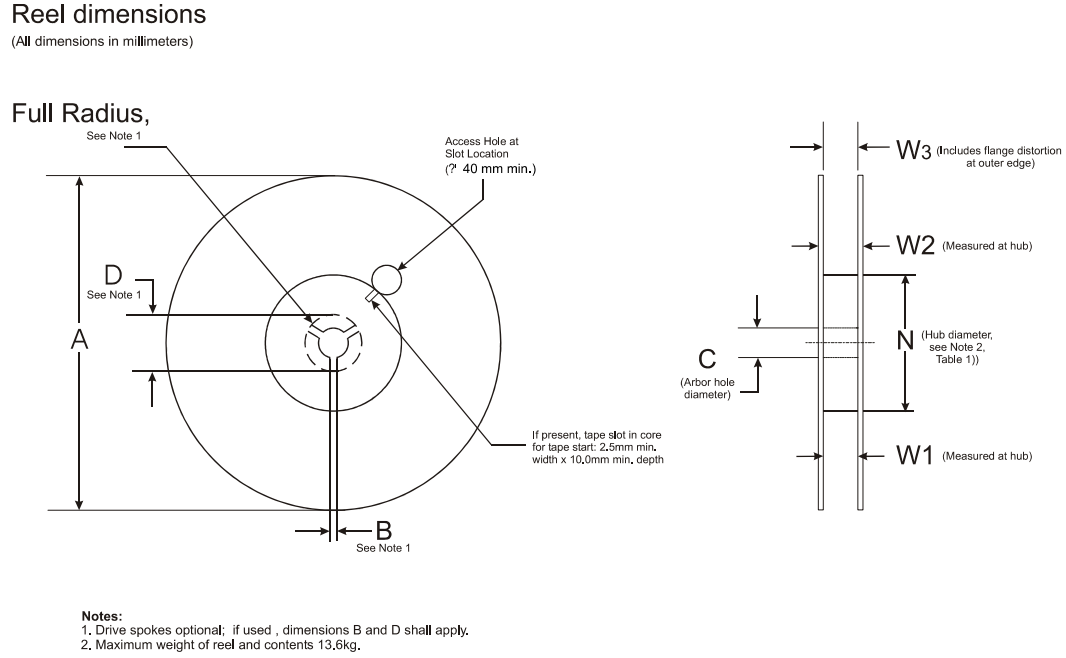


Figure 15.4: Reel Dimensions

Package Type	Tape Width	B Min	C	D Min	N Min	W1	W2 Max	W3
VFBGA	16mm	1.5mm	13.0+0.5/-0.2mm	20.2mm	50mm	16.4+2.0/-0.0mm	22.4mm	15.9mm Min 19.4mm Max
CSP	12mm	1.5mm	13.0+0.5/-0.2mm	20.2mm	102mm	12.8+0.6/-0.4mm	18.2mm	-

Table 15.1: Reel Dimensions

15.3 Dry Pack Information

The primary packed product is dry packed in accordance with Joint IPC / JEDEC J-STD-033.

All materials used in dry packing conform to EIA-541 and EIA-583.

Some illustrative views of reel dry packs are shown in Figure 15.5.

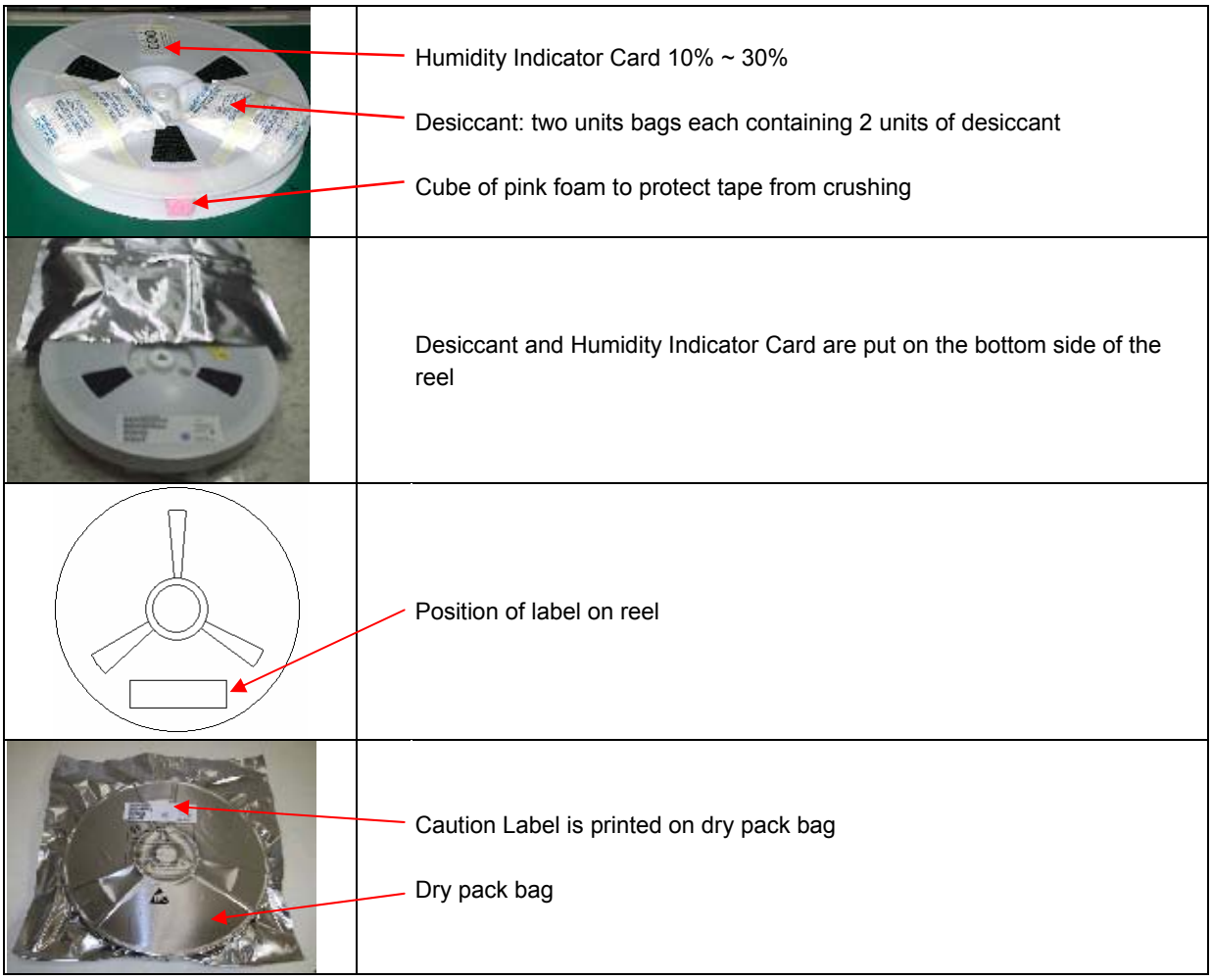


Figure 15.5: Tape and Reel Packaging

Devices shipped in dry-pack bags will withstand storage in normal environmental conditions, such as 30°C and 70% RH for a minimum of one year as long as the dry-pack bag has not become punctured. Humidity indicators inside the dry-pack bag will confirm this when the bag is opened.

15.3.1 Baking Conditions

Devices may, if necessary, be re-baked at 125°C for 24 hours. If devices are still on the reel, which cannot withstand such high temperatures, they should be baked at 45°C for 192 hours at relative humidity less than 5%.

Solder wettability of parts will be unaffected by three such bakes.

15.3.2 Product Information

Example product information labels are shown is Figure 15.6.

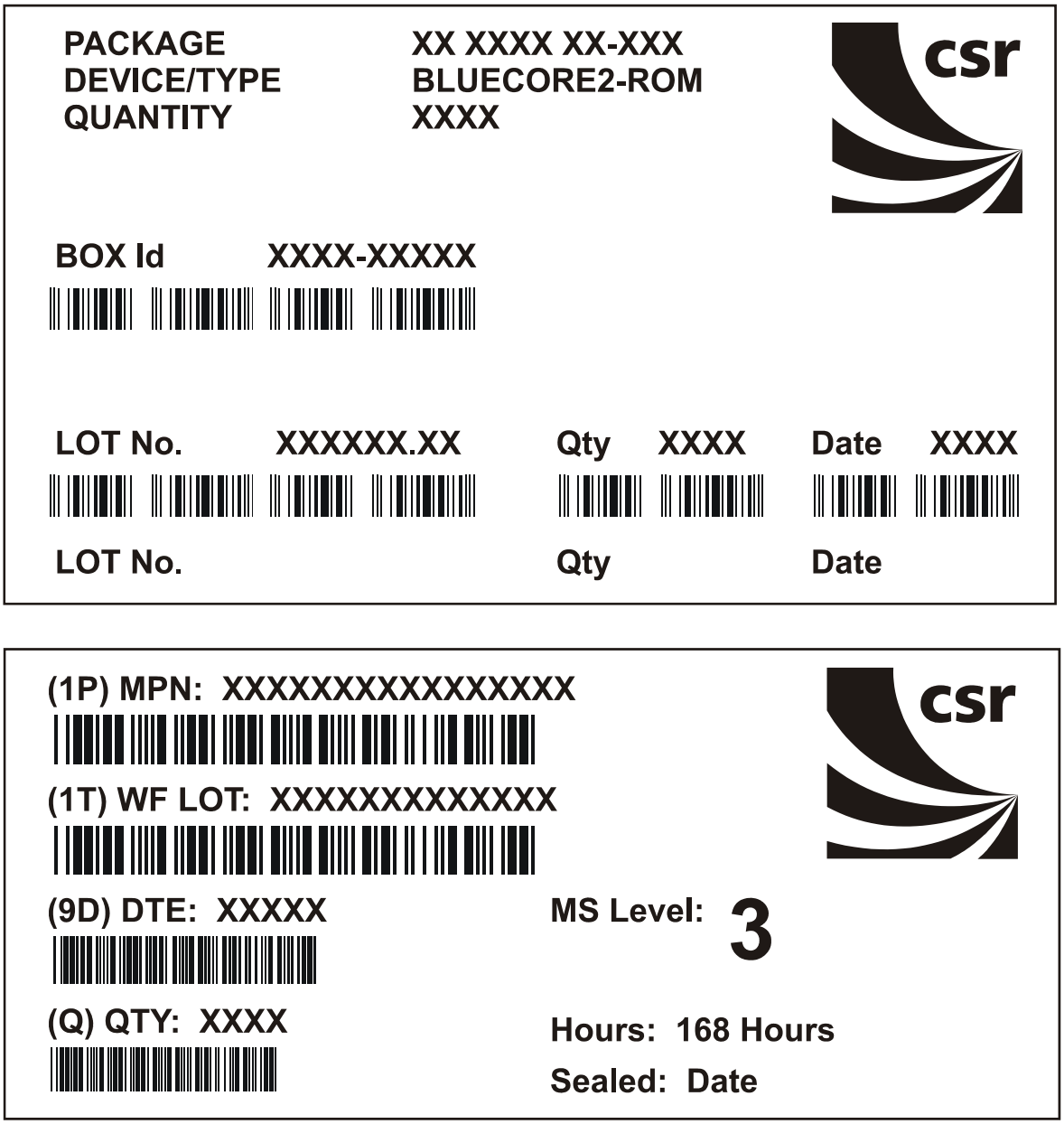


Figure 15.6: Product Information Labels

A product information label is placed on each reel, primary package and shipment package.

15.4 CSP Pack Information

Some illustrative views of reel dry packs are shown in Figure 15.5.

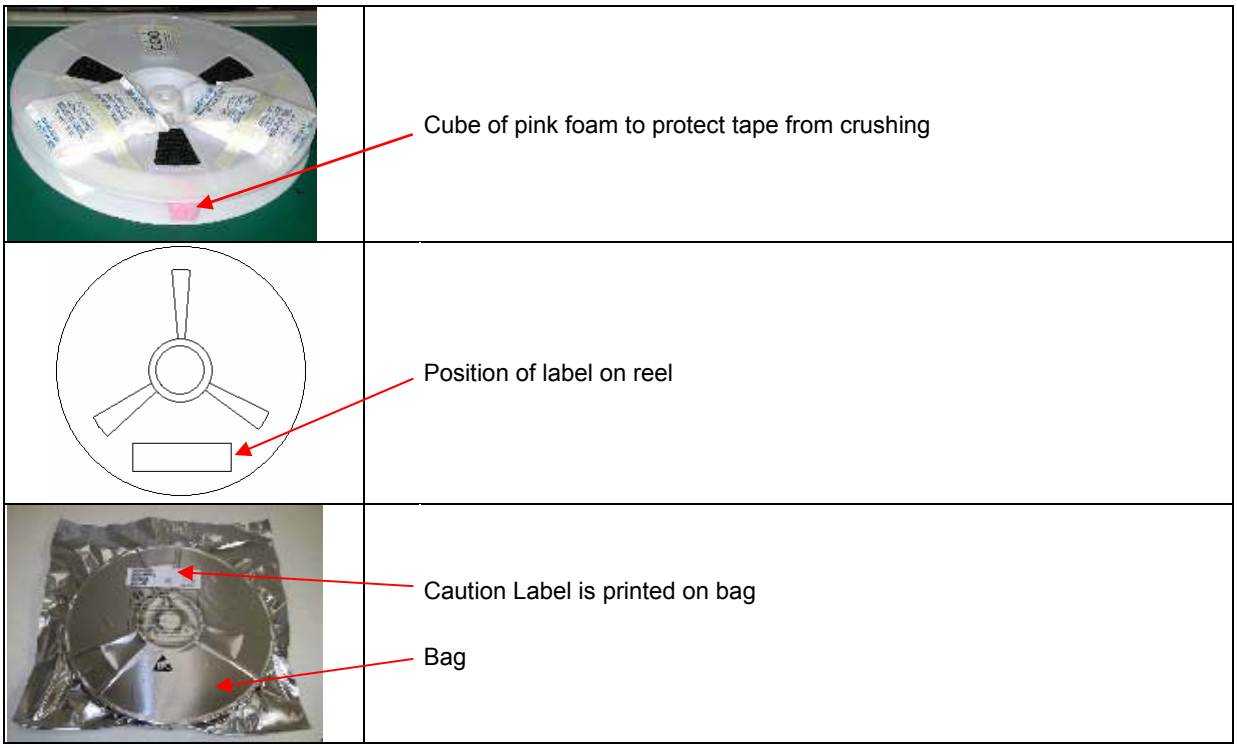


Figure 15.7: Tape and Reel Packaging

Packed in accordance with JEDEC MSL level 1.

15.4.1 Baking Conditions

No baking is required for these devices because they are qualified to JEDEC MSL level 1.

15.4.2 CSP Product Information

Example product information labels are shown is Figure 15.8.

Figure 15.8: CSP Product Information Labels

16 Ordering Information

16.1 BlueCore2-ROM

Interface Version	Package			Order Number
	Type	Size	Shipment Method	
UART and USB	84-Ball VFBGA	6x6x1mm	Tape and reel	BC213143AXX-EK-E4
	84-Ball VFBGA (Pb free)	6x6x1mm	Tape and reel	BC213143AXX-RK-E4
	47-Ball CSP (Pb free)	4x4x0.7mm	Tape and reel	BC213143AXX-XB-E4

Note:

XX denotes firmware type and firmware version status. These are determined on a customer and project basis.

Minimum Order Quantity: 2kpcs Taped and Reeled

17 Contact Information

CSR UK
Cambridge Science Park
Milton Road
Cambridge, CB4 0WH
United Kingdom
Tel: +44 (0) 1223 692 000
Fax: +44 (0) 1223 692 001
e-mail: sales@csr.com

CSR Denmark
Novi Science Park
Niels Jernes Vej 10
9220 Aalborg East
Denmark
Tel: +45 72 200 380
Fax: +45 96 354 599
e-mail: sales@csr.com

CSR Japan
CSR KK
9F Kojimachi KS Square 5-3-3,
Kojimachi,
Chiyoda-ku,
Tokyo 102-0083
Japan
Tel: +81-3-5276-2911
Fax: +81-3-5276-2915
e-mail: sales@csr.com

CSR Korea
Rm. 1111 Keumgang Venturetel,
#1108 Beesan-dong,
Dong An-ku, Anyang-city,
Kyunggi-do 431-050,
Korea
Tel: +82 31 389 0541
Fax : +82 31 389 0545
e-mail: sales@csr.com

CSR Singapore
Blk 5, Ang Mo Kio
Industrial Park 2A,
AMK Tech II, #07-08
Singapore 567760
Tel: +65 6484 2212
Fax: +65 6484 2219
e-mail: sales@csr.com

CSR Taiwan
Rm6A,6F, No. 118,
Hsing-Shan Rd.,
NeiHu, Taipei,
Taiwan, R.O.C.
Tel: +886 2 7721 5588
Fax: +886 2 7721 5589
e-mail: sales@csr.com

CSR U.S.
1651 N. Collins Blvd.
Suite 210
Richardson
TX75080
Tel: +1 (972) 238 2300
Fax: +1 (972) 231 1440
e-mail: sales@csr.com

To contact a CSR representative, go to http://www.csr.com/contacts.htm

18 Document References

Document	Reference
Specification of the Bluetooth system	v1.1, 22 February 2001 and v1.2, 05 November 2003
Universal Serial Bus Specification	v1.1, 23 September 1998
I^2C EEPROMS for Use with BlueCore	CSR document bcore-an-008Pa, October 2002
IA-481-2	16mm, 24mm, 32mm, 44mm and 56mm Embossed Carrier Taping of Surface Mount Components for Automatic Handling
EIA-541	Packaging Material Standards for ESD Sensitive Items
EIA-583	Packaging Material Standards for Electrostatic Discharge (ESD) Sensitive Items
IPC / JEDEC J-STD-033	Standard for Handling, Packing, Shipping and Use of Moisture / Reflow Sensitive Surface Mount Devices
TDK Multilayer Balun Specification P/N: HHM1517 for Bluetooth and EEE802.11b/g	Jun. / 2003 Ver.12 TDK Corporation

Acronyms and Definitions

Term	Definition
BlueCore™	Group term for CSR's range of Bluetooth chips.
Bluetooth®	Set of technologies providing audio and data transfer over short-range radio connections
ACL	Asynchronous Connection-Less. A Bluetooth data packet.
AC	Alternating Current
ADC	Analogue to Digital Converter
AGC	Automatic Gain Control
A-law	Audio encoding standard
API	Application Programming Interface
ASIC	Application Specific Integrated Circuit
BCSP	BlueCore™ Serial Protocol
BER	Bit Error Rate. A measure of the quality of a link
BGA	Ball Grid Array
BIST	Built-In Self-Test
BOM	Bill of Materials. Component part list and costing for a product
BMC	Burst Mode Controller
C/I	Carrier Over Interferer
CMOS	Complementary Metal Oxide Semiconductor
CODEC	Coder Decoder
CPU	Central Processing Unit
CQDDR	Channel Quality Driven Data Rate
CSP	Chip Scale Package
CSR	Cambridge Silicon Radio
CTS	Clear to Send
CVSD	Continuous Variable Slope Delta Modulation
DAC	Digital to Analogue Converter
dBm	Decibels relative to 1mW
DC	Direct Current
DFU	Device Firmware Upgrade
FSK	Frequency Shift Keying
GCI	General Circuit Interface. Standard synchronous 2B+D ISDN timing interface
GSM	Global System for Mobile communications
HCI	Host Controller Interface
IQ Modulation	In-Phase and Quadrature Modulation
IF	Intermediate Frequency
ISDN	Integrated Services Digital Network
ISM	Industrial, Scientific and Medical
ksamples/s	kilosamples per second
L2CAP	Logical Link Control and Adaptation Protocol (protocol layer)
LC	Link Controller
LCD	Liquid Crystal Display
LGA	Land Grid Array
LNA	Low Noise Amplifier

LSB	Least-Significant Bit
μ-law	Audio Encoding Standard
MMU	Memory Management Unit
MISO	Master In Serial Out
OHCI	Open Host Controller Interface
PA	Power Amplifier
PCB	Printed Circuit Board
PCM	Pulse Code Modulation. Refers to digital voice data
PIO	Parallel Input Output
PLL	Phase Lock Loop
ppm	parts per million
PS Key	Persistent Store Key
RAM	Random Access Memory
REF	Reference. Represents dimension for reference use only.
RF	Radio Frequency
RFCOMM	Protocol layer providing serial port emulation over L2CAP
RISC	Reduced Instruction Set Computer
rms	root mean squared
ROM	Read Only Memory
ROHS	The Restriction of Hazardous Substances in Electrical and Electronic Equipment Directive (2002/95/EC)
RSSI	Receive Signal Strength Indication
RTS	Ready To Send
RX	Receive or Receiver
SCO	Synchronous Connection-Oriented. Voice oriented Bluetooth packet
SDK	Software Development Kit
SDP	Service Discovery Protocol
SIG	Special Interest Group
SOC	System On Chip
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSL	Secure Sockets Layer
SUT	System Under Test
SW	Software
TBD	To Be Defined
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus or Upper Side Band (depending on context)
VCO	Voltage Controlled Oscillator
VFBGA	Very Fine Ball Grid Array
VM	Virtual Machine
W-CDMA	Wideband Code Division Multiple Access

Record of Changes

Date	Revision	Reason for Change
December 2002	a	Original publication for BlueCore2-ROM.
February 2003	b	Added PCM CODEC and crystal information.
March 2003	c	Added min and max data. Document status changed to Production Information.
June 2003	d	Device terminal functions for CSP package added. Temperature range extended to -40°C to +105°C.
July 2003	e	Added additional data to Radio Characteristics Section.
August 2003	f	Corrected data alignment error in +20°C data table.
September 2003	g	Added additional blocking information and ROHS statement.
September 2003	h	CSP tape and reel information added.
February 2004	i	Amendment to specification v1.1 and v1.2 compliant statement.
February 2004	j	Fixed Figure 9.40 so that .pdf shows timing parameters.
19 October 2004	k	Amended drift rate data in section 5.

BlueCore™2-ROM

Product Data Book

BC213143A-LF-001Pk

October 2004