Device Features

- Low power 1.8V operation
- Bluetooth v1.1 and v1.2 specification compliant
- Small footprint in 96 ball VFBGA LGA and LFBGA packages (6x6mm, 8 x 8mm and 10 x 10mm)
- Fully qualified Bluetooth component
- 0.18µm CMOS technology
- Full speed Bluetooth operation with full piconet support
- Support for 8Mbit external flash
- Minimum external components

BlueCore™2 External

Single Chip Bluetooth® System

Production Information Data Sheet for:

BC212015 (USB and UART version)

August 2004

General Description

BlueCore2-External is a single chip radio and baseband IC for Bluetooth 2.4GHz systems. It is implemented in 0.18µm CMOS technology.

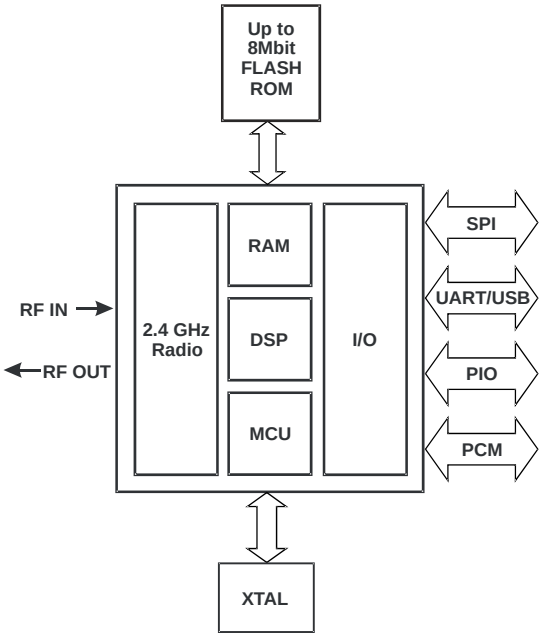
When used with external flash containing the CSR Bluetooth software stack, it provides a fully compliant Bluetooth system for data and voice communications.

Applications

- PCs
- Cellular Handsets
- Cordless Headsets
- Personal Digital Assistants (PDAs)
- Computer Accessories (Compact flash Cards, PCMCIA Cards, SD Cards and USB Dongles)
- Mice, Keyboards and Joysticks
- Digital Cameras and Camcorders

BlueCore2-External has been designed to reduce the number of external RF components required, which ensures module production costs are minimised.

The device incorporates auto calibration and built-in self-test routines to simplify development, type approval and production test. All hardware and device firmware is fully compliant with the Bluetooth specification v1.1 and v1.2.



BlueCore2 External Block Diagram

Bluetooth Qualified

BlueCore™2-External Product Data Sheet

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Status of Information

The status of this Data Sheet is Production Information.

CSR Product Data Sheets progress according to the following format:

Advance Information:

Information for designers concerning a CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All detailed specifications, including pinouts and electrical specifications, may be changed by CSR without notice.

Pre-Production Information:

Final pinout and mechanical dimension specifications. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

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Production Information:

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Production Data Sheets supersede all previous document versions.

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CSR reserves the right to make technical changes to its products as part of its development programme.

While every care has been taken to ensure the accuracy of the contents of this document, CSR cannot accept responsibility for any errors.

1 Key Features

Radio

- Operation with common TX/RX terminals simplifies external matching circuitry and eliminates external antenna switch
- Extensive built-in self-test minimises production test time
- No external trimming is required in production
- Full RF reference designs are available

Transmitter

- Up to +6dBm RF transmit power with level control from the on-chip 6-bit DAC over a dynamic range greater than 30dB
- Supports Class 2 and Class 3 radios without the need for an external power amplifier or TX/RX switch
- Supports Class 1 radios with an external power amplifier provided by a power control terminal controlled by an internal 8-bit voltage DAC and an external RF TX/RX switch

Receiver

- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Digitised RSSI available in real time over the HCI interface
- Fast AGC for enhanced dynamic range

Synthesiser

- Fully integrated synthesiser; no external VCO varactor diode or resonator
- Compatible with crystals between 8 and 32MHz (in multiples of 250kHz) or external clock

Auxiliary Features

- Crystal oscillator with built-in digital trimming
- Power management includes digital shut down and wake up commands and an integrated low power oscillator for ultra-low Park/Sniff/Hold mode power consumption
- Device can be used with an external Master oscillator and provides a clock request signal to control external clock source
- Uncommitted 8-bit ADC and 8-bit DAC are available to application programs

Baseband and Software

- External 8Mbit flash for complete system solution and application flexibility
- 32kbyte on-chip RAM allows full speed Bluetooth data transfer, mixed voice and data, plus full 7 slave piconet operation
- Dedicated logic for forward error correction, header error control, access code correlation, demodulation, cyclic redundancy check, encryption bitstream generation, whitening and transmit pulse shaping
- Transcoders for A-law, μ-law and linear voice from host; A-law, μ-law and CVSD voice over air

Physical Interfaces

- Synchronous serial interface up to 4Mbaud
- UART interface with programmable baud rate up to 1.5Mbaud
- Full speed USB interface supports OHCI and UHCI host interfaces. Compliant with USB v1.1
- Synchronous bi-directional serial programmable audio interface
- Optional I^2CTM compatible interface

Bluetooth Stack Running on Internal Microcontroller

CSR's Bluetooth Protocol Stack runs on-chip in a variety of configurations:

- Standard HCI (UART or USB)
- Fully embedded to RFCOMM, thus reducing host CPU load

Package Options

- 96-ball VFBGA 8 x 8 x 1.0mm 0.65mm pitch
- 96-ball VFBGA 6 x 6 x 1.0mm 0.50mm pitch
- 96-ball LGA 6 x 6 x 0.65mm 0.50mm pitch
- 96-ball LFBGA 10 x 10 x 1.4mm 0.80mm pitch

2 Device Pinout Diagram

Orientation from top of device

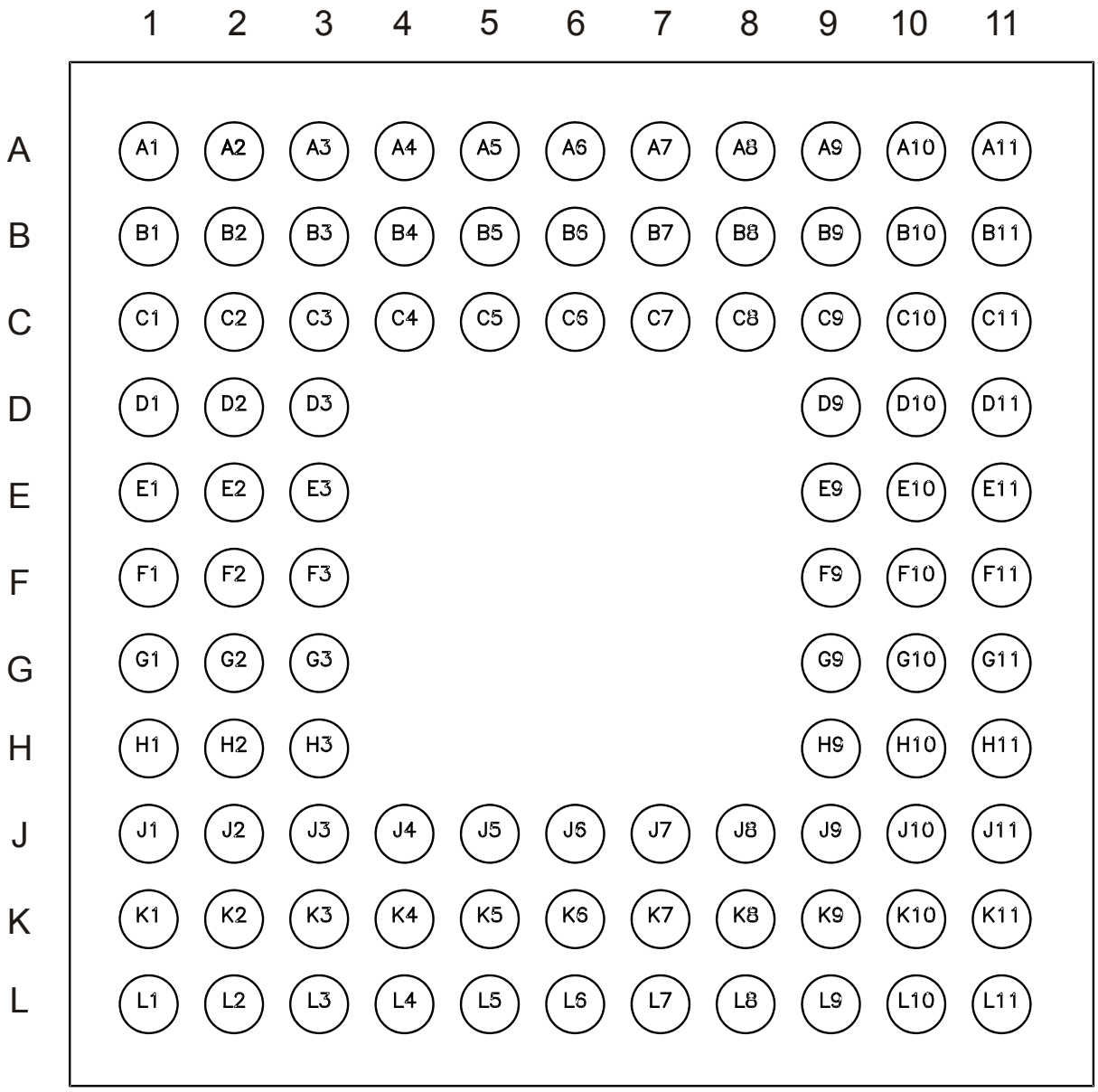


Figure 2.1: BlueCore2-External Device Pinout Diagram

Notes:

Device pinout diagram is the same for:

10 x 10 x 1.4mm LFBGA package (BN)

8 x 8 x 1mm VFBGA package (DN and QN)

6 x 6 x 1mm VFBGA package (EN and RN)

6 x 6 x 0.6mm LGA package (LN)

3 Device Terminal Functions

Radio	Ball	Pad Type	Description
RF_IN	E1	Analogue	Single ended receiver input
PIO[0]/RXEN	C1	Bi-directional with weak internal pull-up/down	Control output for external LNA (if fitted)
PIO[1]/TXEN	C2	Bi-directional with weak internal pull-up/down	Control output for external PA Class 1 applications only
TX_A	G1	Analogue	Transmitter output/Switched Receiver input
TX_B	F1	Analogue	Complement of TX_A
AUX_DAC	D2	Analogue	Voltage DAC output

Synthesiser and Oscillator	Ball	Pad Type	Description
XTAL_IN	L1	Analogue	For crystal or external clock input
XTAL_OUT	L2	Analogue	Drive for crystal
LOOP_FILTER	J1	Analogue	Connection to external PLL loop filter

External Memory Port	Ball	Pad Type	Description
REB	D10	CMOS output, tristate with internal weak pull-up	Read enable for external memory (active low)
WEB	E10	CMOS output, tristate with internal weak pull-up	Write enable for external memory (active low)
CSB	C10	CMOS output, tristate with internal weak pull-up	Chip select for external memory (active low)

Address Lines	Ball	Pad Type	Description
A[0]	D9	CMOS output, tristate	Address line
A[1]	E9	CMOS output, tristate	Address line
A[2]	E11	CMOS output, tristate	Address line
A[3]	F9	CMOS output, tristate	Address line
A[4]	F10	CMOS output, tristate	Address line
A[5]	F11	CMOS output, tristate	Address line
A[6]	G9	CMOS output, tristate	Address line
A[7]	G10	CMOS output, tristate	Address line
A[8]	G11	CMOS output, tristate	Address line
A[9]	H9	CMOS output, tristate	Address line
A[10]	H10	CMOS output, tristate	Address line
A[11]	H11	CMOS output, tristate	Address line
A[12]	J8	CMOS output, tristate	Address line
A[13]	J9	CMOS output, tristate	Address line
A[14]	J10	CMOS output, tristate	Address line
A[15]	J11	CMOS output, tristate	Address line
A[16]	K9	CMOS output, tristate	Address line
A[17]	K10	CMOS output, tristate	Address line
A[18]	K11	CMOS output, tristate	Address line

Data Bus	Ball	Pad Type	Description
D[0]	K8	Bi-directional with weak internal pull-down	Data line
D[1]	L9	Bi-directional with weak internal pull-down	Data line
D[2]	L10	Bi-directional with weak internal pull-down	Data line
D[3]	L11	Bi-directional with weak internal pull-down	Data line
D[4]	L8	Bi-directional with weak internal pull-down	Data line
D[5]	J7	Bi-directional with weak internal pull-down	Data line
D[6]	K7	Bi-directional with weak internal pull-down	Data line
D[7]	L7	Bi-directional with weak internal pull-down	Data line
D[8]	J6	Bi-directional with weak internal pull-down	Data line
D[9]	K6	Bi-directional with weak internal pull-down	Data line
D[10]	L6	Bi-directional with weak internal pull-down	Data line
D[11]	J5	Bi-directional with weak internal pull-down	Data line
D[12]	K5	Bi-directional with weak internal pull-down	Data line
D[13]	L5	Bi-directional with weak internal pull-down	Data line
D[14]	J4	Bi-directional with weak internal pull-down	Data line
D[15]	K4	Bi-directional with weak internal pull-down	Data line

PCM Interface	Ball	Pad Type	Description
PCM_OUT	B9	CMOS output, tristate with internal weak pull-down	Synchronous data output
PCM_IN	B10	CMOS input, with internal weak pull-down	Synchronous data input
PCM_SYNC	B11	Bi-directional with weak internal pull-down	Synchronous data SYNC
PCM_CLK	B8	Bi-directional with weak internal pull-down	Synchronous data clock

USB and UART	Ball	Pad Type	Description
UART_TX	C8	CMOS output	UART data output active high
UART_RX	C9	CMOS input with weak internal pull-down	UART data input active high
UART_RTS	B7	CMOS output, tristate with internal pull-up	UART request to send active low
UART_CTS	B6	CMOS input with weak internal pull-down	UART clear to send active low
USB_D+ (1) (2)	A7	Bi-directional	USB data plus
USB_D- (1) (2)	A6	Bi-directional	USB data minus

Test and Debug	Ball	Pad Type	Description
RESET	F3	CMOS input with weak internal pull-down	Reset if high. Input debounced so must be high for >5ms to cause a reset
SPI_CSB	A4	CMOS input with weak internal pull-up	Chip select for Synchronous Serial Interface active low
SPI_CLK	B5	CMOS input with weak internal pull-down	Serial Peripheral Interface clock
SPI_MOSI	A5	CMOS input with weak internal pull-down	Serial Peripheral Interface data input
SPI_MISO	B4	CMOS output, tristate with weak internal pull-down	Serial Peripheral Interface data output
TEST_EN	G3	CMOS input with strong internal pull-down	For test purposes only (leave unconnected)

Notes:

(1) USB functions are available on BC212015 only.

(2) If unused USB_D+ and USB_D- should be connected to ground

PIO Port[1]	Ball	Pad Type	Description
PIO[2]/ USB_PULL_UP[2] [3]	B3	Bi-directional with programmable weak internal pull-up/down	PIO or USB pull-up (via 1.5kΩ resistor to USB_D+)
PIO[3]/USB_WAKE_UP/RAM_CSB[2] [3]	B2	Bi-directional with programmable weak internal pull-up/down	PIO or output goes high to wake up PC when in USB mode or external RAM chip select
PIO[4]/USB_ON[2] [3]	B1	Bi-directional with programmable weak internal pull-up/down	PIO or USB on (input senses when VBUS is high, wakes BlueCore2-External)
PIO[5]/USB_DETACH[2] [3]	A3	Bi-directional with programmable weak internal pull-up/down	PIO line or chip detaches from USB when this input is high
PIO[6]/CLK_REQ	C3	Bi-directional with programmable weak internal pull-up/down	PIO line or clock request output to enable external clock for external clock line
PIO[7]	E3	Bi-directional with programmable weak internal pull-up/down	Programmable input/output line
PIO[8]	D3	Bi-directional with programmable weak internal pull-up/down	Programmable input/output line
PIO[9]	C4	Bi-directional with programmable weak internal pull-up/down	Programmable input/output line
PIO[10]	C5	Bi-directional with programmable weak internal pull-up/down	Programmable input/output line
PIO[11]	C6	Bi-directional with programmable weak internal pull-up/down	Programmable input/output line
AIO[0]	K3	Bi-directional	Programmable input/output line[4]
AIO[1]	L4	Bi-directional	Programmable input/output line[4]
AIO[2]	J3	Bi-directional	Programmable input/output line[4]

Notes:

(1) All PIOs are configured as inputs with weak pull-downs at reset.

(2) USB functions are available on BC212015 only.

(3) USB functions can be software mapped to any PIO terminal.

(4) Unused AIO pins may be left unconnected

Power Supplies and Control	Ball	Pad Type	Description
VDD_RADIO	D1 H3	VDD	Positive supply connection for RF circuitry
VDD_VCO	H1	VDD	Positive supply for VCO and synthesiser circuitry
VDD_ANA	K1	VDD	Positive supply for analogue circuitry
VDD_CORE	A8	VDD	Positive supply for internal digital circuitry
VDD_PIO	A1	VDD	Positive supply for PIO and AUX DAC
VDD_PADS	A10	VDD	Positive supply for all other input/output
VDD_MEM	D11	VDD	Positive supply for external memory port and AIO
VSS_RADIO	E2 F2 G2	VSS	Ground connections for RF circuitry
VSS_VCO	J2 H2	VSS	Ground connections for VCO and synthesiser
VSS_ANA	L3 K2	VSS	Ground connections for analogue circuitry
VSS_CORE	A9	VSS	Ground connection for internal digital circuitry
VSS_PIO	A2	VSS	Ground connection for PIO and AUX DAC
VSS_PADS	A11	VSS	Ground connection for input/output except memory port
VSS_MEM	C11	VSS	Ground connection for external memory port
VSS	C7	VSS	Ground connection for internal package shield

4 Electrical Characteristics

Absolute Maximum Ratings		
Rating	**Min**	**Max**
Storage Temperature	-40°C	+150°C
Supply Voltage: VDD_RADIO, VDD_VCO, VDD_ANA, VDD_CORE	-0.40V	1.90V
Supply Voltage: VDD_PADS, VDD_PIO, VDD_MEM	-0.40V	3.60V

Recommended Operating Conditions		
Operating Condition	**Min**	**Max**
Operating Temperature Range(1)	-40°C	105°C
Supply Voltage: VDD_RADIO, VDD_VCO, VDD_ANA, VDD_CORE	1.70V	1.90V
Supply Voltage: VDD_PADS, VDD_PIO, VDD_MEM	1.70V	3.60V

Note:

(1) The device functions across this range. See section 5, Radio Characteristics, for guaranteed performance over temperature.

Input/Output Terminal Characteristics				
Digital Terminals	**Min**	**Typ**	**Max**	**Unit**
Input Voltage				
V_{IL} input logic level low (VDD=3.0V)	-0.4		+0.8	V
(VDD=1.8V)	-0.4	-	+0.4	V
V_{IH} input logic level high	0.7VDD	-	VDD+0.4	V
Output Voltage				
V_{OL} output logic level low, (I_O = 4.0mA), VDD=3.0V	-	-	0.2	V
V_{OL} output logic level low, (I_O = 4.0mA), VDD=1.8V	-	-	0.4	V
V_{OH} output logic level high, (I_O = -4.0mA), VDD=3.0V	VDD-0.2	-	-	V
V_{OH} output logic level high, (I_O = -4.0mA), VDD=1.8V	VDD-0.4	-	-	V
Input and Tristate Current with:				
Strong pull-up	-100	-20	-10	µA
Strong pull-down	+10	+20	+100	µA
Weak pull-up	-5	-1	0	µA
Weak pull-down	0.2	+1	+5	µA
I/O pad leakage current	-1	0	+1	µA
C_I Input Capacitance	2.5	-	10	pF
USB Terminals	**Min**	**Typ**	**Max**	**Unit**
Input threshold				
V_{IL} input logic level low	-	-	0.3VDD_PADS	V
V_{IH} input logic level high (VDD_PADS=3.46V)[1]	0.7VDD_PADS	-	-	V
Input leakage current				
VSS_PADS< VIN< VDD_PADS[2]	-1	-	1	µA
C_I Input capacitance	2.5	-	10	pF
Output levels to correctly terminated USB Cable				
V_{OL} output logic level low	0	-	0.2	V
V_{OH} output logic level high	2.8	-	VDD_PADS	V

Notes:

VDD_CORE, VDD_RADIO, VDD_VCO and VDD_ANA are at 1.8V unless shown otherwise

VDD_PADS, VDD_PIO and VDD_MEM are at 3.0V unless shown otherwise

Current drawn into a pin is defined as positive; current supplied out of a pin is defined as negative.

(1) 3.46V = 3.3V+5%

(2) Internal USB pull-up disabled.

Input/Output Terminal Characteristics (Continued)				
Auxiliary DAC	**Min**	**Typ**	**Max**	**Unit**
Resolution	-	-	8	Bits
Average output step size(1)	12.5	14.5	17.0	mV
Output Voltage		monotonic(1)		
Voltage range (I_O=0mA)	VSS_PIO	-	VDD_PIO	V
Current range	-10	-	+0.1	mA
Minimum output voltage (I_O=100µA)	0	-	0.2	V
Maximum output voltage (I_O=10mA)	VDD_PIO-0.3	-	VDD_PIO	µV
High Impedance leakage current	-1	-	+1	µA
Offset	-220	-	+120	mV
Integral non-linearity(1)	-2	-	+2	LSB
Settling time (50pF load)	-	-	5	µs
Crystal Oscillator	**Min**	**Typ**	**Max**	**Unit**
Crystal frequency(2)	8.0	-	32.0	MHz
Digital trim range(3)	5	6.2	8	pF
Trim step size(3)	-	0.1	-	pF
Transconductance	2.0	-	-	mS
Negative resistance(4)	870	1500	2400	Ω
Power-on Reset	**Min**	**Typ**	**Max**	**Unit**
VDD falling threshold	1.40	1.50	1.60	V
VDD rising threshold	1.50	1.60	1.70	V
Hysteresis	0.05	0.10	0.15	V

Notes:

VDD_CORE, VDD_RADIO, VDD_VCO and VDD_ANA are at 1.8V unless shown otherwise

VDD_PADS, VDD_PIO and VDD_MEM are at 3.0V unless shown otherwise

The same setting of the digital trim is applied to both XTAL_IN and XTAL_OUT.

Current drawn into a pin is defined as positive, current supplied out of a pin is defined as negative.

(1) Specified for output voltage between 0.2V and VDD_PIO -0.2V

(2) Integer multiple of 250kHz.

(3) The difference between the internal capacitance at minimum and maximum settings of the internal digital trim.

(4) XTAL frequency = 16MHz; XTAL C0 = 0.75pF; XTAL load capacitance = 8.5pF

Input/Output Terminal Characteristics (Continued)					
Auxiliary ADC		**Min**	**Typ**	**Max**	**Unit**
Resolution		-	-	8	Bits
Input voltage range (LSB size = VDD_ANA/255)		0	-	VDD_ANA	V
Accuracy	INL	-1	-	1	LSB
(Guaranteed monotonic)	DNL	0	-	1	LSB
Offset		-1	-	1	LSB
Gain Error		-0.8	-	0.8	%
Input Bandwidth		-	100	-	kHz
Conversion time		-	2.5	-	µs
Sample rate(1)		-	-	700	Samples/s

Note:

(1) Access of ADC is through VM function; therefore, sample rate given is achieved as part of this function.

Average Current Consumption[1]		
VDD=1.8V Temperature = 20°C		
Mode	**Avg**	**Unit**
SCO connection HV3 (40ms interval Sniff Mode) (Slave)	26.0	mA
SCO connection HV3 (40ms interval Sniff Mode) (Master)	26.0	mA
SCO connection HV1 (Slave)	53.0	mA
SCO connection HV1 (Master)	53.0	mA
ACL data transfer 115.2kbps UART (Master)	15.5	mA
ACL data transfer 720kbps USB (Slave)	53.0	mA
ACL data transfer 720kbps USB (Master)	53.0	mA
ACL connection, Sniff Mode 40ms interval, 38.4kbps UART	4.0	mA
ACL connection, Sniff Mode 1.28s interval, 38.4kbps UART	0.5	mA
Parked Slave, 1.28s beacon interval, 38.4kbps UART	0.6	mA
Standby Mode (Connected to host, no RF activity)	0.047	mA

Peak Current Consumption[1]			
VDD=1.7V to 1.9V Temperature = 20°C			
Mode	**Typ**	**Max**[2]	**Unit**
Peak RF current during TX burst (+6 dBm)	65.0	80.0	mA
Peak RF current during TX burst (0 dBm)	57.0	70.0	mA
Peak RF current during RX burst (-85 dBm)	47.0	70.0	mA

Deep Sleep Leakage Current			
VDD=1.7V to 1.9V Temperature = 20°C			
Mode	**Typ**	**Max**[2]	**Unit**
Deep Sleep	20.0	50.0	µA

Notes:

(1) Current consumption is the sum of both BC212015B and the flash.

(2) Over process and voltage.

These results are correct only for BlueCore2-External version B running version 14.x firmware.

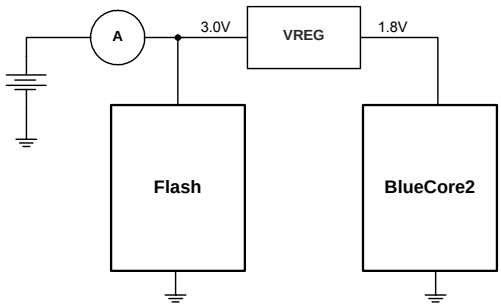


Figure 4.1: Current Measurement Circuit

5 Radio Characteristics

All radio characteristics were measured using the application circuit shown in Figure 10.1 but with the RF filter removed. This circuit and associated RF board layout is correct for the 8 × 8mm package. Other package types have slightly different RF impedances (see 9.1, RF Ports); therefore, they need slightly different matching.

BlueCore2-External meets the Bluetooth specification v1.1 and v1.2 when used in a suitable application circuit between -40°C and +85°C.

Radio Characteristics	**VDD = 1.8V**	**Temperature = +20°C**				
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER	2.402	-	-83	-80	≤-70	dBm
	2.441	-	-85	-82		dBm
	2.480	-	-85	-82		dBm
Maximum received signal at 0.1% BER	2.402	0	-	-	≥-20	dBm
	2.441	0	-	-		dBm
	2.480	0	-	-		dBm
RF transmit power(1)	2.402	3.0	6.0	-	-6to +4(2)	dBm
	2.441	3.0	6.0	-		dBm
	2.480	3.0	6.0	-		dBm
Initial carrier frequency tolerance	2.402	-	12	75	±75	kHz
	2.441	-	10	75		kHz
	2.480	-	9	75		kHz
20dB bandwidth for modulated carrier	2.402	-	879	1000	≤1000	kHz
	2.441	-	816	1000		kHz
	2.480	-	819	1000		kHz
Drift (single slot packet)	2.402	-	-	25	≤25	kHz
	2.441	-	-	25		kHz
	2.480	-	-	25		kHz
Drift (five slot packet)	2.402	-	-	40	≤40	kHz
	2.441	-	-	40		kHz
	2.480	-	-	40		kHz
Drift Rate	2.402	-	-	20	20	kHz/50µs
	2.441	-	-	20		kHz/50µs
	2.480	-	-	20		kHz/50µs
RF power control range		16	35	-	≥16	dB
RF power range control resolution		-	1.8	-	-	dB

Notes:

(1) BlueCore2-External firmware maintains the transmit power to be within the Bluetooth specification v1.1 and v1.2 limits.

(2) Class 2 RF transmit power range, Bluetooth specification v1.1 and v1.2

Radio Characteristics	VDD = 1.8V	Temperature = +20°C				
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
$\Delta f1_{avg}$ "Maximum Modulation"	2.402	140	165	175	140<$\Delta f1_{avg}$<175	kHz
	2.441	140	165	175		kHz
	2.480	140	165	175		kHz
$\Delta f2_{max}$ "Minimum Modulation"	2.402	115	150	-	115	kHz
	2.441	115	150	-		kHz
	2.480	115	150	-		kHz
C/I co-channel		-	10	11	≤11	dB
Adjacent channel selectivity C/I $F=F_0+1MHz$ (1) (3)		-	-4	0	≤0	dB
Adjacent channel selectivity C/I $F=F_0-1MHz$ (1) (3)		-	-4	0	≤0	dB
Adjacent channel selectivity C/I $F=F_0+2MHz$ (1) (3)		-	-35	-30	≤-30	dB
Adjacent channel selectivity C/I $F=F_0-2MHz$ (1) (3)		-	-21	-20	≤-20	dB
Adjacent channel selectivity C/I $F\geq F_0+3MHz$ (1) (3)		-	-45	-	≤-40	dB
Adjacent channel selectivity C/I $F\leq F_0-5MHz$ (1) (3)		-	-45	-	≤-40	dB
Adjacent channel selectivity C/I $F=F_{Image}$ (1) (3)		-	-18	-9	≤-9	dB
Adjacent channel transmit power $F=F_0\pm2MHz$ (2) (3)		-	-35	-20	≤-20	dBc
Adjacent channel transmit power $F=F_0\pm3MHz$ (2) (3)		-	-55	-40	≤-40	dBc

Notes:

(1) Up to five exceptions are allowed in v1.1 and v1.2 of the Bluetooth specification

(2) Up to three exceptions are allowed in v1.1 and v1.2 of the Bluetooth specification

(3) Measured at F_0 = 2441MHz

Radio Characteristics	VDD = 1.8V	Temperature = -40°C				
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER	2.402	-	-83	-78	≤-70	dBm
	2.441	-	-85	-78		dBm
	2.480	-	-85	-78		dBm
Maximum received signal at 0.1% BER	2.402	0	-	-	≥-20	dBm
	2.441	0	-	-		dBm
	2.480	0	-	-		dBm
RF transmit power(1)	2.402	3.5	7.0	-	-6 to +4(2)	dBm
	2.441	3.5	7.0	-		dBm
	2.480	3.5	7.0	-		dBm
Initial carrier frequency tolerance	2.402	-	15	75	±75	kHz
	2.441	-	15	75		kHz
	2.480	-	15	75		kHz
20dB bandwidth for modulated carrier	2.402	-	862	1000	≤1000	kHz
	2.441	-	830	1000		kHz
	2.480	-	828	1000		kHz
Drift (single slot packet)	2.402	-	-	25	≤25	kHz
	2.441	-	-	25		kHz
	2.480	-	-	25		kHz
Drift (five slot packet)	2.402	-	-	40	≤40	kHz
	2.441	-	-	40		kHz
	2.480	-	-	40		kHz
Drift Rate	2.402	-	-	20	20	kHz/50µs
	2.441	-	-	20		kHz/50µs
	2.480	-	-	20		kHz/50µs
$\Delta f1_{avg}$ "Maximum Modulation"	2.402	140	165	175	$140<\Delta f1_{avg}<175$	kHz
	2.441	140	165	175		kHz
	2.480	140	165	175		kHz
$\Delta f2_{max}$ "Minimum Modulation"	2.402	115	150	-	115	kHz
	2.441	115	150	-		kHz
	2.480	115	150	-		kHz
RF power control range		16	35	-	≥16	dB
RF power range control resolution		-	1.8	-	-	dB

Note:

The RF characteristics at –40°C are only guaranteed for BlueCore2-External version B.

(1) BlueCore2-External firmware maintains the transmit power to be within the Bluetooth specification v1.1 and v1.2 limits.

(2) Class 2 RF transmit power range, Bluetooth specification v1.1 and v1.2

Radio Characteristics	VDD = 1.8V	Temperature = -20°C				
Receiver	**Frequency (GHz)**	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER	2.402	-	-83	-80	≤-70	dBm
	2.441	-	-85	-82		dBm
	2.480	-	-85	-82		dBm
Maximum received signal at 0.1% BER	2.402	0	-	-	≥-20	dBm
	2.441	0	-	-		dBm
	2.480	0	-	-		dBm
RF transmit power (1)	2.402	3.5	6.5	-	-6 to +4 (2)	dBm
	2.441	3.5	6.5	-		dBm
	2.480	3.5	6.5	-		dBm
Initial carrier frequency tolerance	2.402	-	18	75	±75	kHz
	2.441	-	17	75		kHz
	2.480	-	18	75		kHz
20dB bandwidth for modulated carrier	2.402	-	906	1000	≤1000	kHz
	2.441	-	844	1000		kHz
	2.480	-	819	1000		kHz
Drift (single slot packet)	2.402	-	-	25	≤25	kHz
	2.441	-	-	25		kHz
	2.480	-	-	25		kHz
Drift (five slot packet)	2.402	-	-	40	≤40	kHz
	2.441	-	-	40		kHz
	2.480	-	-	40		kHz
Drift Rate	2.402	-	-	20	20	kHz/50µs
	2.441	-	-	20		kHz/50µs
	2.480	-	-	20		kHz/50µs
$\Delta f1_{avg}$ "Maximum Modulation"	2.402	140	165	175	$140<\Delta f1_{avg}<175$	kHz
	2.441	140	165	175		kHz
	2.480	140	165	175		kHz
$\Delta f2_{max}$ "Minimum Modulation"	2.402	115	150	-	115	kHz
	2.441	115	150	-		kHz
	2.480	115	150	-		kHz
RF power control range		16	35	-	≥16	dB
RF power range control resolution		-	1.8	-	-	dB

Notes:

(1) BlueCore2-External firmware maintains the transmit power to be within the Bluetooth specification v1.1 and v1.2 limits.

(2) Class 2 RF transmit power range, Bluetooth specification v1.1 and v1.2

Radio Characteristics	VDD = 1.8V	Temperature = +85°C				
Receiver	**Frequency (GHz)**	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER	2.402	-	-81	-78	≤-70	dBm
	2.441	-	-83	-80		dBm
	2.480	-	-83	-80		dBm
Maximum received signal at 0.1% BER	2.402	0	-	-	≥-20	dBm
	2.441	0	-	-		dBm
	2.480	0	-	-		dBm
RF transmit power (1)	2.402	0	3.5	-	-6 to +4(2)	dBm
	2.441	0	3.5	-		dBm
	2.480	0	3.5	-		dBm
Initial carrier frequency tolerance	2.402	-	30	75	±75	kHz
	2.441	-	31	75		kHz
	2.480	-	32	75		kHz
20dB bandwidth for modulated carrier	2.402	-	853	1000	≤1000	kHz
	2.441	-	813	1000		kHz
	2.480	-	801	1000		kHz
Drift (single slot packet)	2.402	-	-	25	≤25	kHz
	2.441	-	-	25		kHz
	2.480	-	-	25		kHz
Drift (five slot packet)	2.402	-	-	40	≤40	kHz
	2.441	-	-	40		kHz
	2.480	-	-	40		kHz
Drift Rate	2.402	-	-	20	20	kHz/50µs
	2.441	-	-	20		kHz/50µs
	2.480	-	-	20		kHz/50µs
$\Delta f1_{avg}$ "Maximum Modulation"	2.402	140	165	175	$140<\Delta f1_{avg}<175$	kHz
	2.441	140	165	175		kHz
	2.480	140	165	175		kHz
$\Delta f2_{max}$ "Minimum Modulation"	2.402	115	150	-	115	kHz
	2.441	115	150	-		kHz
	2.480	115	150	-		kHz
RF power control range		16	35	-	≥16	dB
RF power range control resolution		-	1.8	-	-	dB

Notes:

(1) BlueCore2-External firmware maintains the transmit power to be within the Bluetooth specification v1.1 and v1.2 limits.

(2) Class 2 RF transmit power range, Bluetooth specification v1.1 and v1.2

6 Device Diagram

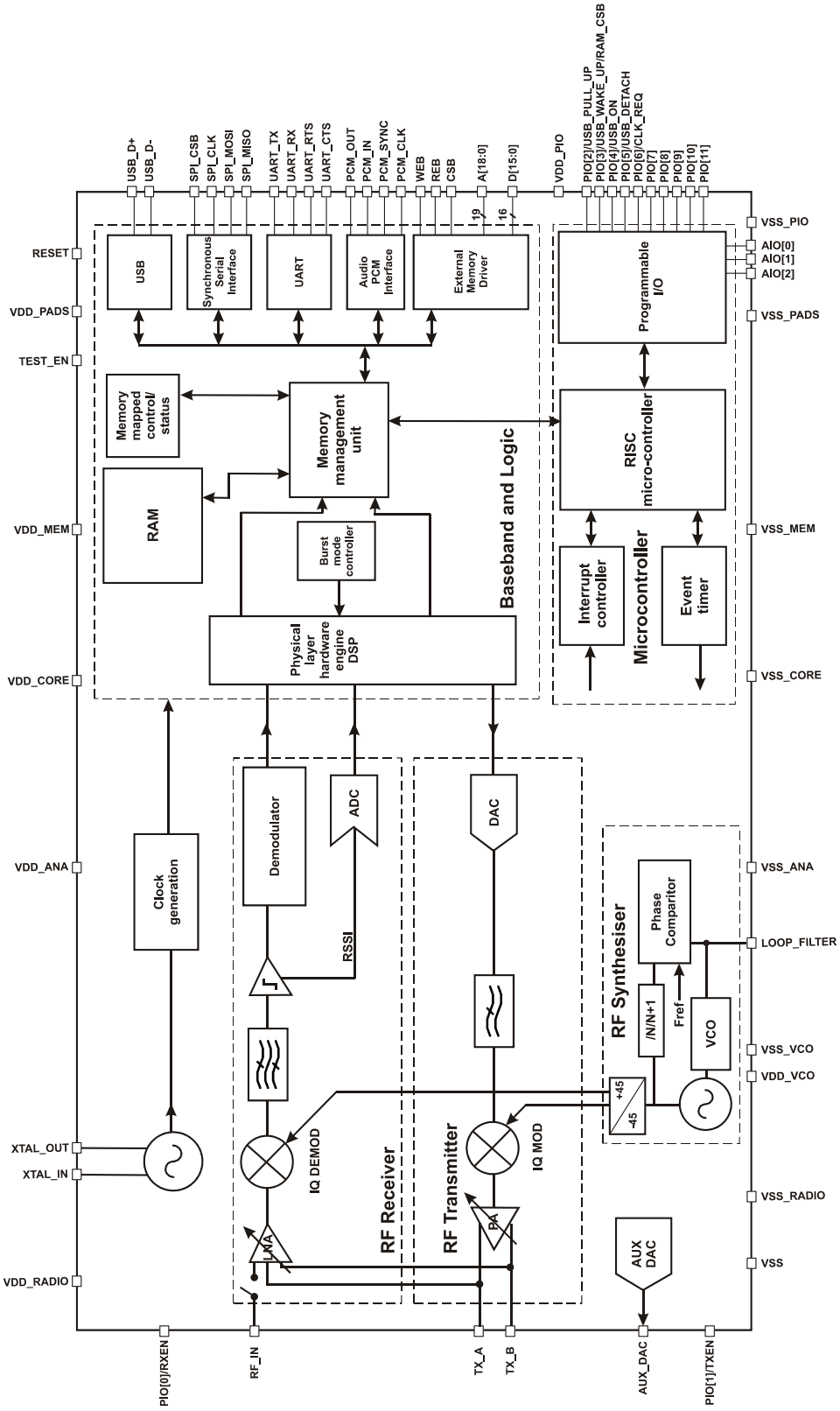


Figure 6.1: BlueCore2-External Device Diagram

7 Description of Functional Blocks

7.1 RF Receiver

The receiver features a near-zero Intermediate Frequency (IF) architecture that allows the channel filters to be integrated on to the die. Sufficient out-of-band blocking specification at the Low Noise Amplifier (LNA) input allows the radio to be used in close proximity to Global System for Mobile Communications (GSM) and Wideband Code Division Multiple Access (W-CDMA) cellular phone transmitters without being desensitised. The use of a digital Frequency Shift Keying (FSK) discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise allows BlueCore2-External to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

7.1.1 Low Noise Amplifier

The LNA can be configured to operate in single-ended or differential mode. Single-ended mode is used for Class 1 Bluetooth operation; differential mode is used for Class 2 operation.

7.1.2 Analogue to Digital Converter

The Analogue to Digital Converter (ADC) is used to implement fast Automatic Gain Control (AGC). The ADC samples the Received Signal Strength Indicator (RSSI) voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference limited environments.

7.2 RF Transmitter

7.2.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise the frequency drift during a transmit timeslot which results in a controlled modulation index. A digital baseband transmit filter provides the required spectral shaping.

7.2.2 Power Amplifier

The internal Power Amplifier (PA) has a maximum output power of +6dBm allowing BlueCore2-External to be used in Class 2 and Class 3 radios without an external RF PA. Support for transmit power control allows a simple implementation for Class 1 with an external RF PA.

7.3 RF Synthesiser

The radio synthesiser is fully integrated onto the die with no requirement for an external Voltage Controlled Oscillator (VCO) screening can, varactor tuning diodes or LC resonators.

7.4 Baseband and Logic

7.4.1 Memory Management Unit

The Memory Management Unit (MMU) provides a number of dynamically allocated ring buffers that hold the data which is in transit between the host and the air or vice versa. The dynamic allocation of memory ensures efficient use of the available Random Access Memory (RAM) and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers.

7.4.2 Burst Mode Controller

During radio transmission the Burst Mode Controller (BMC) constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During radio reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

7.4.3 Physical Layer Hardware Engine DSP

Dedicated logic is used to perform the following:

- Forward error correction
- Header error control
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

The following voice data translations and operations are performed by firmware:

- A-law/μ-law/linear voice data (from host)
- A-law/μ-law/Continuously Variable Slope Delta (CVSD) (over the air)
- Voice interpolation for lost packets
- Rate mismatches

7.4.4 RAM

32Kbytes of on-chip RAM is provided and is shared between the ring buffers used to hold voice/data for each active connection and the general purpose memory required by the Bluetooth stack.

7.4.5 External Memory Driver

The External Memory Driver interface can be used to connect to the external Flash memory and also to the optional external RAM for memory intensive applications.

7.4.6 USB

This is a full speed Universal Serial Bus interface for communicating with other compatible digital devices. BlueCore2-External acts as a USB peripheral, responding to requests from a Master host controller such as a PC.

7.4.7 Synchronous Serial Interface

This is a synchronous serial port interface for interfacing with other digital devices. The SPI port can be used for software debugging and for programming the external Flash memory.

7.4.8 UART

This is a standard Universal Asynchronous Receiver Transmitter (UART) interface for communicating with other serial devices.

7.4.9 Audio PCM Interface

The Audio Pulse Code Modulation (PCM) Interface supports continuous transmission and reception of PCM encoded audio data over Bluetooth.

7.5 Microcontroller

The microcontroller, interrupt controller and event timer run the Bluetooth software stack and control the radio and host interfaces. A 16-bit Reduced Instruction Set Computer (RISC) microcontroller is used for low power consumption and efficient use of memory.

7.5.1 Programmable I/O

BlueCore2-External has a total of 15 (12 digital and 3 analogue) programmable I/O terminals. These are controlled by firmware running on the device.

8 CSR Bluetooth Software Stacks

BlueCore2-External is supplied with Bluetooth stack firmware which runs on the internal RISC microcontroller. This is compliant with the Bluetooth specification v1.1 and v1.2.

The BlueCore2-External software architecture allows Bluetooth processing overheads to be shared in different ways between the internal RISC microcontroller and the host processor. The upper layers of the Bluetooth stack (above HCI) can be run either on-chip or on the host processor.

Running the upper stack on BlueCore2-External reduces (or eliminates, in the case of a virtual machine (VM) application) the need for host-side software and processing time. Running the upper layers on the host processor allows greater flexibility.

8.1 BlueCore HCI Stack

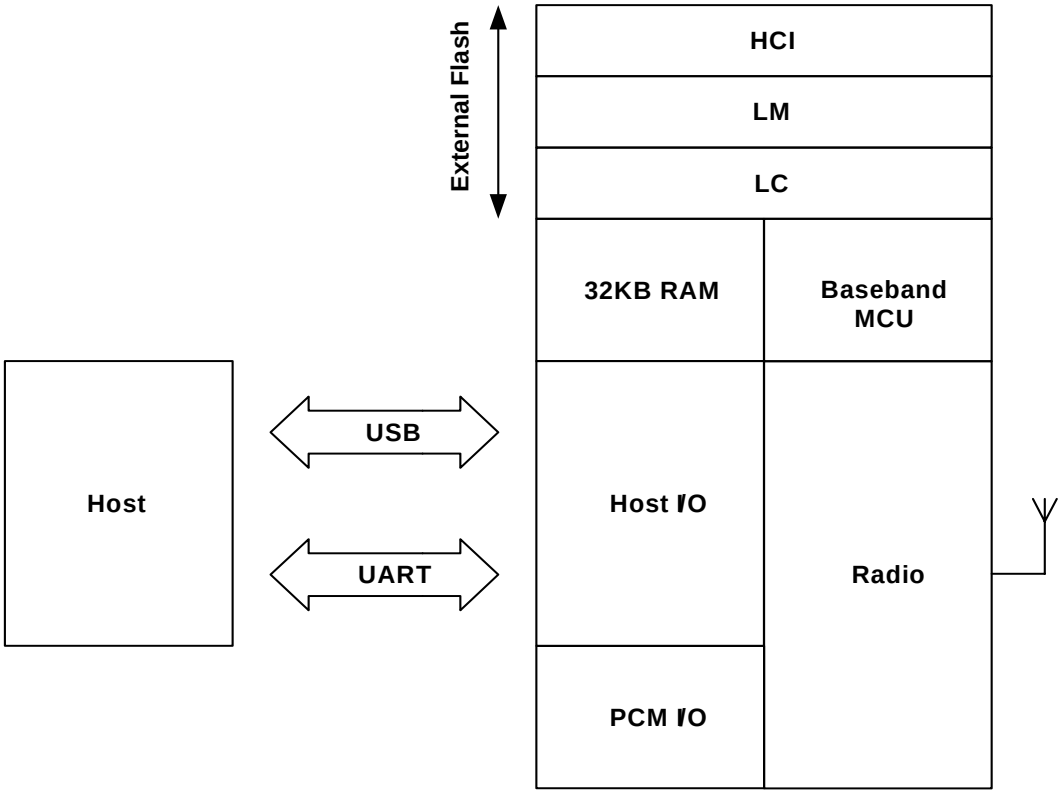


Figure 8.1: BlueCore HCI Stack

In this implementation the internal processor runs the Bluetooth stack up to the Host Controller Interface (HCI). All upper layers must be provided by the Host processor.

8.1.1 Key Features of the HCI Stack

Standard Bluetooth Functionality

The firmware has been written against the Bluetooth Core Specification v1.1 and v1.2.

- Bluetooth components: Baseband (including LC), LM and HCI
- Standard USB v1.1 and UART (H4) HCI Transport Layers
- All standard radio packet types
- Full Bluetooth data rate, up to 723.2kb/s asymmetric(1)
- Operation with up to seven active slaves: 7(1)
- Maximum number of simultaneous active ACL connections: 7(2)
- Maximum number of simultaneous active SCO connections: 3(2)
- Operation with up to three SCO links, routed to one or more slaves
- Role switch: can reverse Master/Slave relationship
- All standard SCO voice codings, plus “transparent SCO”
- Standard operating modes: Page, Inquiry, Page-Scan and Inquiry-Scan
- All standard pairing, authentication, link key and encryption operations
- Standard Bluetooth power saving mechanisms: Hold, Sniff and Park modes, including “Forced Hold”
- Dynamic control of peers’ transmit power via LMP
- Master/Slave switch
- Broadcast
- Channel quality driven data rate
- All standard Bluetooth Test Modes
- Standard firmware upgrade via USB (DFU)

The firmware’s supported Bluetooth features are detailed in the standard PICS documents, available from www.csrsupport.com.

Note:

(1) Maximum allowed by Bluetooth specification v1.1 and v1.2.

(2) BlueCore2-External supports all combinations of active ACL and SCO channels for both Master and Slave operation, as specified by the Bluetooth specification v1.1 and v1.2.

Extra Functionality

The firmware extends the standard Bluetooth functionality with the following features:

- Supports BlueCore Serial Protocol (BCSP), a proprietary, reliable alternative to the standard Bluetooth H4 UART Host Transport.
- Provides a set of approximately 50 manufacturer-specific HCI extension commands. This command set (called BCCMD – “BlueCore Command”), provides:

  - Access to the chip's general-purpose PIO port
  - Access to the chip's Bluetooth clock; this can help transfer connections to other Bluetooth devices
  - The negotiated effective encryption key length on established Bluetooth links
  - Access to the firmware's random number generator
  - Controls to set the default and maximum transmit powers – these can help minimise interference between overlapping, fixed-location piconets
  - Dynamic UART configuration
  - Radio transmitter enable/disable: a simple command connects to a dedicated hardware switch that determines whether the radio can transmit
- The firmware can read the voltage on a pair of the chip's external pins. This is normally used to build a battery monitor, using either VM or host code.
- A block of BCCMD commands provides access to the chip's "persistent store" configuration database. The database sets the device's Bluetooth address, Class of Device, radio (transmit class) configuration, SCO routing, LM, USB and DFU constants, etc.
- A UART "break" condition can be used in three ways:
  - Presenting a UART break condition to the chip can force the chip to perform a hardware reboot
  - Presenting a break condition at boot time can hold the chip in a low power state, preventing normal initialisation while the condition exists
  - With BCSP, the firmware can be configured to send a break to the host before sending data – normally used to wake the host from a Deep Sleep state
- The DFU standard has been extended with public/private key authentication, allowing manufacturers to control the firmware that can be loaded onto their Bluetooth modules.
- A modified version of the DFU protocol allows firmware upgrade via the chip's UART.
- A block of "radio test" or BIST commands allows direct control of the chip's radio. This aids the development of modules' radio designs, and can be used to support Bluetooth qualification.
- Virtual Machine (VM). The firmware provides the VM environment in which to run application-specific code. Although the VM is mainly used with BlueLab™ and RFCOMM builds (alternative firmware builds providing L2CAP, SDP and RFCOMM), the VM can be used with this build to perform simple tasks, such as flashing LEDs, via the chip's PIO port.
- Hardware low power modes: Shallow Sleep and Deep Sleep. The chip drops into modes that significantly reduce power consumption when the software goes idle.
- SCO channels are normally routed over HCI (over BCSP). However, a single SCO channel can be routed over the chip's single PCM port (at the same time as routing up to two other SCO channels over HCI). [Future versions of BlueCore2-External firmware will be able to exploit the hardware's ability to route up to three SCO channels through the single PCM port.]

8.2 BlueCore RFCOMM Stack

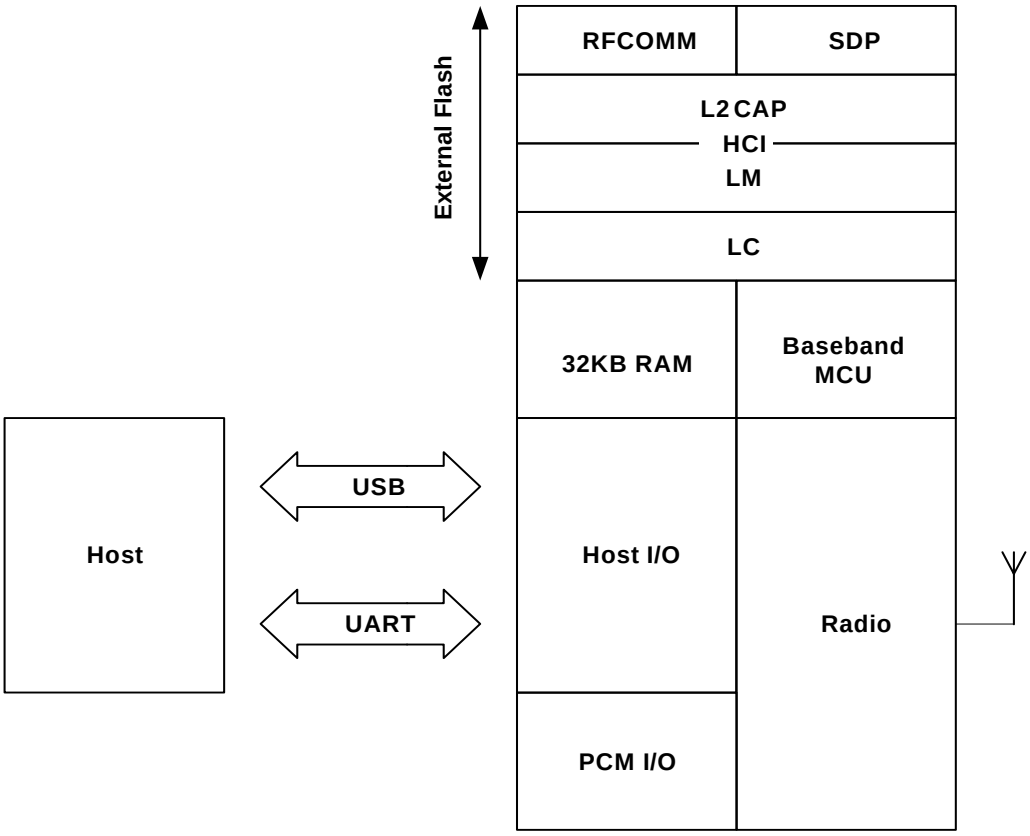


Figure 8.2: BlueCore RFCOMM Stack

In this version of the firmware the upper layers of the Bluetooth stack up to RFCOMM are run on-chip. This reduces host-side software and hardware requirements at the expense of some of the power and flexibility of the HCI only stack.

8.2.1 Key Features of the BlueCore2-External RFCOMM Stack

Interfaces to Host

- RFCOMM, an RS-232 serial cable emulation protocol
- SDP, a service database look-up protocol

Connectivity

- Maximum number of active slaves: 3
- Maximum number of simultaneous active ACL connections: 3
- Maximum number of simultaneous active SCO connections: 3
- Data Rate: up to 350 Kb/s

Security

- Full support for all Bluetooth security features up to and including strong (128-bit) encryption.

Power Saving

- Full support for all Bluetooth power saving modes (Park, Sniff and Hold).

Data Integrity

- CQDDR increases the effective data rate in noisy environments.
- RSSI used to minimise interference to other radio devices using the ISM band.

8.3 BlueCore Virtual Machine Stack

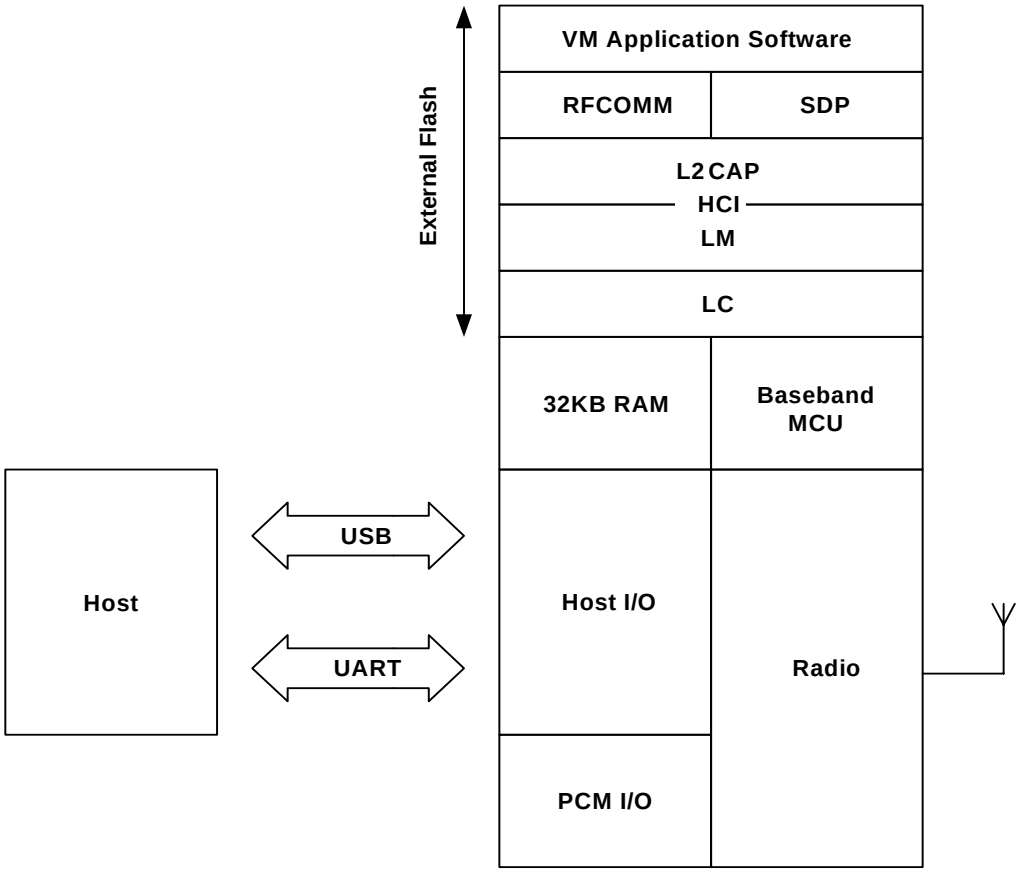


Figure 8.3: Virtual Machine Stack

This version of the stack firmware requires no host processor. All software layers, including application software, run on the internal RISC processor in a protected user software execution environment known as a Virtual Machine (VM).

The user may write custom application code to run on the BlueCore VM using BlueLab software development kit (SDK) supplied with the BlueLab and Casira™ development kits, available separately from CSR. This code will then execute alongside the main BlueCore firmware. The user is able to make calls to the BlueCore firmware for various operations.

The execution environment is structured so the user application does not adversely affect the main software routines, thus ensuring that the Bluetooth stack software component does not need re-qualification when the application is changed.

Using the VM and the BlueLab SDK the user is able to develop applications such as a cordless headset or other profiles without the requirement of a host controller. BlueLab is supplied with example code including a full implementation of the headset profile.

Note:

Sample applications to control PIO lines can also be written with BlueLab SDK and the VM for the HCI stack.

8.4 BlueCore HID Stack

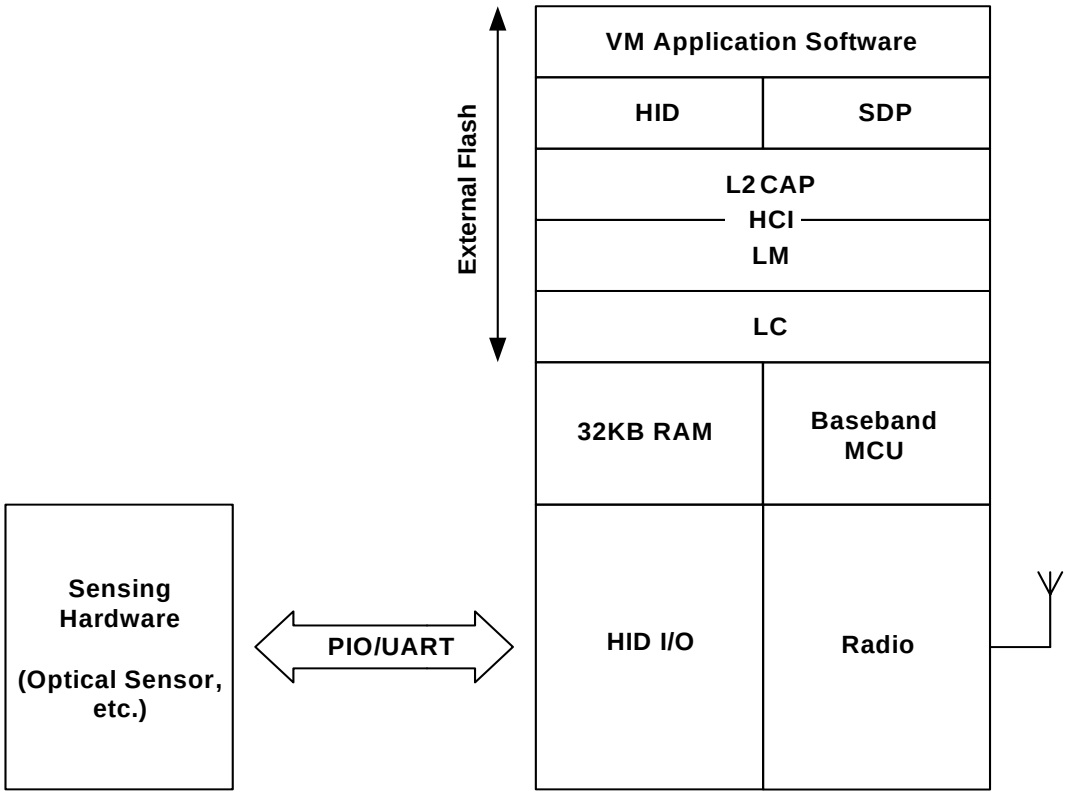


Figure 8.4: HID Stack

This version of the stack firmware requires no host processor. All software layers, including application software, run on the internal RISC microcontroller in a protected user software execution environment known as a virtual machine (VM).

The user may write custom application code to run on the BlueCore VM using BlueLab Professional software development kit (SDK) supplied with the BlueLab Professional and Casira development kits, available separately from CSR. This code will then execute alongside the main BlueCore firmware. The user is able to make calls to the BlueCore firmware for various operations.

The execution environment is structured so the user application does not adversely affect the main software routines, thus ensuring that the Bluetooth stack software component does not need re-qualification when the application is changed.

Using the VM and the BlueLab Professional SDK the user is able to develop Bluetooth HID devices such as an optical mouse or keyboard. The user is able to customise features such as power management and connect/reconnect behaviour.

The HID I/O component in the HID stack controls low latency data acquisition from external sensor hardware. With this component running in native code, it does not incur the overhead of the VM code interpreter. Supported external sensors include 5 mouse buttons, the Agilent ADNS-2030 optical sensor, quadrature scroll wheel, direct coupling to a keyboard matrix and a UART interface to custom hardware.

A reference schematic for implementing a three button, optical mouse with scroll wheel is available from CSR.

8.5 Host-Side Software

BlueCore2-External can be ordered with companion host-side software:

BlueCore2-PC includes software for a full Windows® 98/ME, Windows 2000 or Windows XP Bluetooth host-side stack together with IC hardware described in this document.

BlueCore2-Mobile includes software for a full host-side stack designed for modern ARM based mobile handsets together with IC hardware described in this document.

8.6 Device Firmware Upgrade

BlueCore2-External is supplied with boot loader software which implements a Device Firmware Upgrade (DFU) capability. This allows new firmware to be uploaded to the external Flash memory through BlueCore2-External's UART or USB ports.

8.7 Additional Software for Other Embedded Applications

When the upper layers of the Bluetooth protocol stack are run as firmware on BlueCore2-External, a UART software driver is supplied that presents the L2CAP, RFCOMM and Service Discovery (SDP) APIs to higher Bluetooth stack layers running on the host. The code is provided as 'C' source or object code.

8.8 CSR Development Systems

CSR's BlueLab™, Casira™ and MicroSira™ development kits are available to allow the evaluation of the BlueCore2-External hardware and software, and as toolkits for developing on-chip and host software.

9 Device Terminal Descriptions

9.1 RF Ports

The BlueCore2-External RF_IN terminal can be configured as either a single-ended or differential input. The operational mode is determined by setting the Persistent Store Key (PS Key) PSKEY_TXRX_PIO_CONTROL (0x209).

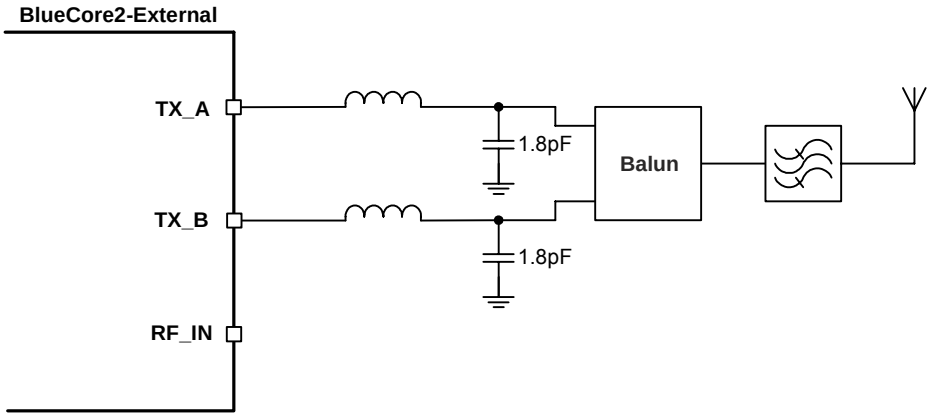


Figure 9.1: Differential RF Input (Class 2)

Figure 9.2 shows how using a single-ended RF input allows an external PA to be used for Class 1 operation.

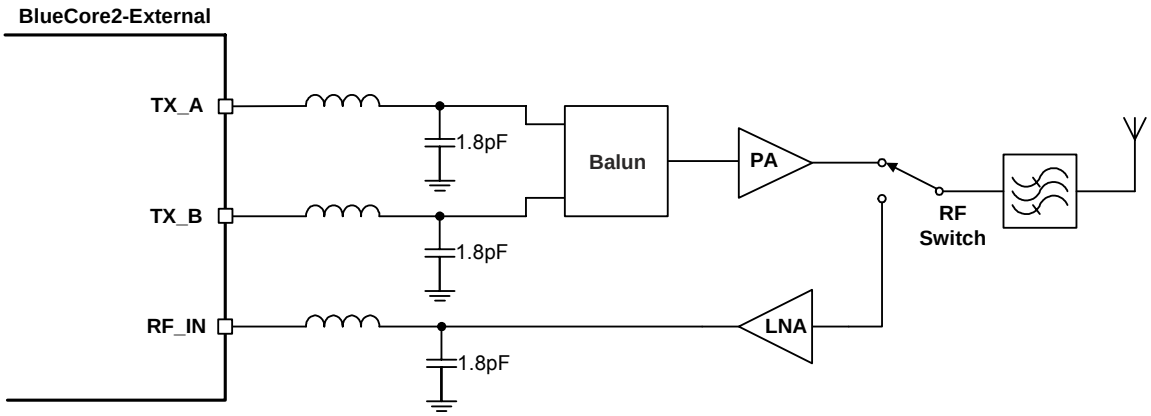


Figure 9.2: Single Ended RF Input (Class 1)

9.1.1 Receiver Input (RF_IN)

This is the single-ended RF input from the antenna. The input presents a complex impedance that requires a matching network between the terminal and the antenna. Starting from the substrate (chip) side, the input can be modelled as a lossy capacitor with the bond wire to the ball grid represented as a series inductance.

The terminal is DC-blocked. The DC level must not exceed (VSS_RADIO - 0.3V to VDD_RADIO + 0.3V).

Note:

Both terminals must be externally DC-biased to VDD_RADIO.

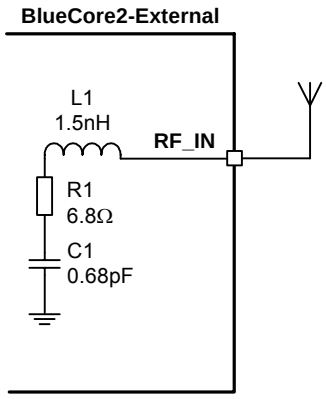


Figure 9.3: Circuit RF_IN

9.1.2 TX_A and TX_B

TX_A and TX_B form a complementary balanced pair. On transmit, their outputs are combined using a balun into the single-ended output required for the antenna. Similarly, on receive, their input signals are combined internally. Both terminals present similar complex impedances that require matching networks between them and the balun. Starting from the substrate (chip-side), the outputs can each be modelled as an ideal current source in parallel with a lossy resistance and a capacitor. The bond wire can be represented as series inductance.

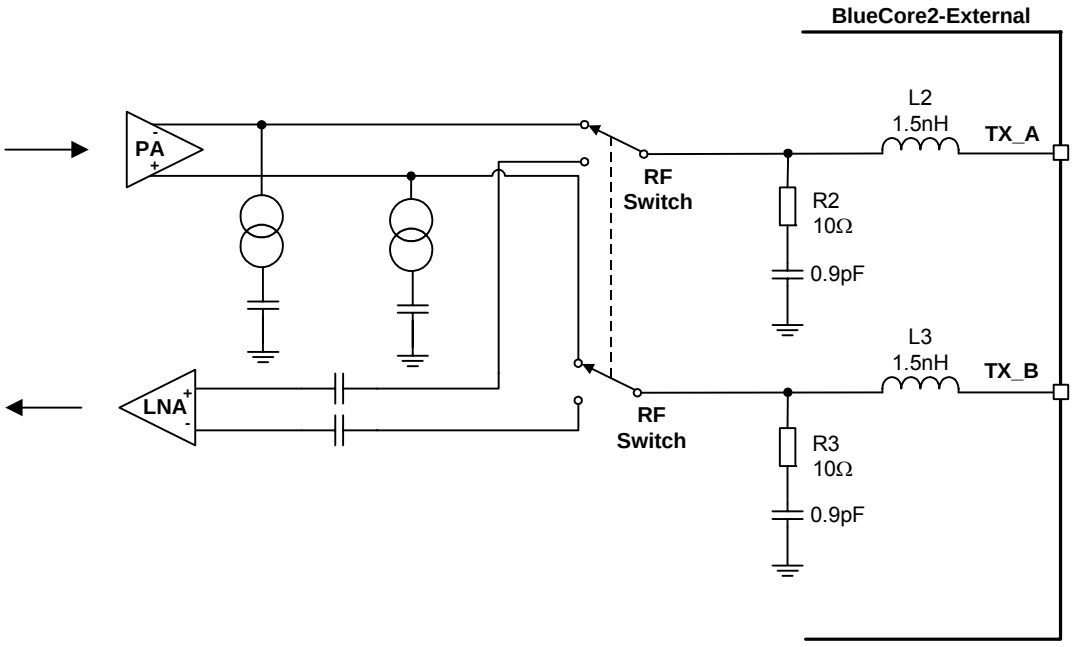


Figure 9.4: Circuit TX/RX_A and TX/RX_B

9.1.3 Transmit RF Power Control for Class 1 Applications (TX_PWR)

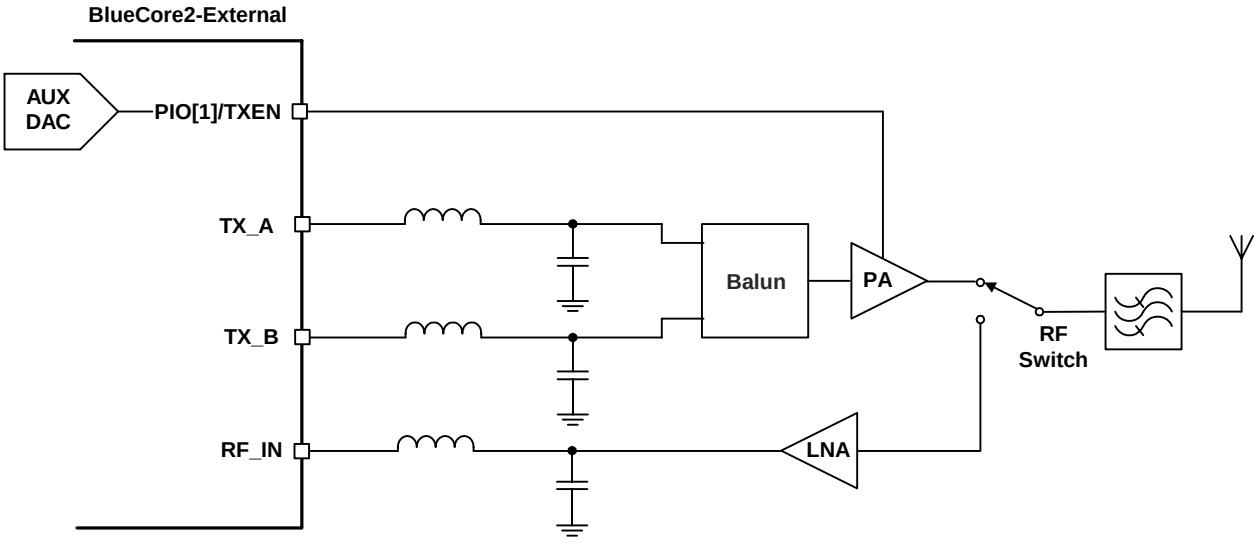


Figure 9.5: Power Amplifier Configuration for Class 1 Applications

An 8-bit voltage DAC (AUX_DAC) is used to control the amplification level of the external PA for Class 1 operation. The DAC output is derived from the on-chip band gap and is virtually independent of temperature and supply voltage. For a load current ≤10mA (sourced from the device), the output voltage is derived by:

$$V_{DAC} = MIN\left(\left(3.3v \times \frac{CNTRL\_WORD}{255}\right), \left(VDD\_PIO - 0.3v\right)\right)$$

Or, for no load current, the output voltage is derived by:

$$V_{DAC} = MIN\left(\left(3.3v \times \frac{CNTRL\_WORD}{255}\right), VDD\_PIO\right)$$

BlueCore2-External enables the external PA only when transmitting. Before transmitting, the chip normally ramps up the power to the internal PA, then it ramps it down again afterwards. However, if a suitable external PA is used, it may be possible to ramp the power externally by driving the TX_PWR pin on the PA from AUX_DAC.

Internal Power Ramping

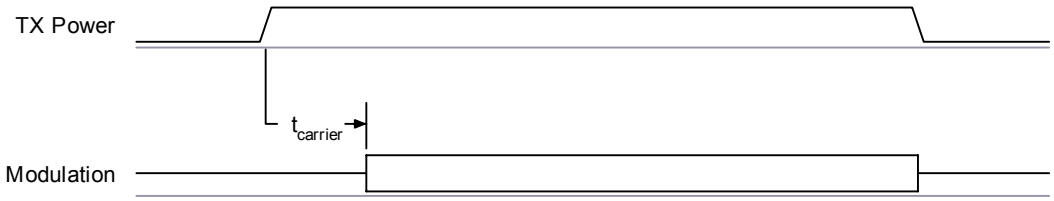


Figure 9.6: Internal Power Ramping

The PS Key PSKEY_TX_GAINRAMP (0x1d), is used to control the delay (in units of μs) between the end of the transmit power ramp and the start of modulation. In this period the carrier is transmitted which gives the transmit circuitry, time to fully settle to the correct frequency.

Bits [15:8] define a delay, $t_{carrier}$, (in units of μs) between the end of the transmit power ramp and the start of modulation. In this period carrier is transmitted, which aids interoperability with some other vendor equipment which is not strictly Bluetooth compliant.

Control of External RF Components

A PS Key TXRX_PIO_CONTROL (0x209) is used to control external RF components such as a switch, an external PA or an external LNA. PIO[0], PIO[1] and the AUX_DAC can be used for this purpose as follows:

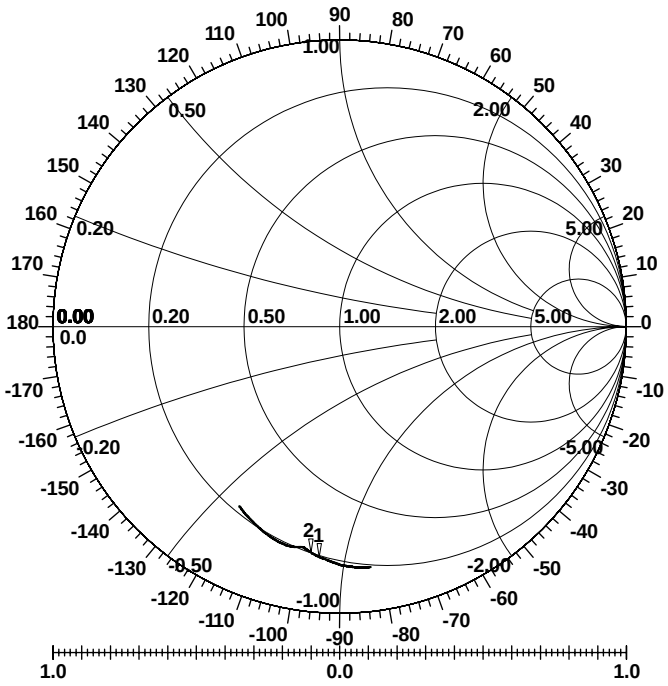
TXRX_PIO_CONTROL Value	
0	PIO[0], PIO[1], AUX_DAC not used to control RF. Power ramping is internal.
1	PIO[0] is high during RX, PIO[1] is high during TX. AUX_DAC not used. Power ramping is internal.
2	PIO[0] is high during RX, PIO[1] is high during TX. AUX_DAC used to set gain of external PA. Power ramping is external.
3	PIO[0] is low during RX, PIO[1] is low during TX. AUX_DAC used to set gain of external PA. Power ramping is external.
4	PIO[0] is high during RX, PIO[1] is high during TX. AUX_DAC used to set gain of external PA. Power ramping is internal.

Table 9.1: TXRX_PIO_CONTROL Values

See **Error! Reference source not found.**, which shows the typical TX output RF level of the internal TX RF PA against the internal control word.

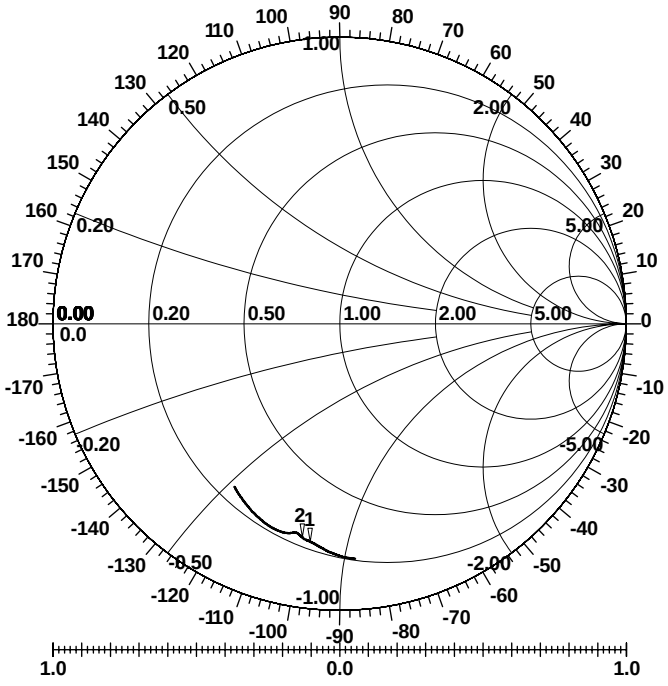
The Bluetooth specification (v1.1 and v1.2) requires a step size between 2dB and 8dB. The BlueCore2-External power control circuits operate with much finer granularity than that required in the specification.

9.1.4 Transmit and Receive Port Impedances for 8 x 8 x 1.0mm package



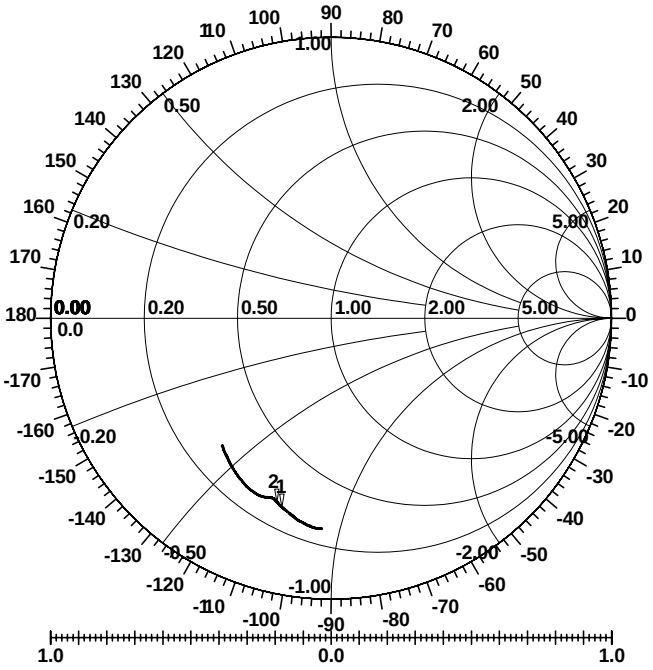
1: ZTTX_A (2.402GHz) = (9.8-j44.8)Ω
2: ZTTX_A (2.480GHz) = (10.1-j43.0)Ω

Figure 9.7: TX_A Transmit Mode (Power Level 30)



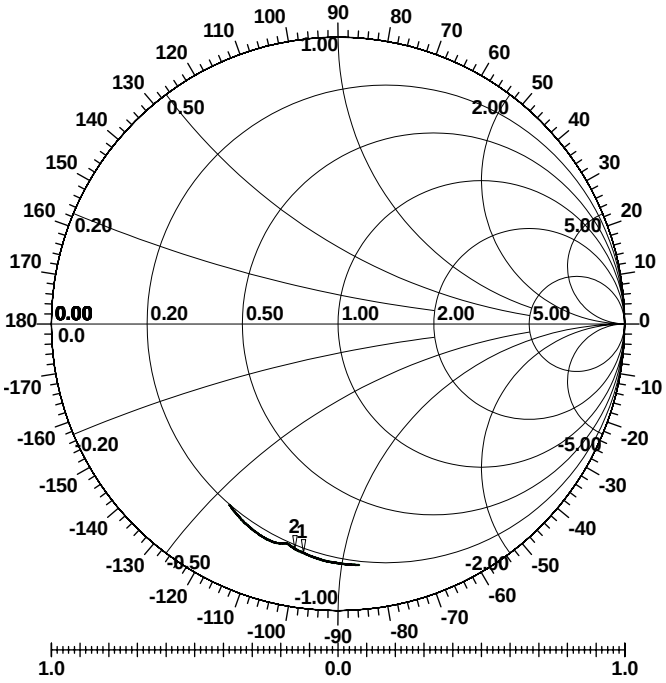
1: ZTTX_A (2.402GHz) = (11.5-j42.3)Ω
2: ZTTX_A (2.480GHz) = (11.8-j40.6)Ω

Figure 9.8: TX_A Transmit Mode (Power Level 45)



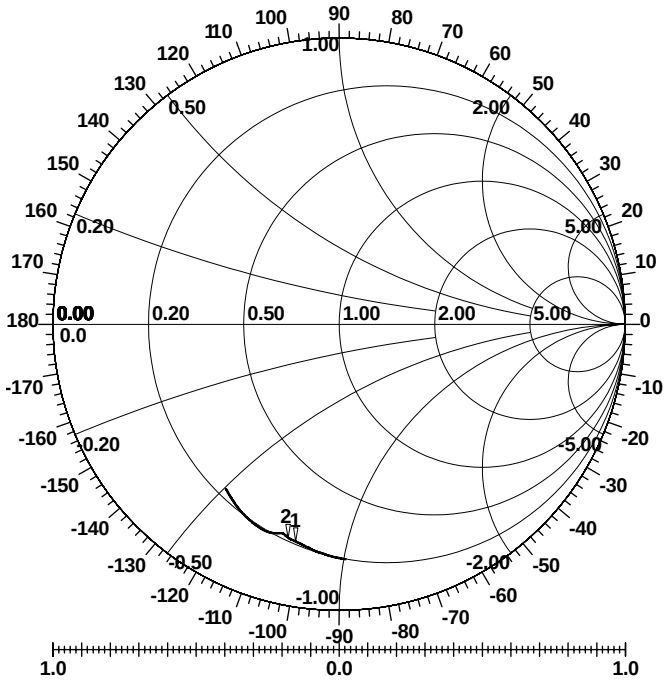
1: ZTTX_A (2.402GHz) = (14.1-j36.7)Ω
2: ZTTX_A (2.480GHz) = (14.5-j35.3)Ω

Figure 9.9: TX_A Transmit Mode (Power Level 63)



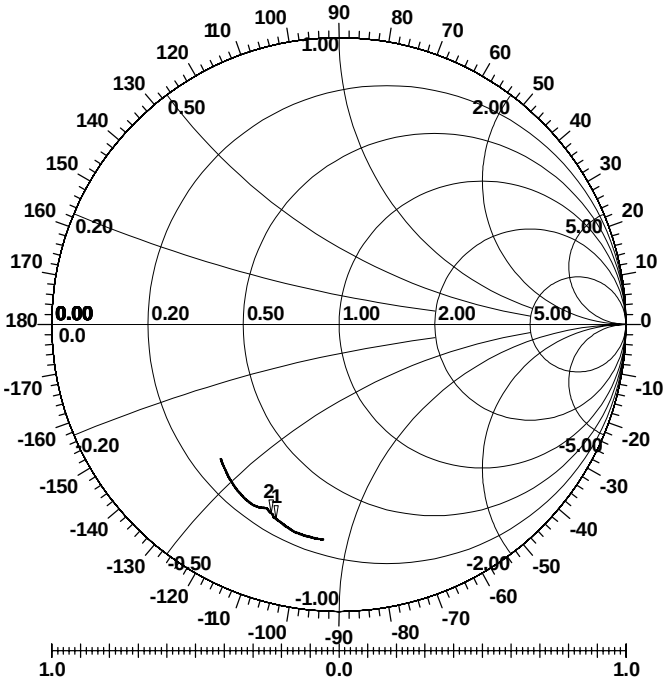
1: ZTTX_B (2.402GHz) = (9.2-j42.2)Ω
2: ZTTX_B (2.480GHz) = (9.3-j40.5)Ω

Figure 9.10: TX_B Transmit Mode (Power Level 30)



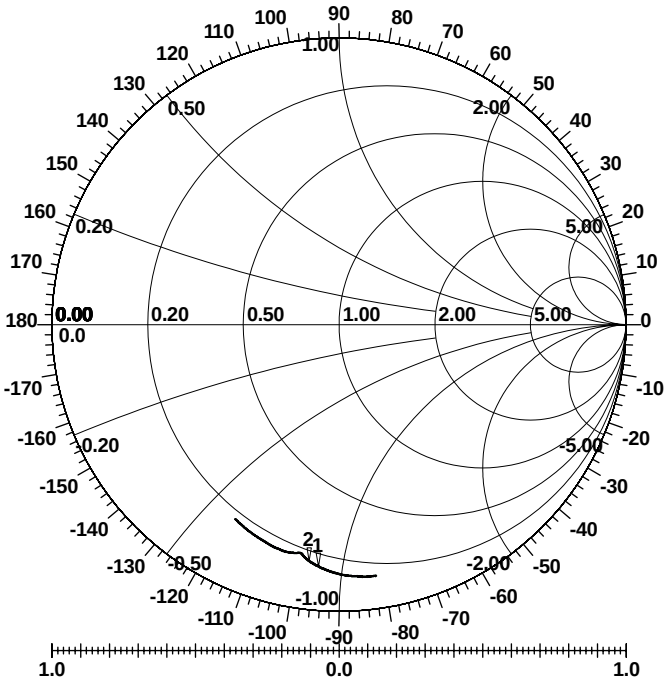
1: ZTTX_B (2.402GHz) = (10.6-j39.9)Ω
2: ZTTX_B (2.480GHz) = (10.7-j38.3)Ω

Figure 9.11: TX_B Transmit Mode (Power Level 45)



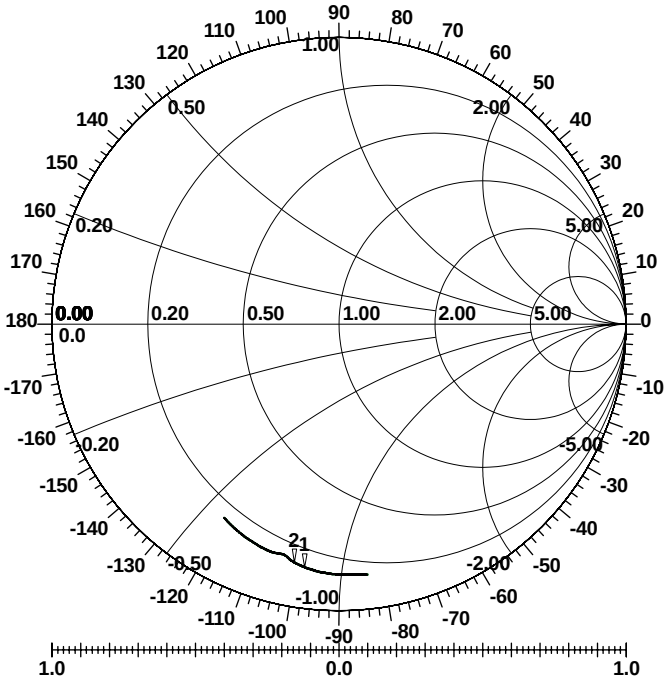
1: ZTTX_B (2.402GHz) = (12.7-j34.9)Ω
2: ZTTX_B (2.480GHz) = (13.1-j33.6)Ω

Figure 9.12: TX_B Transmit Mode (Power Level 63)



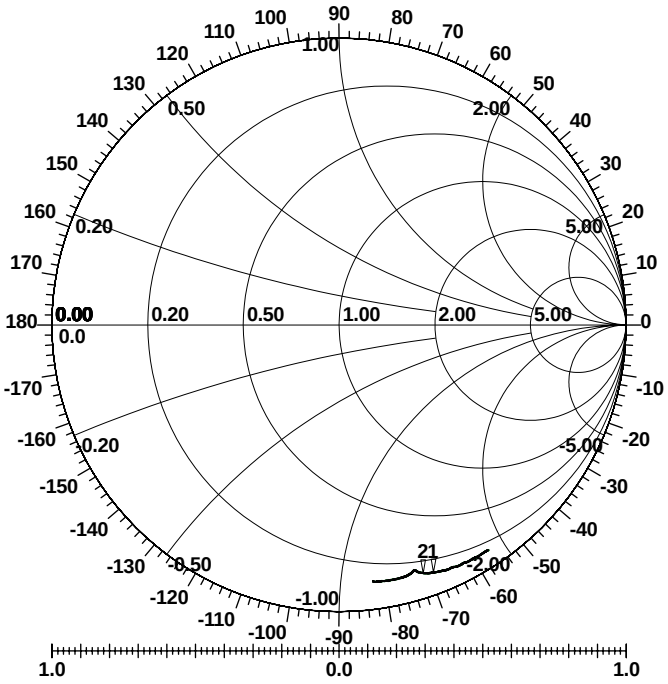
1: ZRTX_A (2.402GHz) = (7.7-j45)Ω
2: ZRTX_A (2.480GHz) = (8.2-j43.4)Ω

Figure 9.13: TX_A in Receive Mode



1: ZRTX_B (2.402GHz) = (6.8-j43.0)Ω
2: ZRTX_B (2.480GHz) = (7.1-j41.0)Ω

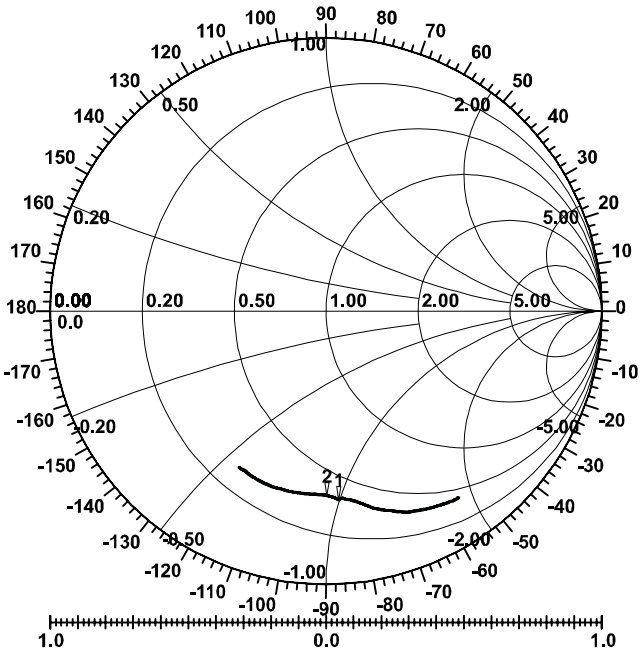
Figure 9.14: TX_B in Receive Mode



1: ZRF_IN (2.402GHz) = (6.2-j72.2)Ω
2: ZRF_IN (2.480GHz) = (6.7-j69.3)Ω

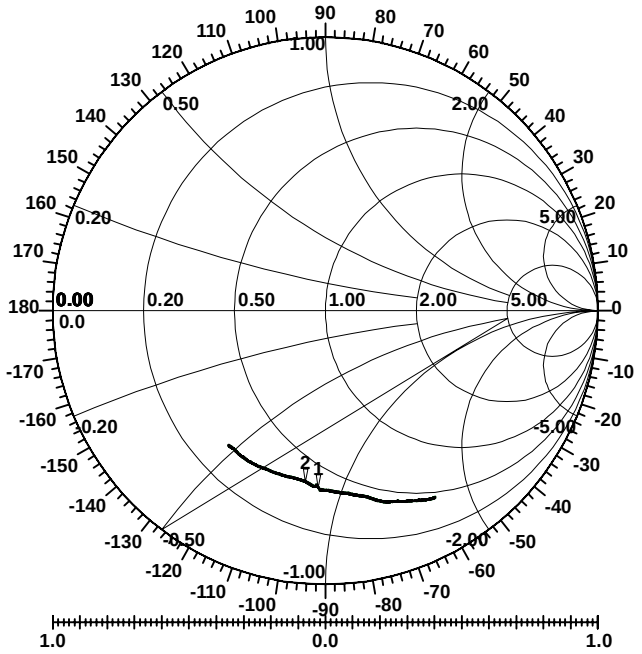
Figure 9.15: Unbalanced RF Input

9.1.5 Transmit and Receive Port Impedances for 6 x6 x 1.0mm Package



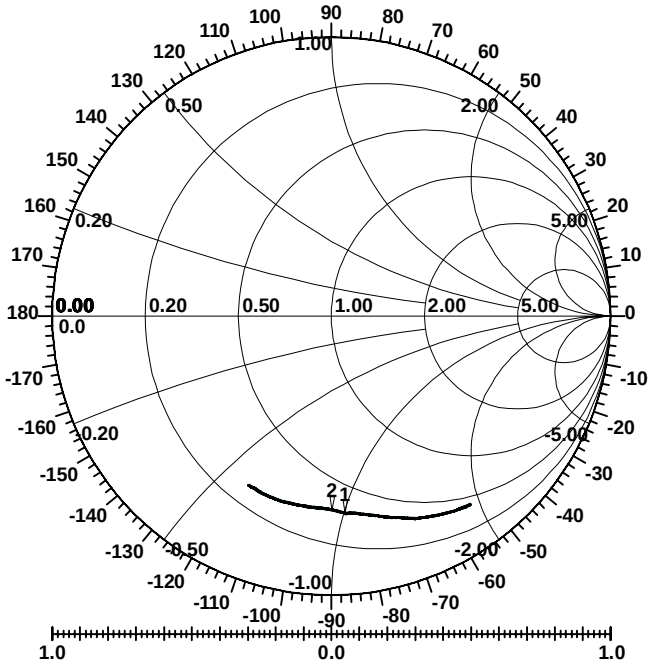
ZTTX_A (2.402GHz) = (18.9-j-49.7)
ZTTX_A (2.480GHz) = (18.85-j46.5)

Figure 9.16: TX_A Transmit Mode (Power Level 50)



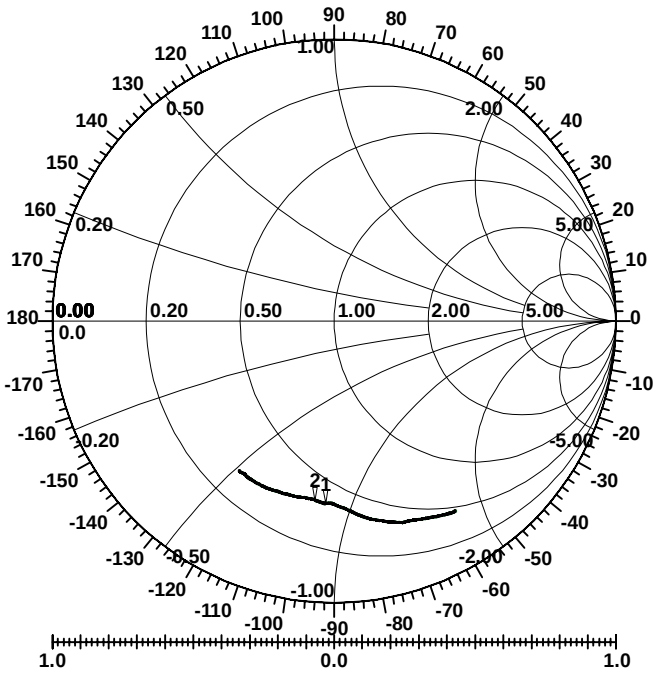
ZTTX_A (2.402GHz) = (19.8-j-43.95)
ZTTX_A (2.480GHz) = (19.6-j-40.55)

Figure 9.17: TX_A Transmit Mode (Power Level 63)



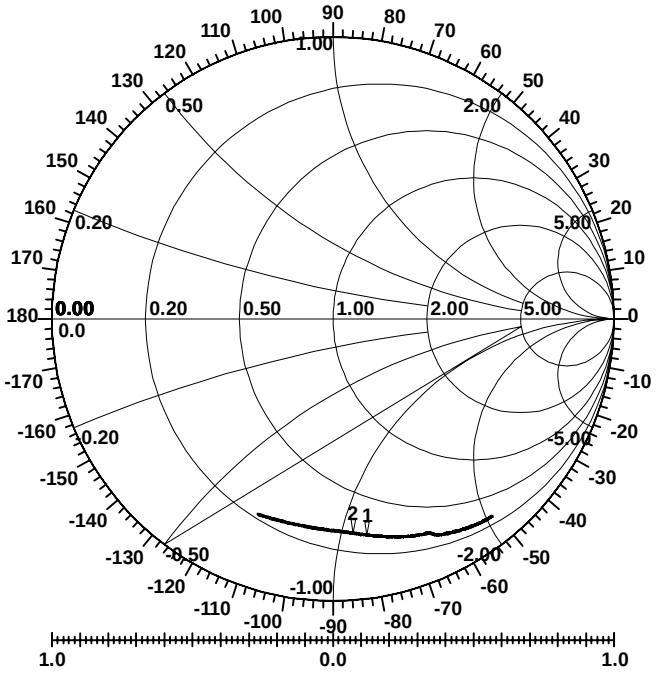
ZTTX_A (2.402GHz) = (17.8-j-50.3)
ZTTX_A (2.480GHz) = (17.6-j-46.95)

Figure 9.18: TX_B Transmit Mode (Power Level 50)



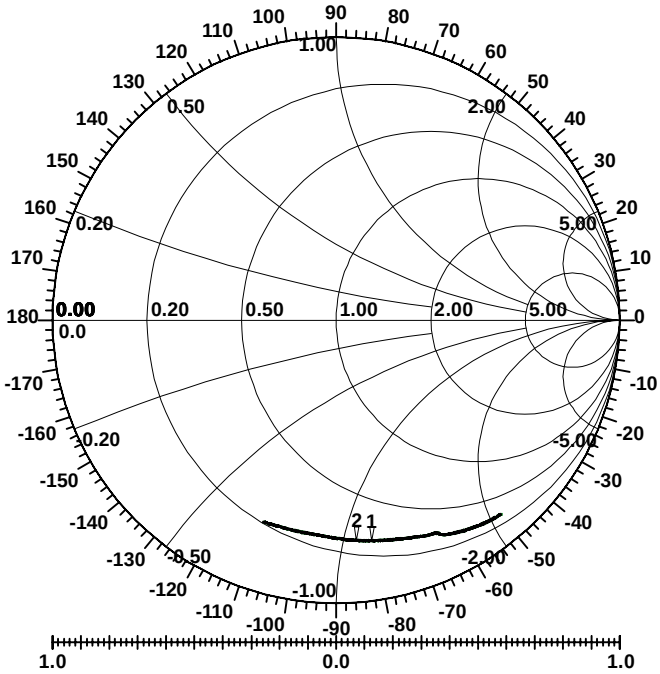
ZTTX_A (2.402GHz) = (19.6-j-43.7)
ZTTX_A (2.480GHz) = (19.15-j-41.1)

Figure 9.19: TX_B Transmit Mode (Power Level 63)



ZRTX_A (2.402GHz) = (14.7-j-56.35)
ZRTX_A (2.480GHz) = (14.5-j-52.75)

Figure 9.20: TX_A in Receive Mode



ZRTX_B (2.402GHz) = (13.85-j-56.8)
ZRTX_B (2.480GHz) = (13.4-j-53.05)

Figure 9.21: TX_B in Receive Mode

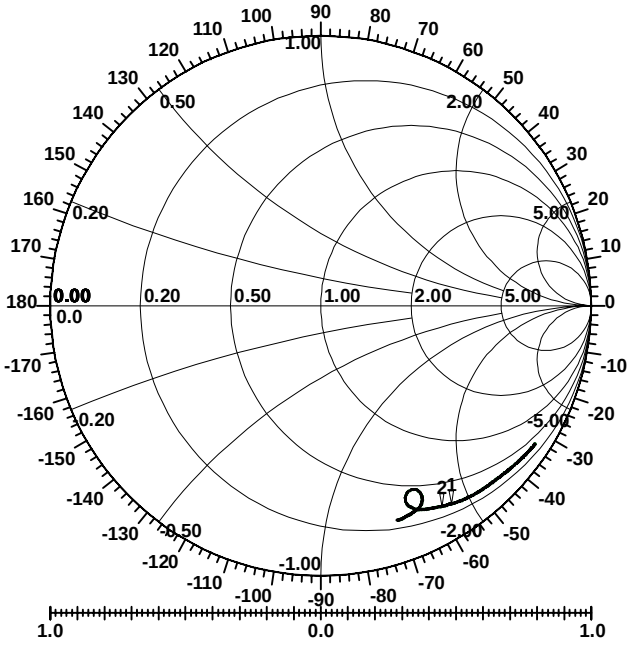


Figure 9.22: Unbalanced RF Inputt

9.2 Loop Filter

The RF Synthesiser that generates the transmit and receive frequencies consists of a VCO controlled by an RF frequency comparator. The control voltage loop requires external filter components, which are attached to the LOOP_FILTER terminal. Figure 9.23 indicates recommended values for these components.

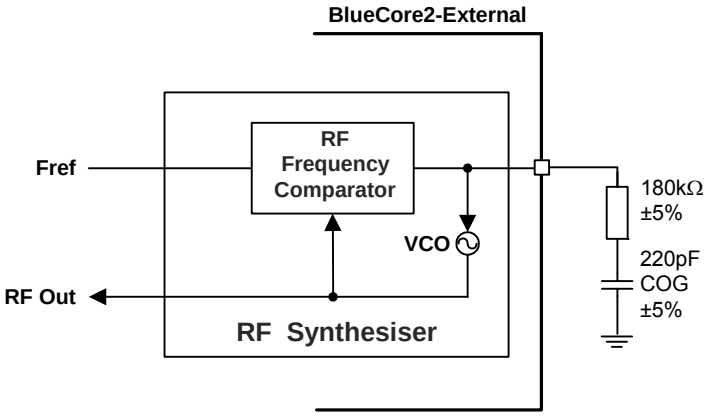


Figure 9.23: Recommended Component Values for External Loop_Filter

9.3 Crystal Oscillator/Reference Clock Input (XTAL_IN)

The BlueCore2-External RF local oscillator and internal digital clocks are derived from the reference clock at the BlueCore2-External XTAL_IN input. This reference may be either an external clock or from a crystal placed between XTAL_IN and XTAL_OUT.

9.3.1 External Mode

BlueCore2-External may be configured to accept an external reference clock (from another device) at XTAL_IN by setting the PS Key PSKEY_USE_EXTERNAL_CLOCK (0x23b), and connecting XTAL_OUT to ground. Ideally, the external clock should be a digital level square wave as this may be directly coupled to XTAL_IN without the need for additional components. If the reference clock is sinusoidal, it must be driven through a DC blocking capacitor connected to XTAL_IN. A digital level reference clock gives superior noise immunity as the high slew rate clock edges have lower voltage-to-phase conversion.

Digital Clock

The digital clock signal should meet the following specifications:

	Min	Typ	Max
Frequency (1)	8MHz	16MHz	32MHz
Duty cycle	10:90	50:50	90:10
Edge Jitter			15ps rms
Logic High Level (2)	VDD_ANA –0.2V		VDD_ANA +0.2V
Logic Low Level	-0.2V		+ 0.2V
Rise Time (3)			1ns
Fall time (3)			1ns

Table 9.2: Digital Clock Signals

Notes:

(1) The frequency should be an integer multiple of 250kHz

(2) VDD_ANA is 1.8V nominal

(3) Rise/Fall times measured between 20% and 80% levels

9.3.2 Input Frequencies

BlueCore2-External should be configured to operate with the chosen reference frequency. This is accomplished by setting the PS PSKEY_ANA_FREQ (0x1fe).

9.3.3 XTAL Mode

BlueCore2-External contains a crystal driver circuit. This operates with an external crystal and capacitors to form a Pierce oscillator.

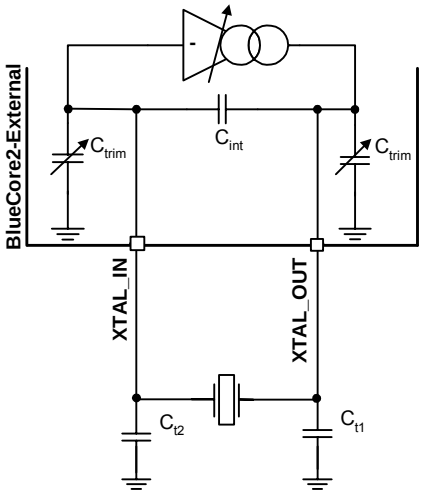


Figure 9.24: BlueCore2 External Crystal Driver Circuit

Figure 9.25 shows an electrical equivalent circuit for a crystal. The crystal appears inductive near its resonant frequency. It forms a resonant circuit with its load capacitors.

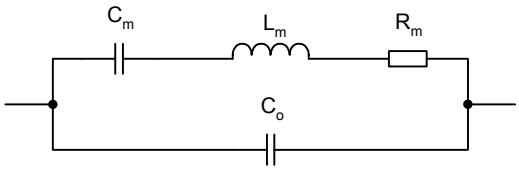


Figure 9.25: Crystal Equivalent Circuit

The resonant frequency may be trimmed with the crystal load capacitance. BlueCore2-External contains variable internal capacitors to provide a fine trim.

The BlueCore2-External driver circuit is a transconductance amplifier. A voltage at XTAL_IN generates a current at XTAL_OUT. The value of transconductance is variable and may be set for optimum performance.

9.3.4 Load Capacitance

For resonance at the correct frequency the crystal should be loaded with its specified load capacitance, which is defined for the crystal. This is the total capacitance across the crystal viewed from its terminals. BlueCore2-External provides some of this load with the capacitors Ct_{rim} and C_{int}. The remainder should be from the external capacitors labelled C_{t1} and C_{t2} , as Figure 9.24 indicates.

C_{t1} should be three times the value of C_{t2} for best noise performance. This maximises the signal swing, hence slew rate at XTAL_IN, to which all on-chip clocks are referred. Crystal load capacitance, C_l is calculated with the following formula:

$$C_l = C_{int} + \frac{C_{trim}}{2} + \frac{C_{t1} \cdot C_{t2}}{C_{t1} + C_{t2}}$$

Where:

C_{trim} = 3.4pF nominal (Mid range setting)

C_{int} = 1.5pF

Note:

(C_{int}) does not include the crystal internal self-capacitance; it is the driver self capacitance.

9.3.5 Frequency Trim

BlueCore2-External enables frequency adjustments to be made. This feature is typically used to remove initial tolerance frequency errors associated with the crystal. Frequency trim is achieved by adjusting the crystal load capacitance with on-chip trim capacitors, Ct_{rim}. The value of C_{trim} is set by a 6-bit word in the PS Key PSKEY_ANA_FTRIM (`0x1f6`). Its value is calculated thus:

$$C_{trim} = 110\,\text{fF} \times \text{PSKEY\_ANA\_FTRIM}$$

There are two C_{trim} capacitors, which are both connected to ground. When viewed from the crystal terminals, they appear in series so each least significant bit (LSB) increment of frequency trim presents a load across the crystal of 55fF.

The frequency trim is described by the following equation:

$$\frac{\Delta(F_X)}{F_X} = pullability \times 55 \times 10^{-3} (ppm / LSB)$$

Where F_X is the nominal crystal frequency, $\Delta(F_X)$ is the change in crystal frequency per LSB and pullability is a crystal parameter with units of ppm/pF. Total trim range is 63 times the value above.

If not specified, the pullability of a crystal may be calculated from its motional capacitance with the following equation:

$$\frac{\partial(F_X)}{\partial(C)} = F_X \cdot \frac{C_m}{4(C_l + C_0)^2}$$

Where:

C_0 = Crystal self capacitance (shunt capacitance)

Note:

It is a Bluetooth requirement that the frequency is always within ±20ppm. The trim range should be sufficient to pull the crystal within ±5ppm of the exact frequency. This leaves a margin of ±15ppm for frequency drift with ageing and temperature. A crystal with an ageing and temperature drift specification of better than ±15ppm is required.

9.3.6 Transconductance Driver Model

The crystal and its load capacitors should be viewed as a transimpedance element, whereby a current applied to one terminal generates a voltage at the other. The transconductance amplifier in BlueCore2-External uses the voltage at its input, XTAL_IN, to generate a current at its output, XTAL_OUT. Therefore, the circuit will oscillate if the transconductance, transimpedance product is greater than unity. For sufficient oscillation amplitude, the product should be greater than 3. The transconductance required for oscillation is defined by the following relationship:

$$g_m > \frac{3(C_{t1}+C_{trim})(C_{t2}+C_{trim})}{(2\pi F_x)^2 R_m((C_0+C_{int})(C_{t1}+C_{t2}+2C_{trim})+(C_{t1}+C_{trim})(C_{t2}+C_{trim}))^2}$$

BlueCore2-External guarantees a transconductance value of at least 2mA/V at maximum drive level.

Notes:

More drive strength is required for higher frequency crystals, higher loss crystals (larger Rm) or higher capacitance loading.

Optimum drive level is attained when the level at XTAL_IN is approximately 1V pk-pk. The drive level is determined by the crystal driver transconductance, by setting the PS KEY_XTAL_LVL (0x241).

9.3.7 Negative Resistance Model

An alternative representation of the crystal and its load capacitors is a frequency dependent resistive element. The driver amplifier may be considered as a circuit that provides negative resistance. For oscillation, the value of the negative resistance must be greater than that of the crystal circuit equivalent resistance. Although the BlueCore2-External crystal driver circuit is based on a transimpedance amplifier, an equivalent negative resistance may be calculated for it with the following formula:

$$R_{neg} > \frac{3(C_{t1}+C_{trim})(C_{t2}+C_{trim})}{g_m(2\pi F_x)^2(C_0+C_{int})((C_{t1}+C_{t2}+2C_{trim})+(C_{t1}+C_{trim})(C_{t2}+C_{trim}))^2}$$

This formula shows the negative resistance of the BlueCore2-External driver as a function of its drive strength.

The value of the driver negative resistance may be easily measured by placing an additional resistance in series with the crystal. The maximum value of this resistor (oscillation occurs) is the equivalent negative resistance of the oscillator.

	Min	Typ	Max
Frequency	8MHz	16MHz	32MHz
Initial Tolerance	-	±25ppm	-
Pullability	-	±20ppm/pF	-

Table 9.3: Crystal Specifications

PS Key values for PS KEY_ANA_FREQ (0x1fe) as a function of reference frequency:

Reference Freq (MHz)	PS Key Value (Hex)
8.00	49
8.25	72
8.50	05
8.75	6b
9.00	36
9.25	0c
9.50	78
9.75	11
10.00	43
10.25	66
10.50	2d
10.75	3b
11.00	17
11.25	4f
11.50	7e
11.75	1d
12.00	5b
12.25	56
12.50	4d
12.75	7a
13.00	15
13.25	4b
13.50	76
13.75	0d
14.00	7b
14.25	16
14.50	4c
14.75	79
15.00	12
15.25	44
15.50	69
15.75	32
16.00	04
16.25	68
16.50	31
16.75	03
17.00	67
17.25	2e
17.50	3c
17.75	18
18.00	50
18.25	41
18.50	62
18.75	25
19.00	2b
19.25	37
19.50	0f
19.75	7f

Reference Freq (MHz)	PS Key Value (Hex)
20.00	1e
20.25	5c
20.50	59
20.75	52
21.00	45
21.25	6a
21.50	35
21.75	0b
22.00	77
22.25	0e
22.50	7c
22.75	19
23.00	53
23.25	46
23.50	6d
23.75	3a
24.00	14
24.25	48
24.50	71
24.75	02
25.00	64
25.25	29
25.50	33
25.75	07
26.00	6f
26.25	3e
26.50	1c
26.75	58
27.00	51
27.25	42
27.50	65
27.75	2a
28.00	34
28.25	08
28.50	70
28.75	01
29.00	63
29.25	26
29.50	2c
29.75	38
30.00	10
30.25	40
30.50	61
30.75	22
31.00	24
31.25	28
31.50	30
31.75	00
32.00	60

Table 9.4: PS Key Values for PS KEY_ANA_FREQ

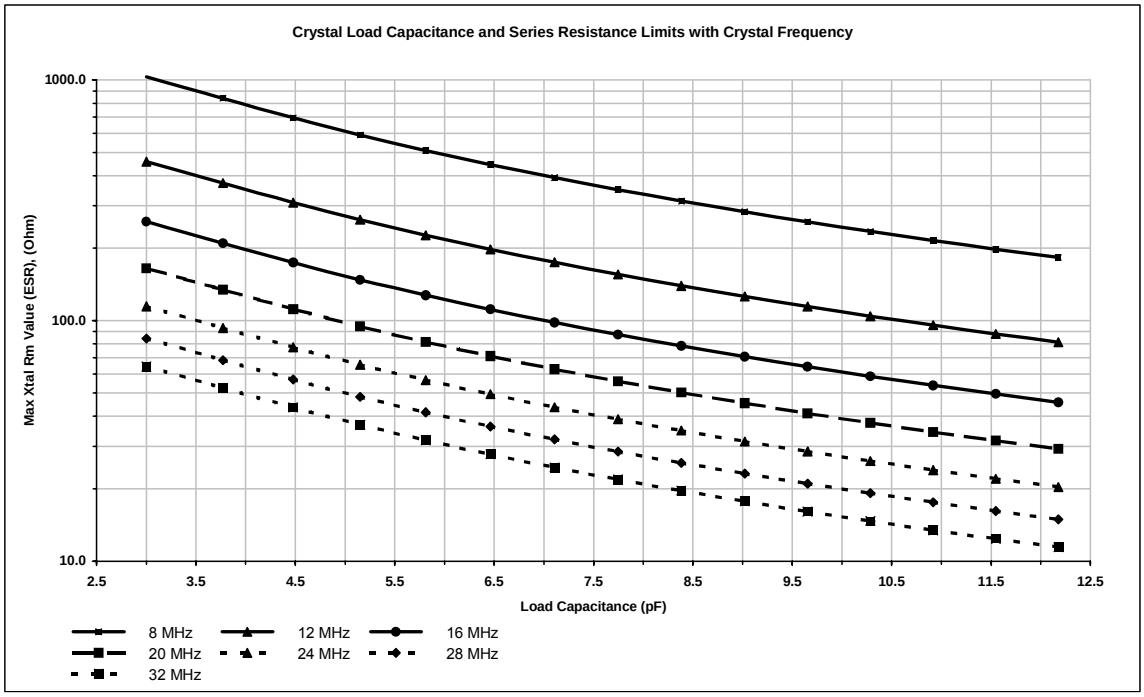


Figure 9.26: Crystal Load Capacitance and Series Resistance Limits with Crystal Frequency

Note:

Graph shows results for BlueCore2-External crystal driver at maximum drive level.

Conditions

Ctrim = 3.4pF centre value

Crystal Co = 2pF

Transconductance = 2mA/V

Loop gain = 3

Ct1/Ct2 = 3

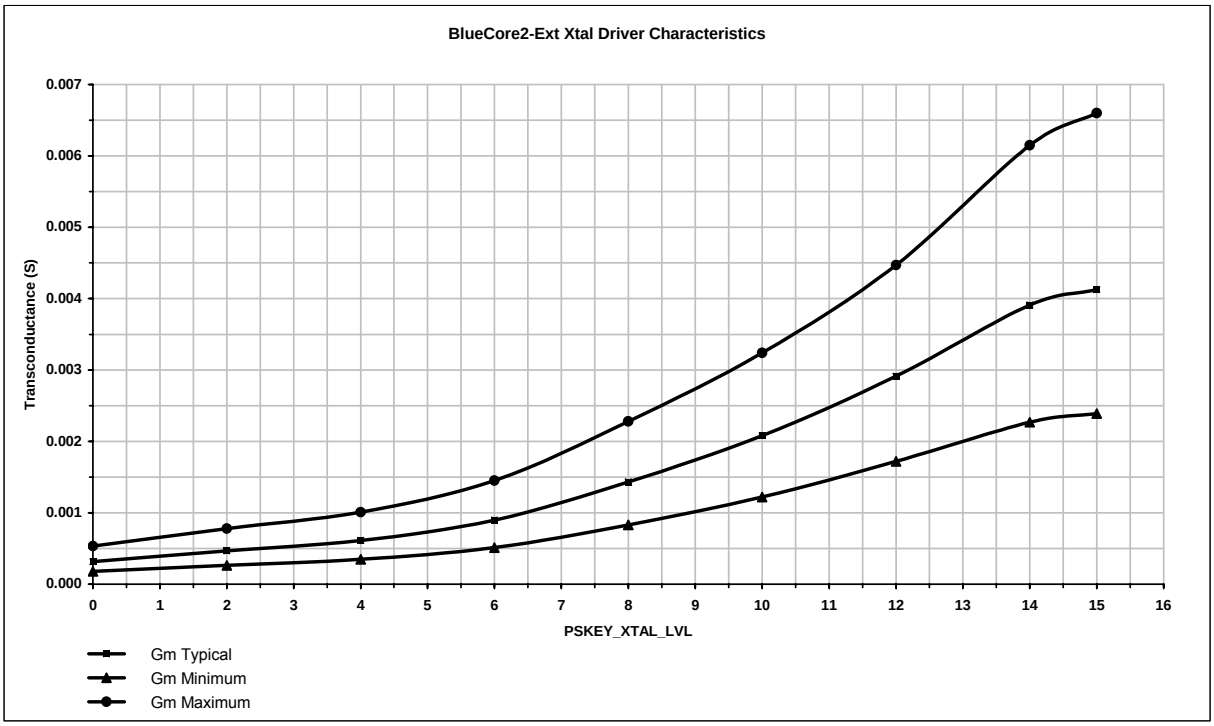


Figure 9.27: Crystal Driver Transconductance vs. Driver Level Register Setting

Note:

Drive level is set by PS Key PSKEY_XTAL_LVL (0x241).

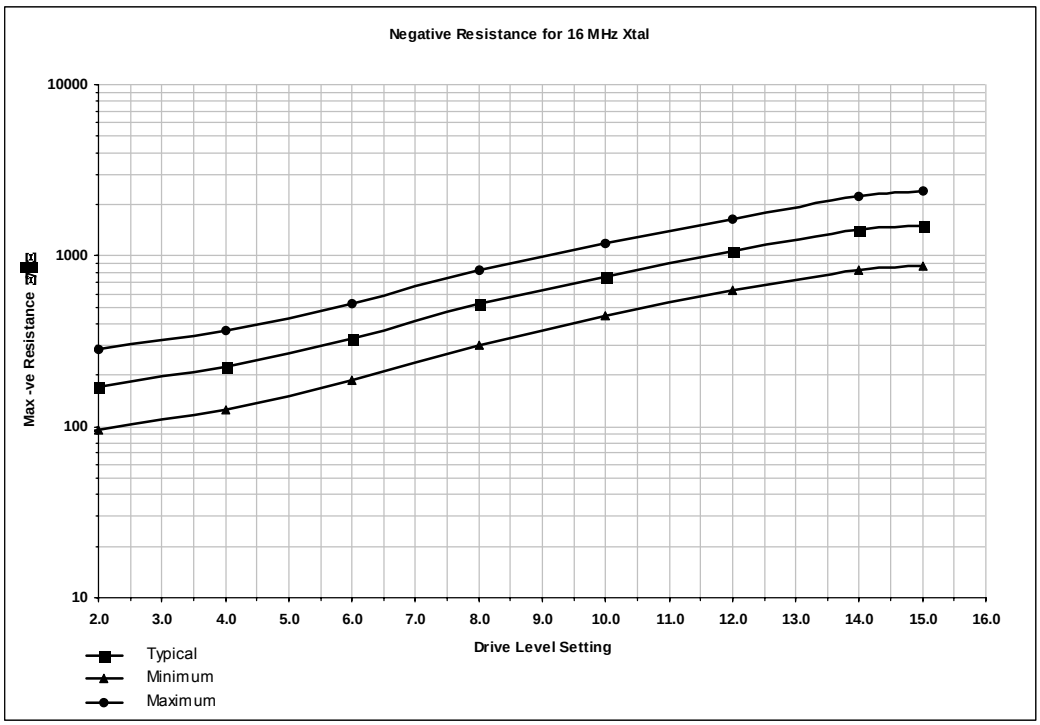


Figure 9.28: Crystal Driver Negative Resistance as a Function of Drive Level Setting

Crystal Parameters

Crystal frequency 16MHz

Crystal C0 = 0.75pF

Circuit Parameters

Ctrim = 8pF, maximum value

Ct1,Ct2 = 5pF (3.9pF plus 1.1 pF stray)

(Crystal total load capacitance 8.5pF)

9.4 Off-Chip Program Memory

The external memory port provides a facility to interface up to 8Mbits of 16-bit external memory. This off-chip storage is used to store BlueCore2-External settings and program code. Flash is the storage mechanism typically used by BlueCore2-External modules. However, external masked-ROM may also be used if the host takes over responsibility for storing configuration data.

The external memory port consists of 16 bi-directional data lines, D[15:0]; 19 output address lines, A[18:0] and three active low output control signals (WEB, CEB, REB). WEB is asserted when data is written to external memory. REB is asserted when data is read from external memory and the chip select line. CSB is asserted when any data transfer (read or write) is required. All of the external memory port connections are implemented using CMOS technology and use standard 0V and VDD_MEM (1.8-3.6V) signalling levels.

Parameter	Value
Data width	16-bit
Minimum total capacity	4Mbit (256kWord)
Maximum access time	90ns @125°C 50pF load
	110ns @85°C 10pF load

Table 9.5: Flash Device Hardware Requirements

In addition to these hardware requirements, particular care should be taken to ensure that the sector organisation of the extended memory has the correct format. A sector is defined as an individually erasable area of external Flash.

It is important to make sure that external memory devices meet certain minimum specifications. In addition particular care should be taken to ensure that the sector organisation of the extended memory has the correct format.

9.4.1 Minimum Flash Specification

The flash device used with BueCore2-External must meet the following criteria:

- Standard or extended form of either the JEDEC (AMD/Fujitsu/SST) or Intel command set.
- Access time must be ≤90ns @125°C 50pF load or ≤110ns @85°C 10pF load.
- Write strobe of 100ns.
- Accessible in word mode, i.e., via a 16-bit data bus.
- Support changing different bits within each word from 1 to 0 in at least two separate programming operations.
- Programming and erase times must have fixed upper limits.
- Must be bottom boot or uniform sector.
- Must have independently erasable sectors with (at least) the following boundaries (see Memory Map for more information).

Word Address	Size (kWords)
0x00000 - 0x01FFF	8
0x02000 - 0x02FFF	4
0x03000 - 0x03FFF	4
0x04000 - 0x07FFF	16
0x08000 - 0x0FFFF	32
0x10000 - 0x17FFF	32
0x18000 - ...	Don't care

Table 9.6: Flash Sector Boundaries

Important Note:

Satisfaction of these criteria is not sufficient for a particular device to be used; it must also support the Common Flash Interface described below or be supported in the BlueCore2-External firmware and host-side tools.

9.4.2 Common Flash Interface

The firmware can adapt automatically to work with some flash devices. If in addition to satisfying the minimum Flash specification described above, they meet the following criteria:

The device must support the Common Flash Interface CFI), as defined by JEDEC standard JESD68.

The device must return one of the following codes for either the Primary or Alternative Algorithm Command Set (offset 0x13b or 0x17 of the Query Structure Output).

Code	Descripton
0x0001	Intel/Sharp Extended Command Set
0x0002	AMD/Fujitsu Standard Command Set
0x0003	Intel Standard Command Set
0x0701	AMD/Fujitsu Extended Command Set

Table 9.7: Common Flash Interface Return Codes

The device must return one of the following patterns of Erase Block Region Information (beginning at offset 0x2d of the Query Structure Output):

If any of these criteria is not met, then the device will **not** work unless the device is supported by the BlueCore2-External firmware.

9.4.3 Memory Timing

Memory Write Cycle

Symbol	Parameter	Min	Typ	Max	Unit
t_{wc}	Write cycle time	300	-	-	ns
$t_{dat:su}$	Data set-up time	150	-	-	ns
$t_{dat:hd}$	Data hold time	150	-	-	ns
$t_{addr:su}$	Address set-up time	150	-	-	ns
$t_{we:low}$	WEB low	100	-	-	ns

Table 9.8: Memory Write Cycle

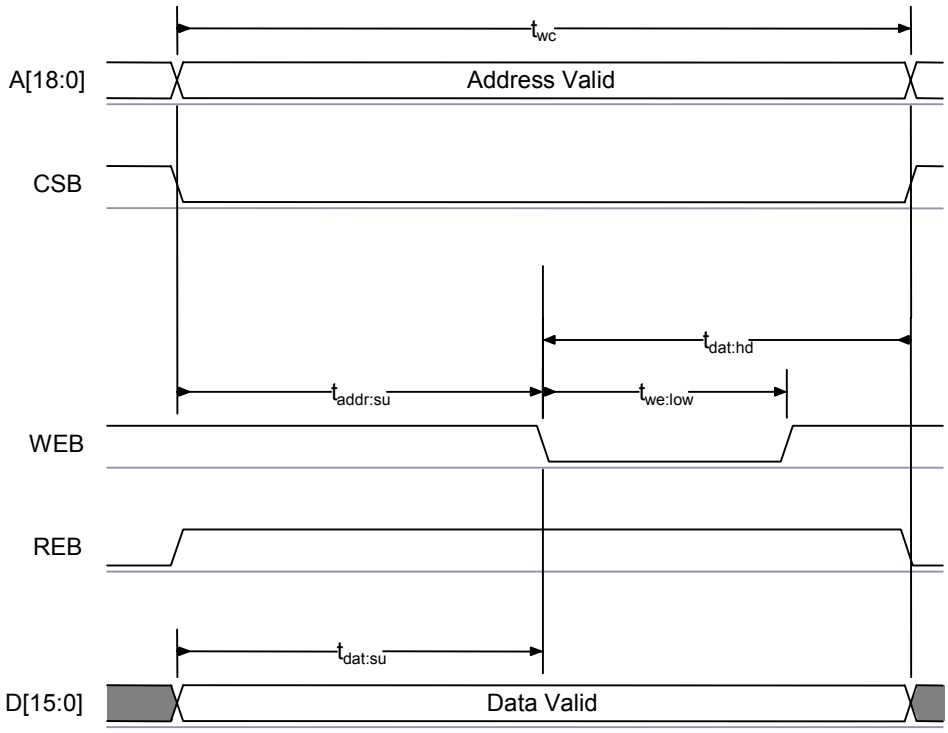


Figure 9.29 : Memory Write Cycle

Memory Read Cycle

Symbol	Parameter	Min(1)	Typ	Max(1)	Unit
t_{rc}	Read cycle time	114	125	-	ns
t_{aa}	Address access time	-	-	110	ns
t_{re}	Read enable access time	-	-	110	ns
$t_{dat:hd}$	Data hold time from address line	0	-	-	ns

Table 9.9: Memory Read Cycle

Note:

(1) Valid for temperatures between -40°C and +105°C

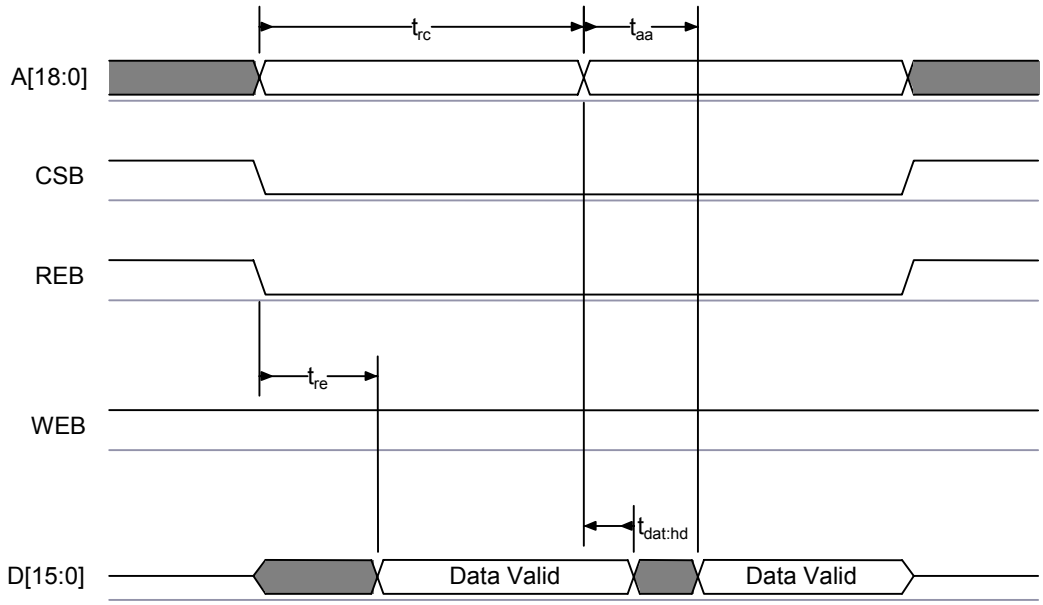


Figure 9.30: Memory Read Cycle

9.5 UART Interface

BlueCore2-External Universal Asynchronous Receiver Transmitter (UART) interface provides a simple mechanism for communicating with other serial devices using the RS232 standard(1).

Note:

(1) Uses RS232 protocol but voltage levels are 0V to VDD_PADS, (requires external RS232 transceiver IC)

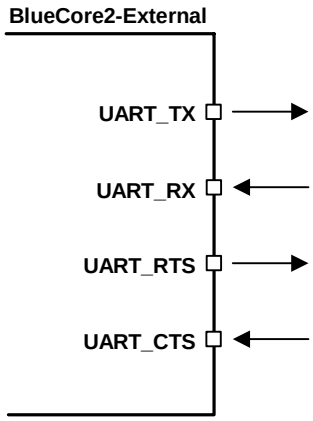


Figure 9.31: Universal Asynchronous Receiver

Figure 9.31 shows four signals used to implement the UART function. When BlueCore2-External is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators. All UART connections are implemented using CMOS technology and have signalling levels of 0V and VDD_PADS.

UART configuration parameters, such as baud rate and packet format, are set using BlueCore2-External software.

Note:

In order to communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

Parameter		**Parameter**
Baud Rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	1.5Mbaud (≤1%Error)
Flow Control		RTS/CTS or None
Parity		None, Odd or Even
Number of Stop Bits		1 or 2
Bits per channel		8

Table 9.10: Possible UART Settings

The UART interface is capable of resetting BlueCore2-External upon reception of a break signal. A Break is identified by a continuous logic low on the UART_RX terminal, as Figure 9.32 shows. If t_{BRK} is longer than the value, defined by the PS Key PSKEY_HOST_IO_UART_RESET_TIMEOUT, (0x1a4), a reset will occur. This feature allows a host to initialise the system to a known state. Also, BlueCore2-External can emit a Break character that may be used to wake the Host.

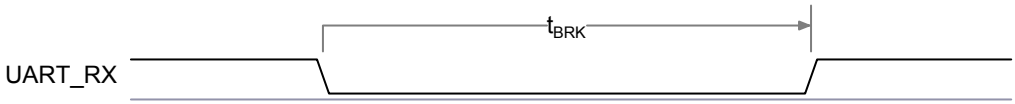


Figure 9.32: Break Signal

Note:

The DFU boot-loader must be loaded into the Flash device before the UART or USB interfaces can be used. This initial Flash programming can be done via the serial peripheral interface.

Table 9.11 shows a list of commonly used baud rates and their associated values for the PS Key PSKEY_UART_BAUD_RATE (0x204). There is no requirement to use these standard values. Any baud rate within the supported range can be set in the PS Key according to the following formula.

$$\text{Baud Rate} = \frac{\text{PSKEY\_UART\_BAUD\_RATE}}{0.004096}$$

Baud Rate	Persistent Store Value		Error
	Hex	Dec	
1200	0x0005	5	1.73%
2400	0x000a	10	1.73%
4800	0x0014	20	1.73%
9600	0x0027	39	-0.82%
19200	0x004f	79	0.45%
38400	0x009d	157	-0.18%
57600	0x00ec	236	0.03%
76800	0x013b	315	0.14%
115200	0x01d8	472	0.03%
230400	0x03b0	944	0.03%
460800	0x075f	1887	-0.02%
921600	0x0ebf	3775	0.00%
1382400	0x161e	5662	-0.01%

Table 9.11: Standard Baud Rates

9.6 USB Interface

BlueCore2-External USB devices contain a full-speed (12Mbits/s) USB interface, capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported. The set of USB endpoints implemented behave as specified in the USB section of the Bluetooth specification v1.1 and v1.2 part H:2.

As USB is a master-slave oriented system, Bluecore2-External only supports USB slave operation.

9.6.1 USB Data Connections

The USB data lines emerge as pins USB_D+ and USB_D- on the package. These terminals are connected to the internal USB I/O buffers of BlueCore2-External and therefore have a low output impedance. To match the connection to the characteristic impedance of the USB cable, series resistors must be connected to both USB_D+ and USB_D-.

9.6.2 USB Pull-up Resistor

BlueCore2-External features an internal USB pull-up resistor. This pulls the USB_D+ pin weakly high when BlueCore2-External is ready to enumerate. It signals to the PC that it is a full-speed (12Mbit/s) USB device.

The USB internal pull-up is implemented as a current source, and is compliant with section 7.1.5 of the USB specification v1.1. The internal pull-up pulls USB D+ high to at least 2.8V when loaded with a 15kΩ-5% pull-down resistor (in the hub/host) when VDD_PADS=3.1V). This presents a Thevenin resistance to the host of at least 900Ω. Alternatively, an external 1.5kΩ pull-up resistor can be placed between a PIO line and D+ on the USB cable. The firmware must be alerted to which mode is used by setting PS Key PSKEY_USB_PIO_PULLUP (0x2d0) appropriately. The default setting uses the internal pull-up resistor.

9.6.3 Power Supply

The USB specification dictates that the minimum output high voltage for USB data lines is 2.8V. To safely meet the USB specification, the voltage on the VDD_USB supply terminals must be an absolute minimum of 3.1V. CSR recommends 3.3V for optimal USB signal quality.

9.6.4 Self-Powered Mode

In self-powered mode, the circuit is powered from its own power supply and not from the VBUS (5V) line of the USB cable. It draws only a small leakage current (below 0.5mA) from VBUS on the USB cable. This is the easier mode for which to design, as the design is not limited by the power that can be drawn from the USB hub or root port. However, it requires that VBUS be connected to BlueCore2-External via a resistor network (R_{vb1} and R_{vb2}), so BlueCore2-External can detect when VBUS is powered up. BlueCore2-External will not pull USB_D+ high when VBUS is off.

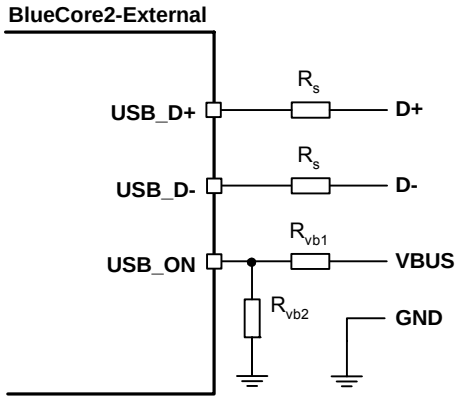


Figure 9.33: Connections to BlueCore2 External for Self-Powered Mode

The terminal marked USB_ON can be any free PIO pin. The PIO pin selected must be registered by setting PSKEY_USB_PIO_VBUS (0x2d1) to the corresponding pin number.

9.6.5 Bus-Powered Mode

In bus-powered mode the application circuit draws its current from the 5V VBUS supply on the USB cable. BlueCore2-External negotiates with the PC during the USB enumeration stage about how much current it is allowed to consume.

For Class 2 Bluetooth applications, CSR recommends that the regulator used to derive 3.3V from VBUS is rated at 100mA average current and should be able to handle peaks of 120mA without foldback or limiting. In bus-powered mode, BlueCore2-External requests 100mA during enumeration.

For Class 1 Bluetooth applications, the USB power descriptor should be altered to reflect the amount of power required. This is accomplished by setting the PS Key PSKEY_USB_MAX_POWER (0x2c6). This is higher than for a Class 2 application due to the extra current drawn by the Transmit RF PA.

When selecting a regulator, be aware that VBUS may go as low as 4.4V. The inrush current (when charging reservoir and supply decoupling capacitors) is limited by the USB specification (see USB 1.1 specification, section 7.2.4.1). Some applications may require soft-start circuitry to limit inrush current if more than 10μF is present between VBUS and GND.

The 5V VBUS line emerging from a PC is often electrically noisy. As well as regulation down to 3.3V and 1.8V, applications should include careful filtering of the 5V line to attenuate noise that is above the voltage regulator's bandwidth. Excessive noise on the 1.8V supply to the analogue supply pins of Bluecore2-External will result in reduced receive sensitivity and a distorted transmit signal.

9.6.6 Suspend Current

USB devices that run off VBUS must be able to enter a suspended state, whereby they consume less that 0.5mA from VBUS. The voltage regulator circuit itself should draw only a small quiescent current (typically less than 100μA) to ensure adherence to the suspend-current requirement of the USB specification. This is not normally a problem with modern regulators. Ensure that external LEDs and/or amplifiers can be turned off by BlueCore2-External. The entire circuit must be able to enter the suspend mode.

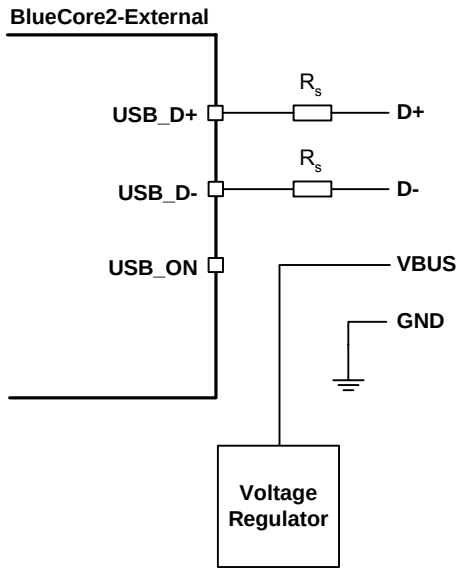


Figure 9.34: Connections to BlueCore2 External for Bus-Powered Mode

Identifier	Value	Function
R_s	27Ω nominal	Impedance matching to USB cable
R_{vb1}	47kΩ 5%	VBUS ON sense divider
R_{vb2}	22kΩ 5%	VBUS ON sense divider

Table 9.12: USB Interface Component Values

Note:

USB_ON is shared with BlueCore2-External's PIO terminals.

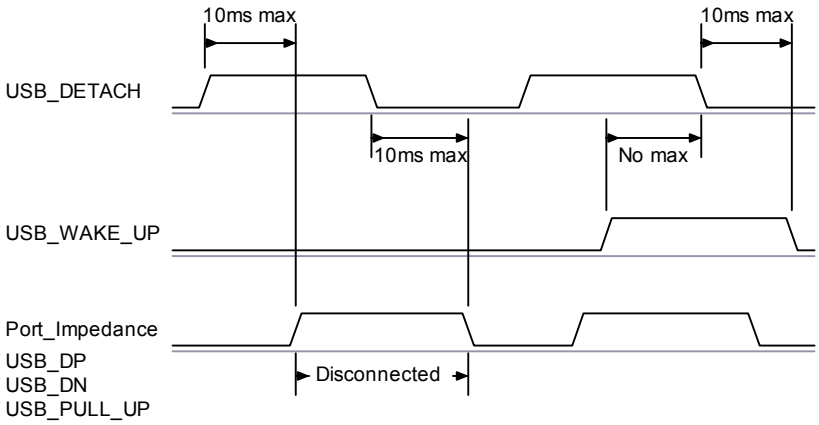


Figure 9.35: USB_DETACH and USB_WAKE_UP Signal

9.6.7 Detach and Wake_Up Signalling

BlueCore2-External can provide out-of-band signalling to a host controller by using the control lines called USB_DETACH and USB_WAKE_UP. These are outside the USB specification (no wires exist for them inside the USB cable), but can be useful when embedding BlueCore2-External into a circuit where no external USB is visible to the user. Both control lines are shared with PIO pins and can be assigned to any PIO pin by setting the PS Keys PSKEY_USB_PIO_DETACH (0x2ce) and PSKEY_USB_PIO_WAKEUP (0x2cf) to the selected PIO number).

USB_DETACH, is an input which, when asserted high, causes BlueCore2-External to put USB_D- and USB_D+ in a high-impedance state and turns off the pull-up resistor on USB_D+. This detaches the device from the bus and is logically equivalent to unplugging the device. When USB_DETACH is taken low, BlueCore2-External will connect back to USB and await enumeration by the USB host.

USB_WAKE_UP, is an active high output (used only when USB_DETACH is active) to wake up the host and allow USB communication to recommence. It replaces the function of the software USB WAKE_UP message (which runs over the USB cable proper), and cannot be sent while BlueCore2-External is effectively disconnected from the bus.

9.6.8 USB Driver

A USB Bluetooth device driver is required to provide a software interface between BlueCore2-External and Bluetooth software running on the host computer. Suitable drivers are available from www.csrsupport.com.

9.6.9 USB 1.1 Compliance

BlueCore2-External is qualified to the USB specification v1.1, details of which are available from www.usb.org. The specification contains valuable information on aspects such as PCB track impedance, supply inrush current and product labelling.

Although BlueCore2-External meets the USB specification, CSR cannot guarantee that an application circuit designed around the chip is USB compliant. The choice of application circuit, component choice and PCB layout all affect USB signal quality and electrical characteristics. The information in this document is intended as a guide and should be read in association with the USB specification, with particular attention being given to chapter 7. Independent USB qualification must be sought before an application is deemed USB compliant and can bear the USB logo. Such qualification can be obtained from a USB plugfest or from an independent USB test house.

Terminals USB_D+ and USB_D- adhere to the USB specification v1.1 (chapter 7) electrical requirements.

9.6.10 USB v2.0 Compatibility

BlueCore2-External is compatible with USB specification v2.0 host controllers; under these circumstances the two ends agree the mutually acceptable rate of 12Mbits/s according to the USB v2.0 specification.

9.7 Serial Peripheral Interface

BlueCore2-External uses 16-bit data and 16-bit address serial peripheral interface, where transactions may occur when the internal processor is running or is stopped. This section details the considerations required when interfacing to BlueCore2-External via the four dedicated serial peripheral interface terminals. Data may be written or read one word at a time or the auto increment feature may be used to access blocks.

9.7.1 Instruction Cycle

BlueCore2-External is the slave and receives commands on SPI_MOSI and outputs data on SPI_MISO. Table 9.13 shows the instruction cycle for an SPI transaction.

1	Reset the SPI interface	Hold SPI_CSB high for two SPI_CLK cycles
2	Write the command word	Take SPI_CSB low and clock in the 8-bit command
3	Write the address	Clock in the 16-bit address word
4	Write or read data words	Clock in or out 16-bit data word(s)
5	Termination	Take SPI_CSB high

Table 9.13: Instruction Cycle for an SPI Transaction

With the exception of reset, SPI_CSB must be held low during the transaction. Data on SPI_MOSI is clocked into the BlueCore2-External on the rising edge of the clock line SPI_CLK. When reading, BlueCore2-External will reply to the master on SPI_MISO with the data changing on the falling edge of the SPI_CLK. The master provides the clock on SPI_CLK. The transaction is terminated by taking SPI_CSB high.

Sending a command word and the address of a register for every time it is to be read or written is a significant overhead, especially when large amounts of data are to be transferred. To overcome this BlueCore2-External offers increased data transfer efficiency via an auto increment operation. To invoke auto increment, SPI_CSB is kept low, which auto increments the address, while providing an extra 16 clock cycles for each extra word to be written or read.

9.7.2 Writing to BlueCore2-External

To write to BlueCore2-External, the 8-bit write command (00000010) is sent first (C[7:0]) followed by a 16-bit address (A[15:0]). The next 16-bits (D[15:0]) clocked in on SPI_MOSI are written to the location set by the address (A). Thereafter for each subsequent 16-bits clocked in, the address (A) is incremented and the data written to consecutive locations until the transaction terminates when SPI_CSB is taken high.

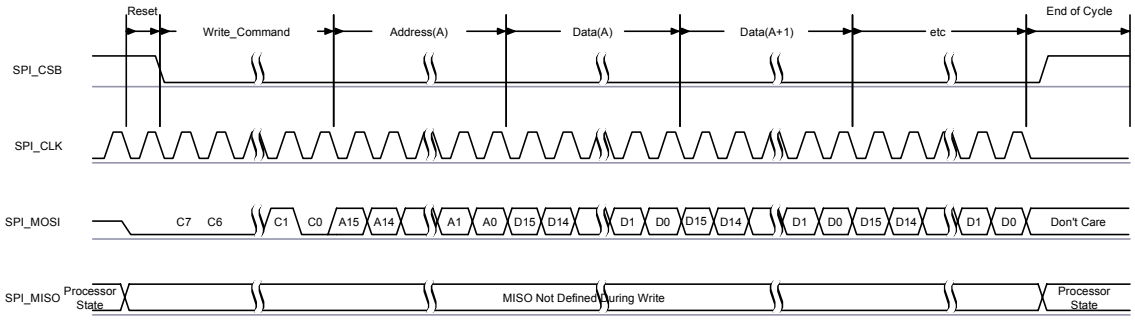


Figure 9.36: Write Operation

9.7.3 Reading from BlueCore2-External

Reading from BlueCore2-External is similar to writing to it. An 8-bit read command (00000011) is sent first (C[7:0]), followed by the address of the location to be read (A[15:0]). BlueCore2-External then outputs on SPI_MISO a check word during T[15:0] followed by the 16-bit contents of the addressed location during bits D[15:0].

The check word is composed of {command, address [15:8]}. The check word may be used to confirm a read operation to a memory location. This overcomes the problems encountered with typical serial peripheral interface slaves, whereby it is impossible to determine whether the data returned by a read operation is valid data or the result of the slave device not responding.

If SPI_CSB is kept low, data from consecutive locations is read out on SPI_MISO for each subsequent 16 clocks, until the transaction terminates when SPI_CSB is taken high.

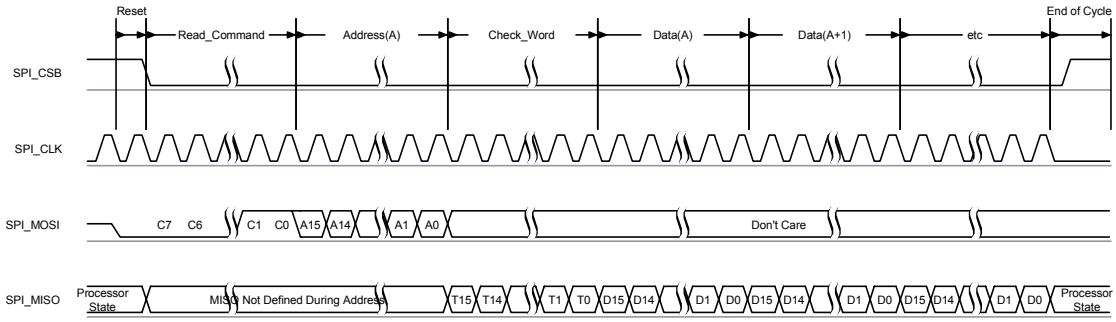


Figure 9.37: Read Operation

9.7.4 Multi Slave Operation

BlueCore2-External should not be connected in a multi slave arrangement by simple parallel connection of slave MISO lines. When BlueCore2-External is deselected (SPI_CSB = 1), the SPI_MISO line does not float, instead, BlueCore2-External outputs 0 if the processor is running or 1 if it is stopped.

9.8 PCM Interface

Pulse Code Modulation (PCM) is the standard method used to digitise human voice patterns for transmission over digital communication channels. Through its PCM interface, BlueCore2-External has hardware support for continual transmission and reception of PCM data, thus reducing processor overhead for wireless headset applications. BlueCore2-External offers a bi-directional digital audio interface that routes directly into the baseband layer of the on-chip firmware. It does not pass through the HCI protocol layer.

Hardware on BlueCore2-External allows the data to be sent to and received from a SCO connection.

Up to three SCO connections can be supported by the PCM interface at any one time.(1)

Note:

(1) Subject to firmware support, contact CSR for current status.

BlueCore2-External can operate as the PCM interface Master generating an output clock of 128, 256 or 512kHz. When configured as PCM interface slave it can operate with an input clock up to 2048kHz. BlueCore2-External is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13 or 16-bit linear, 8-bit μ-law or A-law companded sample formats at 8ksamples/s and can receive and transmit on any selection of three of the first four slots following PCM_SYNC. The PCM configuration options are enabled by setting the PS Key PS KEY_PCM_CONFIG (0x1b3).

BlueCore2-External interfaces directly to PCM audio devices includes the following:

- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
- OKI MSM7705 four channel A-law and μ-law CODEC
- Motorola MC145481 8-bit A-law and μ-law CODEC
- Motorola MC145483 13-bit linear CODEC

BlueCore2-External is also compatible with the Motorola SSI™ interface

9.8.1 PCM Interface Master/Slave

When configured as the Master of the PCM interface, BlueCore2-External generates PCM_CLK and PCM_SYNC.

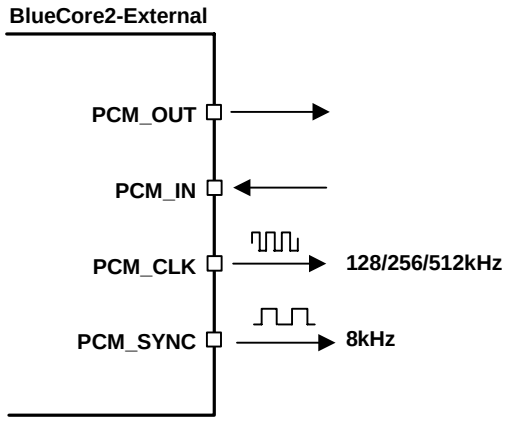


Figure 9.38: BlueCore2 External as PCM Interface Master

When configured as the Slave of the PCM interface, BlueCore2-External accepts PCM_CLK rates up to 2048kHz.

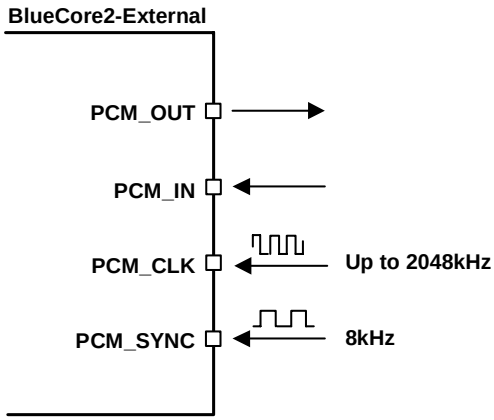


Figure 9.39: BlueCore2-External as PCM Interface Slave

Notes:

A minimum of three clock cycles needs to be applied before a SCO is established

9.8.2 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When BlueCore2-External is configured as PCM Master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8-bits long. When BlueCore2-External is configured as PCM Slave, PCM_SYNC may be from two consecutive falling edges of PCM_CLK to half the PCM_SYNC rate (i.e., 62.5µs) long.

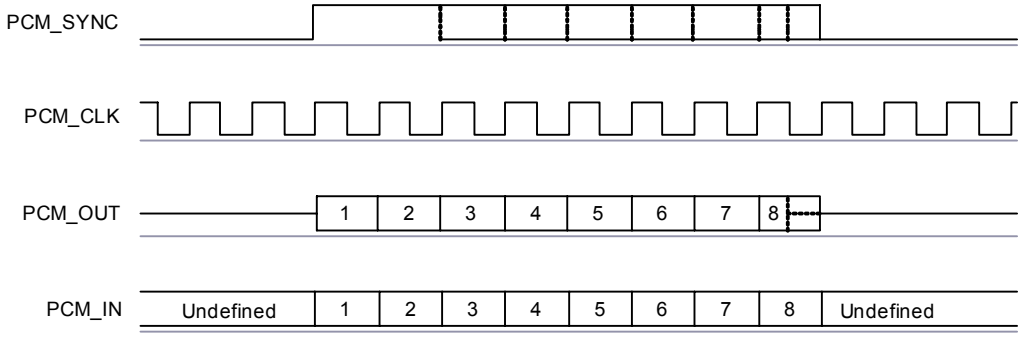


Figure 9.40: Long Frame Sync (Shown with 8-bit Companded Sample)

BlueCore2-External samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

9.8.3 Short Frame Sync

In Short Frame Sync the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

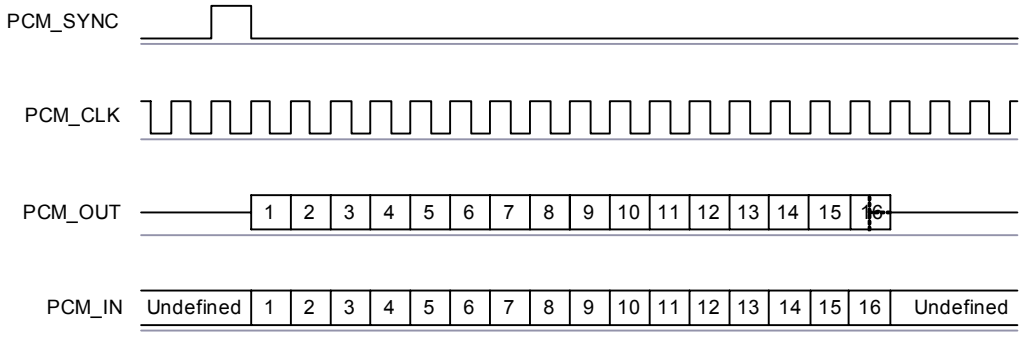


Figure 9.41: Short Frame Sync (Shown with 16 bit Sample)

As with Long Frame Sync, BlueCore2-External samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

9.8.4 Multi-Slot Operation

More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCO connections can be carried over any of the first four slots.

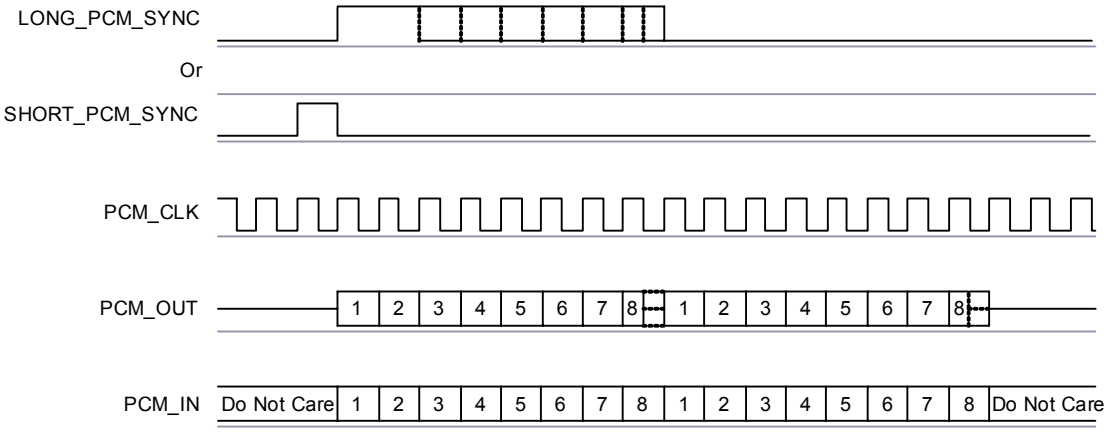


Figure 9.42: Multi slot Operation with Two Slots and 8-bit Companded Samples

9.8.5 GCI Interface

BlueCore2-External is compatible with the General Circuit Interface, a standard synchronous 2B+D ISDN timing interface. The two 64Kbps B channels can be accessed when this mode is configured. In the GCI interface two clock cycles are required for each bit of the voice sample. The voice sample format is 8-bit companded. As for the standard PCM interface up to 3 SCO connections can be carried over the first four slots.

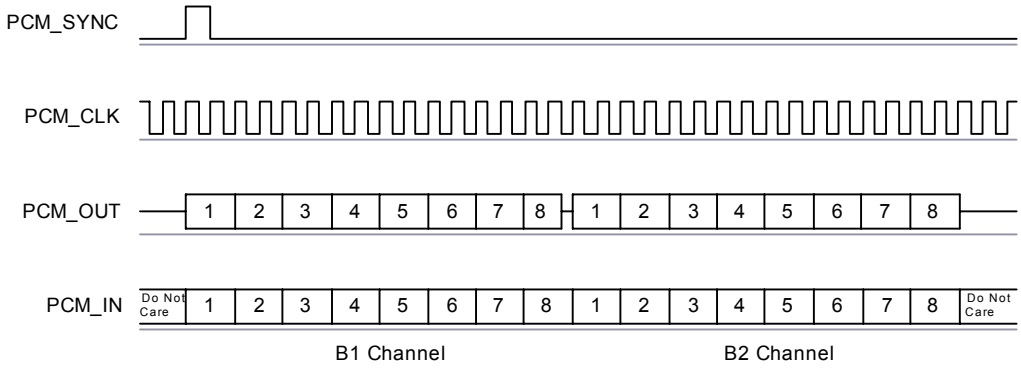


Figure 9.43: GCI Interface

The start of frame is indicated by PCM_SYNC and runs at 8kHz. With BlueCore2-External in Slave mode, the frequency of PCM_CLK can be up to 4.096MHz. In order to configure the PCM interface to work in GCI mode it is necessary to set GCI_MODE bit in PSKEY_PCM_CONFIG32. The SAMPLE_FORMAT bits should be set to `0x0b01` to allow for the double clocking of each.

9.8.6 Slots and Sample Formats

BlueCore2-External can receive and transmit on any selection of the first four slots following each sync pulse. Slot durations can be either 8 or 16 clock cycles. Durations of 8 clock cycles may only be used with 8-bit sample formats. Durations of 16 clocks may be used with 8, 13 or 16-bit sample formats.

Bluecore2-External supports 13-bit linear, 16-bit linear and 8-bit μ-law or A-law sample formats. The sample rate is 8ksamples/s. The bit order may be little or big endian. When 16-bit slots are used, the 3 or 8 unused bits in each slot may be filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some Motorola CODECs.

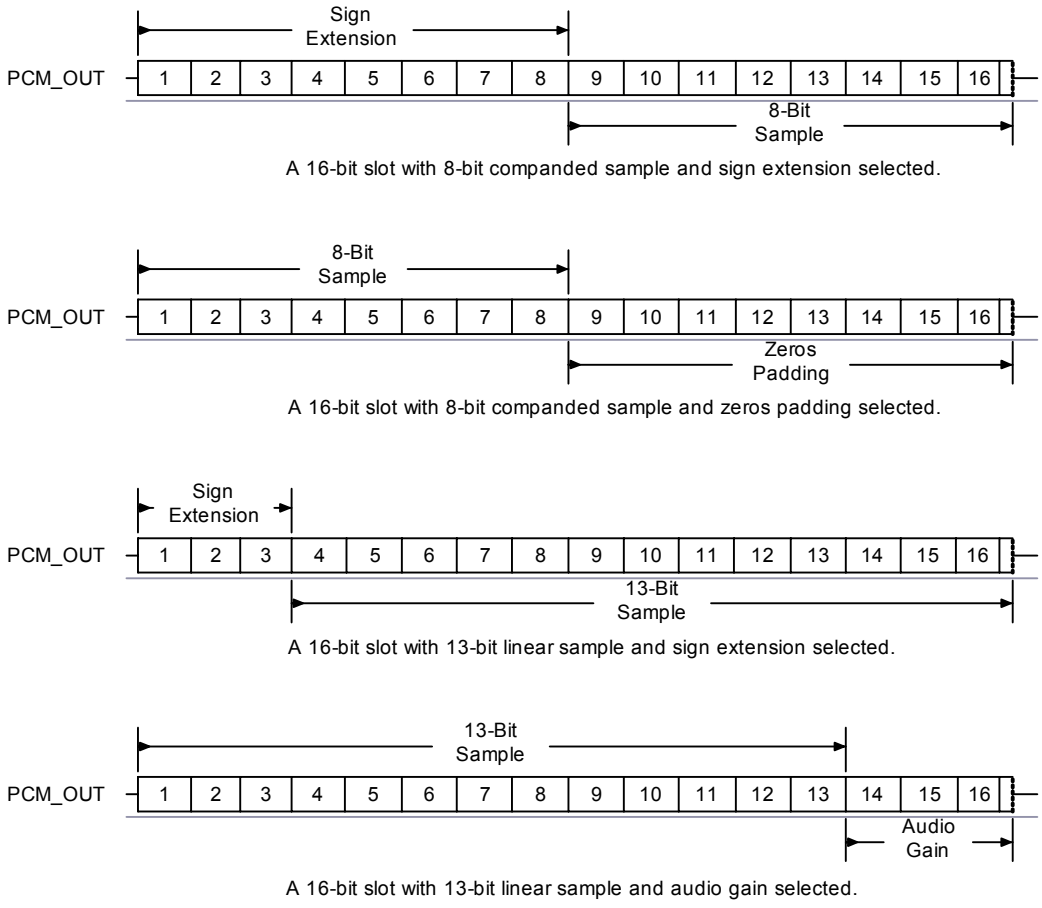


Figure 9.44: 16 bit Slot Length and Sample Formats

9.8.7 Additional Features

BlueCore2-External has a mute facility that forces PCM_OUT to be 0. In Master mode, PCM_SYNC may also be forced to 0 while keeping PCM_CLK running (which some CODECS use to control power-down).

9.8.8 PCM Timing Information

Symbol	Parameter	Min[1]	Typ	Max[1]	Unit
fmclk	PCM_CLK frequency	-	128 256 512	-	kHz
-	PCM_SYNC frequency	-	8		kHz
Tmclkh[2]	PCM_CLK high	980	-	-	ns
Tmclkl[2]	PCM_CLK low	730	-		ns
tdmclksynch	Delay time from PCM_CLK high to PCM_SYNC high	-	-	20	ns
tdmclkpout	Delay time from PCM_CLK high to valid PCM_OUT	-	-	20	ns
tdmclklsyncl	Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only)	-	-	20	ns
tdmclkhsyncl	Delay time from PCM_CLK high to PCM_SYNC low	-	-	20	ns
tdmclklpoutz	Delay time from PCM_CLK low to PCM_OUT high impedance	-	-	20	ns
tdmclkhpoutz	Delay time from PCM_CLK high to PCM_OUT high impedance	-	-	20	ns
tsupinclkl	Set-up time for PCM_IN valid to PCM_CLK low	30	-	-	ns
thpinclkl	Hold time for PCM_CLK low to PCM_IN invalid	30	-	-	ns
tr	Edge rise time (C_l = 50 pf, 10-90 %)	-	-	15	ns
tf	Edge fall time (C_l = 50 pf, 10-90 %)	-	-	15	ns

Table 9.14: PCM Master Timing

Notes:

(1) Valid for temperatures between -40°C and +105°C

(2) Assumes normal system clock operation. Figures will vary during low power modes, when system clock speeds are reduced.

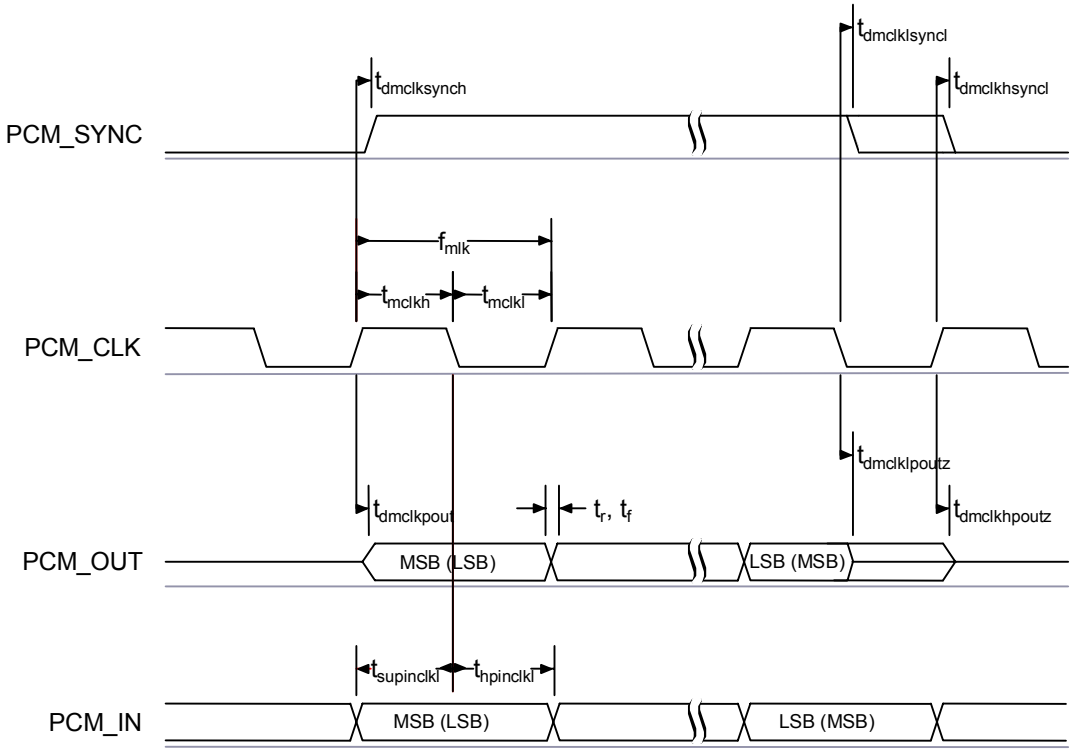


Figure 9.45: PCM Master Timing

Symbol	Parameter	Min(1)	Typ	Max(1)	Unit
fsclk	PCM clock frequency (Slave mode: input)	64	-	2048	kHz
fsclk	PCM clock frequency (GCI mode)	128	-	4096	kHz
tsclkl	PCM_CLK low time	200	-	-	ns
tsclkh	PCM_CLK high time	200	-	-	ns
thsclksynch	Hold time from PCM_CLK low to PCM_SYNC high	30	-	-	ns
tsusclksynch	Set-up time for PCM_SYNC high to PCM_CLK low	30	-	-	ns
tdpout	Delay time from PCM_SYNC or PCM_CLK whichever is later, to valid PCM_OUT data (Long Frame Sync only)	-	-	20	ns
tdsclkhpout	Delay time from CLK high to PCM_OUT valid data	-	-	20	ns
tdpoutz	Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	20	ns
tsupinsclkl	Set-up time for PCM_IN valid to CLK low	30	-	-	ns
thpinsclkl	Hold time for PCM_CLK low to PCM_IN invalid	30	-		ns
tr	Edge rise time (C_l = 50 pF, 10-90 %)	-	-	15	ns
Tf	Edge fall time (C_l = 50 pF, 10-90 %)	-	-	15	ns

Table 9.15: PCM Slave Timing

Note:

(1) Valid for temperatures between -40°C and +105°C

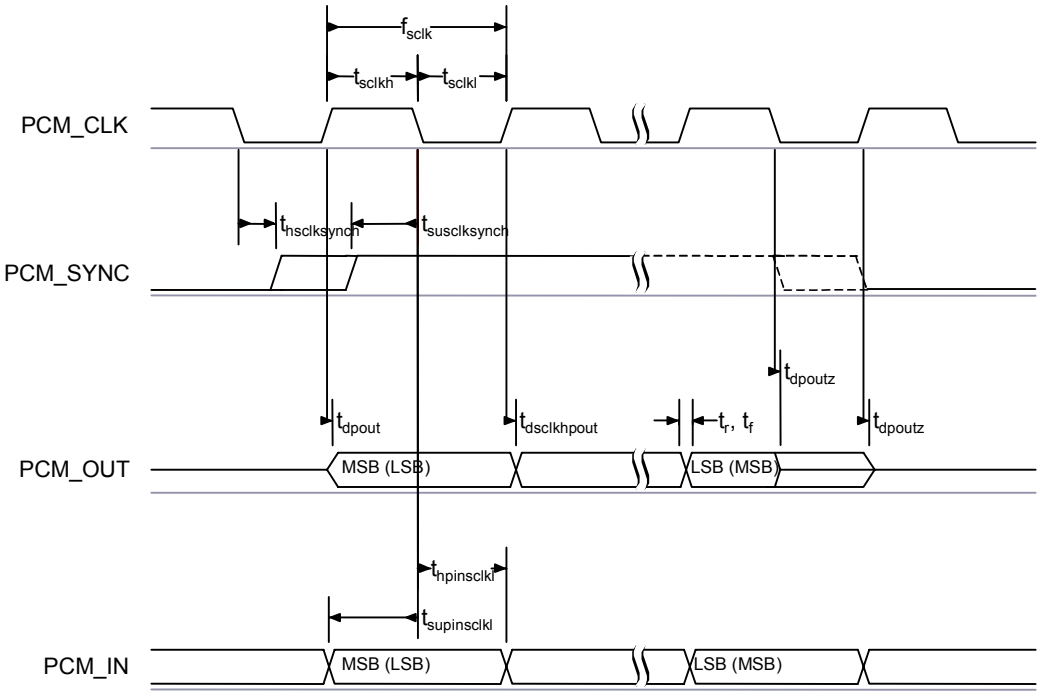


Figure 9.46: PCM Slave Timing

9.8.9 PCM Configuration PS Key

The PCM configuration is set using PSKEY_PCM_CONFIG32. Table 9.16 details this PS Key(1). The default for this PSKEY is `0x00000000`, i.e., 13-bit linear voice format, long frame sync and interface master generating 256kHz PCM_CLK with no tristating of PCM_OUT.

Name	Bit Position	Description
-	0	Set to 0.
SLAVE_MODE_EN	1	0 selects master mode with internal generation of PCM_CLK and PCM_SYNC. 1 selects slave mode requiring externally generated PCM_CLK and PCM_SYNC.
SHORT_SYNC_EN	2	0 selects long frame sync (rising edge indicates start of frame), 1 selects short frame sync (falling edge indicates start of frame).
-	3	Set to 0.
SIGN_EXTEND_EN	4	0 selects padding of 8 or 13-bit voice sample into a 16-bit slot by inserting extra lsbs, 1 selects sign extension. When padding is selected with 13-bit voice sample, the 3 padding bits are the audio gain setting; with 8-bit samples the 8 padding bits are zeroes.
LSB_FIRST_EN	5	0 transmits and receives voice samples msb first, 1 uses lsb first.
TX_TRISTATE_EN	6	0 drives PCM_OUT continuously, 1 tristates PCM_OUT immediately after the falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is not active.
TX_TRISTATE_RISING_EDGE_EN	7	0 tristates PCM_OUT immediately after the falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is also not active. 1 tristates PCM_OUT after the rising edge of PCM_CLK.
SYNC_SUPPRESS_EN	8	0 enables PCM_SYNC output when master, 1 suppresses PCM_SYNC whilst keeping PCM_CLK running. Some CODECs utilise this to enter a low power state.
GCI_MODE_EN	9	1 enables GCI mode.
MUTE_EN	10	1 forces PCM_OUT to 0.
-	[20:16]	Set to `(bits 00000)`
MASTER_CLK_RATE	[22:21]	Selects `128 (bits 01)`, `256 (bits 00)`, `512 (bits 10)` kHz PCM_CLK frequency when master.
-	[26:23]	Ignored. Set to `(bits 0000)`.
SAMPLE_FORMAT	[28:27]	Selects between 13 `(bits 00)`, `16(bits 01)`, 8 `(bits 10)` bit sample with 16 cycle slot duration or 8 `(bits 11)` bit sample with 8 cycle slot duration.

Table 9.16: Setting PCM Configuration Using PSKEY_PCM_CONFIG32

Note:

(1) Subject to firmware support; contact CSR for current status.

9.9 PIO Interface

The Parallel Input Output (PIO) Port is a general-purpose I/O interface to BlueCore2-External. The port consists of twelve programmable, bi-directional I/O lines, PIO[11:0].

Programmable I/O lines can be accessed either via an embedded application running on BlueCore2-External or via private channel or manufacturer-specific HCI commands.

PIO[0]/RXEN

This is a multifunction terminal. Its function is selected by setting the PS Key PSKEY_TX/RX_PIO_CONTROL (0x209). It can be used as a programmable I/O, however it will normally be used to control the radio front-end receive switch.

PIO[1]/TXEN

This is a multifunction terminal. Its function is selected by setting the PS Key PSKEY_TX/RX_PIO_CONTROL (0x209). It can be used as a programmable I/O, however it will normally be used to control the radio front end transmit switch. Refer to CSR documentation for BlueCore2-External software.

PIO[2]/USB_PULL_UP(1)

This is a multifunction terminal. The function depends on whether BlueCore2-External is a USB or UART capable version. On UART versions, this terminal is a programmable I/O. On USB versions, it can drive a pull-up resistor on USB_D+. For application using external RAM this terminal may be programmed for chip select.

PIO[3]/USB_WAKE_UP(1)

This is a multifunction terminal. On UART versions of BlueCore2-External this terminal is a programmable I/O. On USB versions, its function is selected by setting the PS Key PSKEY_USB_PIO_WAKEUP (0x2cf) either as a programmable I/O or as a USB_WAKE_UP function.

PIO[4]/USB_ON(1)

This is a multifunction terminal. On UART versions of BlueCore2-External this terminal is a programmable I/O. On USB versions, the USB_ON function is also selectable (see USB Interface section 9.6).

PIO[5]/USB_DETACH(1)

This is a multifunction terminal. On UART versions of BlueCore2-External this terminal is a programmable I/O. On USB versions, the USB_DETACH function is also selectable (see USB Interface section 9.6).

PIO[6]/CLK_REQ

This is multifunction terminal, its function is determined by PS Keys. Using PSKEY_CLOCK_REQUEST_ENABLE, (0x246) this terminal can be configured to be low when BlueCore2-External is in Deep Sleep and high when a clock is required. The clock must be supplied within 4ms of the rising edge of PIO[6] to avoid losing timing accuracy in certain Bluetooth operating modes.

PIO[7]

Programmable I/O terminal.

PIO[8]

Programmable I/O terminal.

PIO[9]

Programmable I/O terminal.

PIO[10]

Programmable I/O terminal.

PIO[11]

Programmable I/O terminal.

Note:

A USB functions can be software mapped to any PIO terminal.

9.10 Power Supplies

VDD_CORE

Power for digital circuitry.

VDD_RADIO

Power for RF circuitry.

VDD_VCO

Power for VCO and synthesiser circuitry.

VDD_ANA

Power for analogue circuitry.

To isolate the VCO from supply noise, a filter circuit is required. Refer to CSR documentation for supply decoupling.

VDD_PADS

Power for I/O circuitry.

VDD_MEM

Power for external memory port circuitry.

VSS_CORE

Ground for digital circuitry.

VSS_RADIO

Ground for RF circuitry.

VSS_VCO

Ground for VCO and synthesiser circuitry.

VSS_PADS

Ground for I/O circuitry.

VSS_MEM

Ground for external memory port circuitry.

NC

To guarantee correct operation, NC must not be connected externally. CSR recommends that unconnected terminals be placed on unconnected pads to ensure mechanical robustness.

RESET

Tie to VSS either directly or via a 1kΩresistor.

10 Schematics

10.1 VFBGA, LGA and LFBGA Package

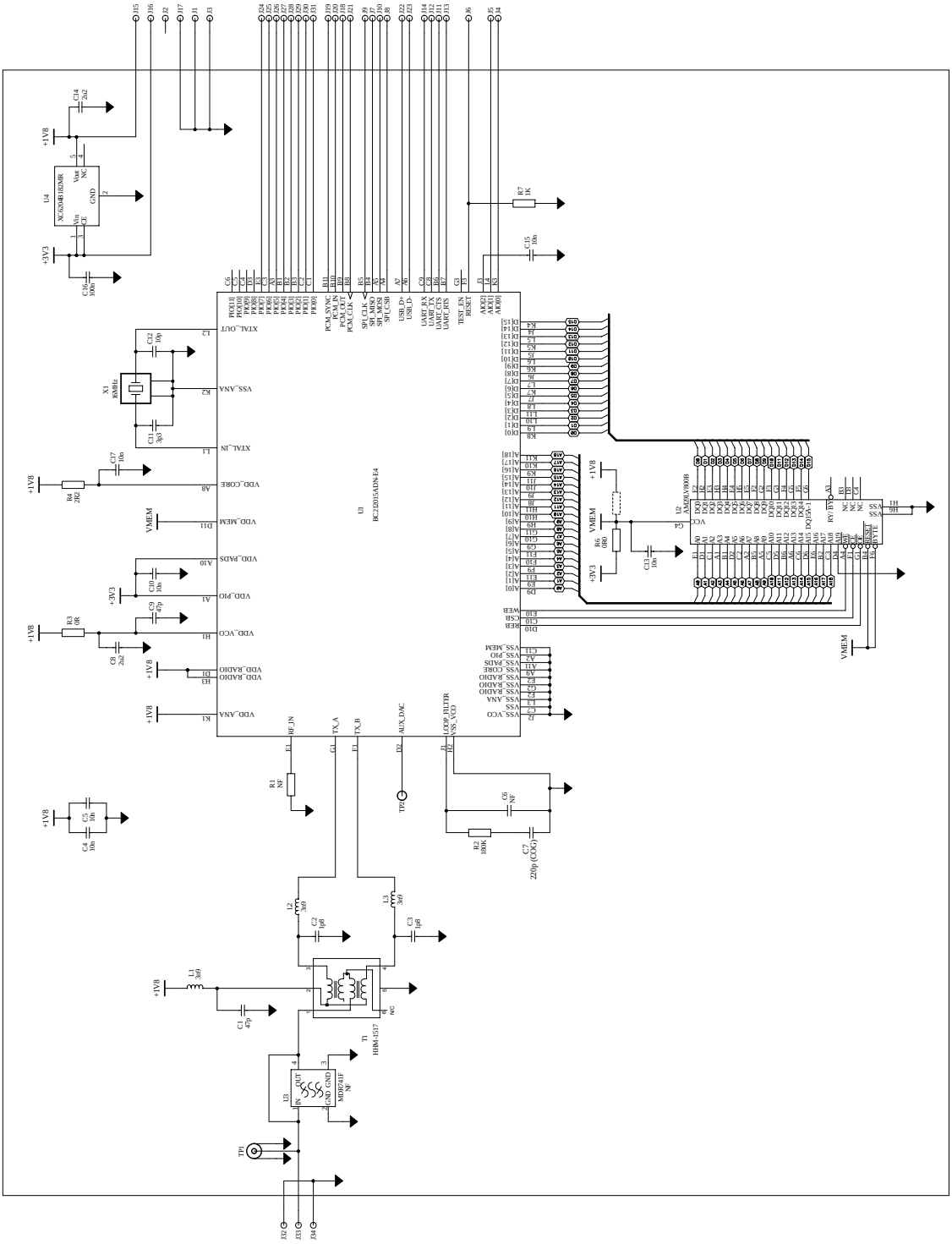


Figure 10.1: Circuit Used for Data Book Characterisation

BlueCore2-External Characterisation Circuit BOM

Item No.	Qty Req.	Circuit Ref.	Description	Value	Tol	Voltage	Material	Package	Part Type	Manufacturer	Manufacturers Part No.
1	1	PCB	4 Layer				FR4		PCB	Express Circuits	DEV-PC-1129A
2	1	U2	FLASH MEMORY				CMOS	TFBGA6x9	FLASH MEM	AMD	AM29LV800BB-90RWAI
3	1	U1	BlueCore2				CMOS	BGA11x11 96 ball 0.65mm Pt	BLUECORE2	CSR	BC212015BESDN-E4 Lot No. DC7283.00 DTE 0215
4	1	U4	Voltage regulator	1v8				SOT-23-5	REG	TOREX	XC6204B182MR
5	1	U3	Not Fitted								
6	1	X1	SURFACE MOUNT CRYSTAL	16 MHz				TSX-10A (4x2.5mm)	CRYSTAL	Toyocom	TN4-25820
7	1	T1	Surface mount balun	2.4GHz				2012		TDK	HHM-1517
8	2	C2, C3	CERAMIC CAPACITOR	1p8	+/-0.25pF	50V	COG	0402	CAP	Rohm Murata	MCH155A1R8CK GRM36C0G1R8C50PT
9	1	C11	CERAMIC CAPACITOR	3p3	+/-0.25pF	50V	COG	0402	CAP	Rohm Murata	MCH155A3R3CK GRM36C0G3R3C50PT
10	1	C12	CERAMIC CAPACITOR	10p	5%	50V	COG	0402	CAP	Rohm Murata	MCH155A100JK GRM36C0G100J50PT
11	2	C1, C9	CERAMIC CAPACITOR	47p	5%	50V	COG	0402	CAP	Rohm Murata	MCH155A470JK GRM36C0G470J50PT
12	1	C7	CERAMIC CAPACITOR	220p	5%	50V	COG	0603	CAP	Rohm Murata	MCH185A221JK GRM39C0G221J50PT
13	5	C4, C5, C10, C13, C17	CERAMIC CAPACITOR	10n	+80/-20%	50V	X7R	0402	CAP	Rohm Murata	
14	2	C15, C16	CERAMIC CAPACITOR	100n	+80/-20%	16V	X7R	0603	CAP	Murata TDK	
15	2	C8, C14	CERAMIC CAPACITOR	2u2	+80/-20%	16V	X7R	0805	CAP	TDK	CC0805CY5V225ZTR
16	1	C6		NF				0402			
17	2	R3, R6	THICK FILM RESISTOR	0R				0402	RES	Rohm	MCR01EZH000E
18	1	R4	THICK FILM RESISTOR	2R2	5%			0402	RES	Rohm	MCR01MZSJ2R2E
19	1	R7	THICK FILM RESISTOR	1k	5%			0402	RES	Rohm	MCR01MZSJ102E
20	1	R2	THICK FILM RESISTOR	180k	5%			0402	RES	Rohm	MCR01MZSJ184E
21	1	R1	THICK FILM RESISTOR	NF				0402			
22	3	L1, L2, L3	Thin Film INDUCTOR	3n9	0.2nH 01.nH			0402	IND	Meggit Murata	3640 1E3n9A LQP10A3N9B00

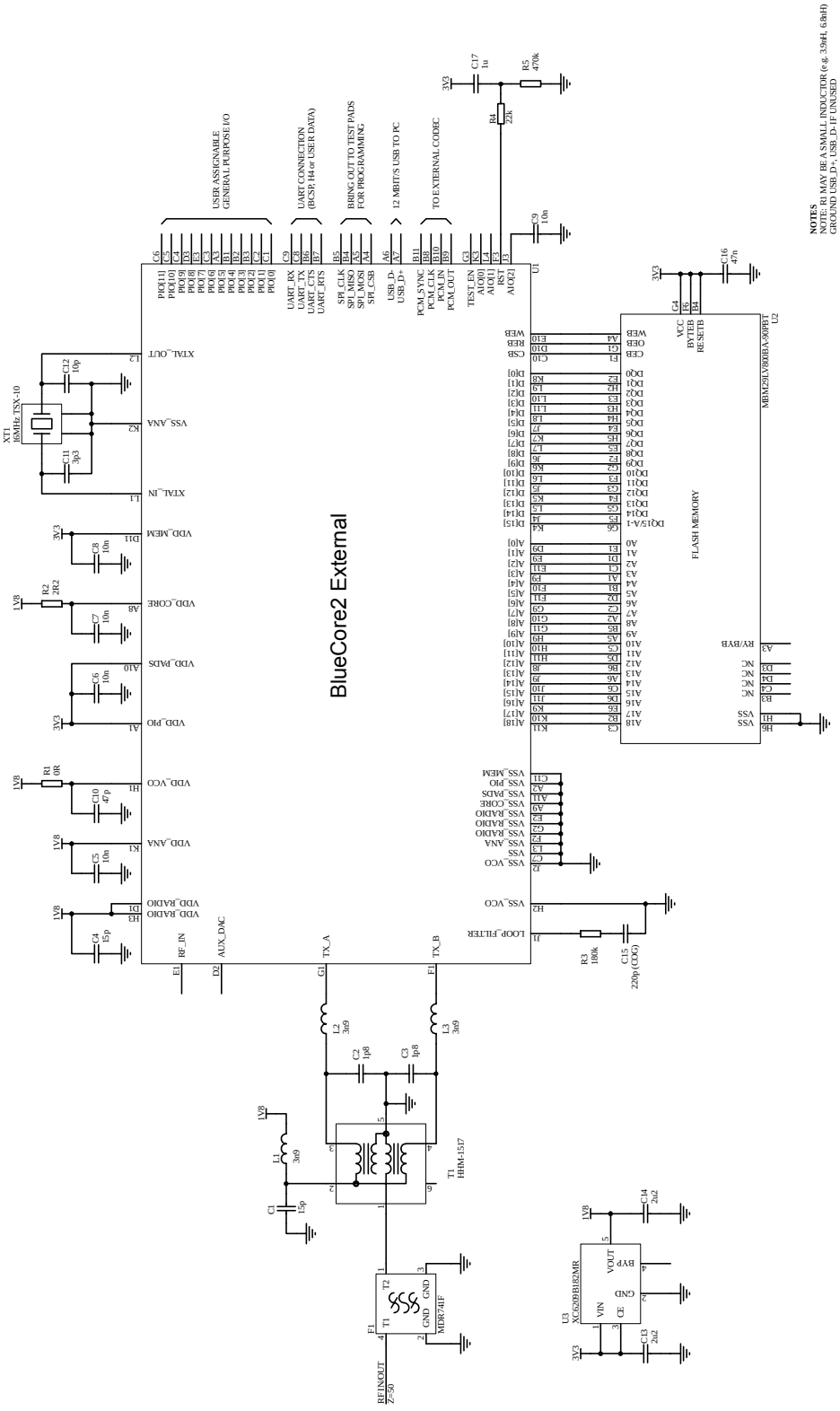
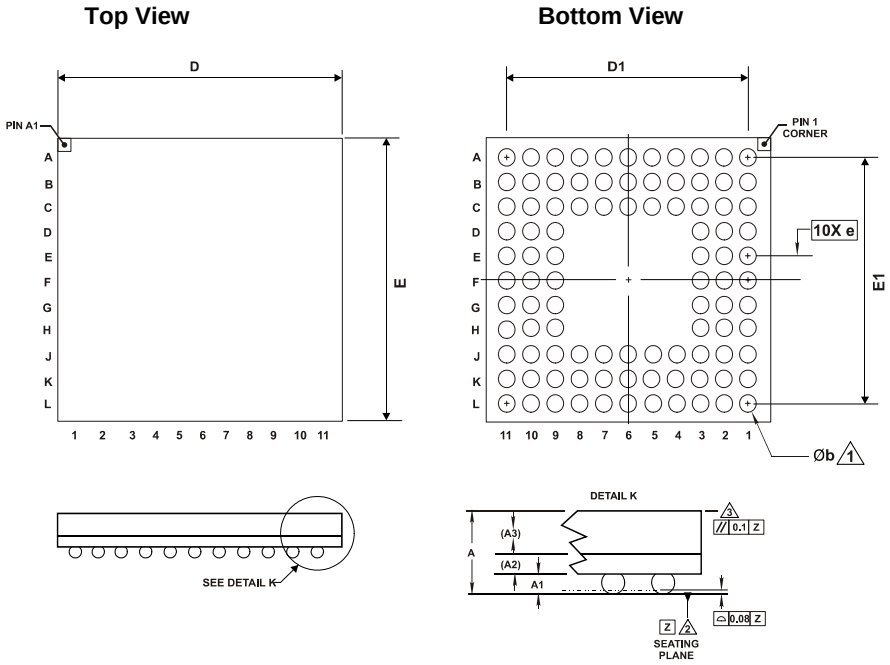


Figure 10.2: Example Application Circuit

For a full BlueCore2-External reference design, contact your local CSR representative.

11 Package Dimensions

11.1 8 x 8 and 6 x 6 VFBGA Packages

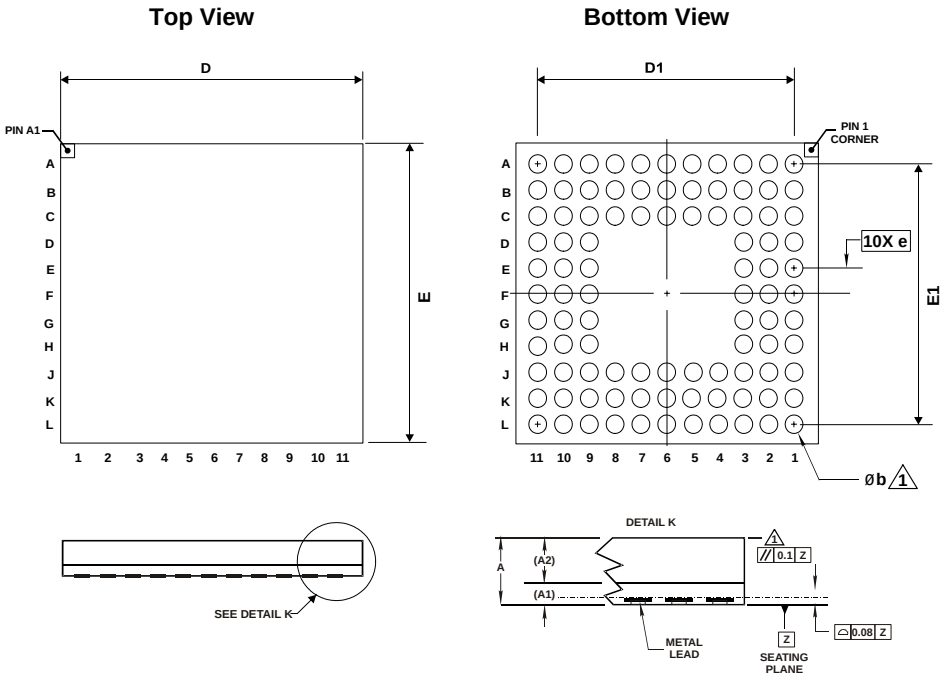


BC212015DN 8x8x1mm VFBGA			
DIM	MIN	MAX	NOTES
A	0.8	1	1 DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM PLANE Z.
A1	0.2	0.3	
A2	0.22 REF		2 DATUM Z IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
A3	0.45 REF		
b	0.25	0.35	3 PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
D	8 BSC		
E	8 BSC		
e	0.65 BSC		
D1	6.5 BSC		
E1	6.5 BSC		
VFBGA 96 BALLS 8X8X1mm (JEDEC MO-225)			UNIT: MM

BC212015EN and BC212013EN 6x6x1mm VFBGA			
DIM	MIN	MAX	NOTES
A	0.8	1	1 DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM PLANE Z.
A1	0.2	0.3	
A2	0.22 REF		2 DATUM Z IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
A3	0.45 REF		
b	0.25	0.35	3 PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
D	6 BSC		
E	6 BSC		
e	0.5 BSC		
D1	5 BSC		
E1	5 BSC		
VFBGA 96 BALLS 6X6X1mm (JEDEC MO-225)			UNIT: MM

Figure 11.1: BlueCore2-External VFBGA Package Dimensions

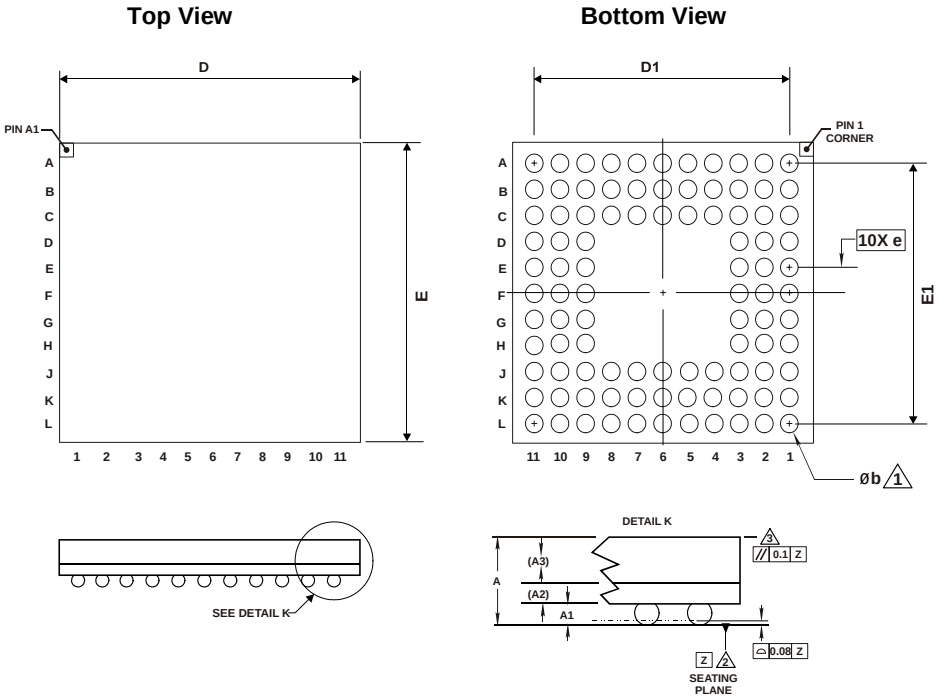
11.2 6 x 6 LGA Package



BC212015LN and BC212013LN 6x6x0.6mm LGA				
DIM	MIN	TYP	MAX	NOTES
A		0.6	0.65	1 PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
A1		0.22 REF		
A2	0.32	0.37	0.42	
b	0.15		0.25	
D		6 BSC		
E		6 BSC		
e		0.5 BSC		
D1		5 BSC		
E1		5 BSC		
LGA 96 BALLS 6X6X0.6mm (JEDEC MO-222)				UNIT: MM

Figure 11.2: BlueCore2 External LGA Package Dimensions

11.3 10 x 10 LFBGA Package



BC212015BN 10x10x1.4mm LFBGA			
DIM	MIN	MAX	NOTES
A	---	1.4	1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM PLANE Z.
A1	0.3	0.4	
A2	0.26 REF		2. DATUM Z IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
A3	0.8 REF		
b	0.35	0.45	3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
D	10 BSC		
E	10 BSC		
e	0.8 BSC		
D1	8 BSC		
E1	8 BSC		
LFBGA 96 BALLS 10X10X1.4mm (JEDEC MO-210)			UNIT: MM

Figure 11.3: BlueCore2 External LFBGA Package Dimensions

12 Solder Profiles

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder re-flow. There are four zones:

1. Preheat Zone: This zone raises the temperature at a controlled rate, typically 1-2.5°C/s.
2. Equilibrium Zone: This zone brings the board to a uniform temperature and also activates the flux. The duration in this zone (typically two to three minutes) will need to be adjusted to optimise the out gassing of the flux.
3. Reflow Zone: The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint.
4. Cooling Zone: The cooling rate should be fast, to keep the solder grains small which will give a longer lasting joint. Typical rates will be 2-5°C/s.

12.1 Solder Re-flow Profile for Devices with Tin/Lead Solder Balls

Composition of the solder ball: Sn 62%, Pb 36.0%, Ag 2.0%

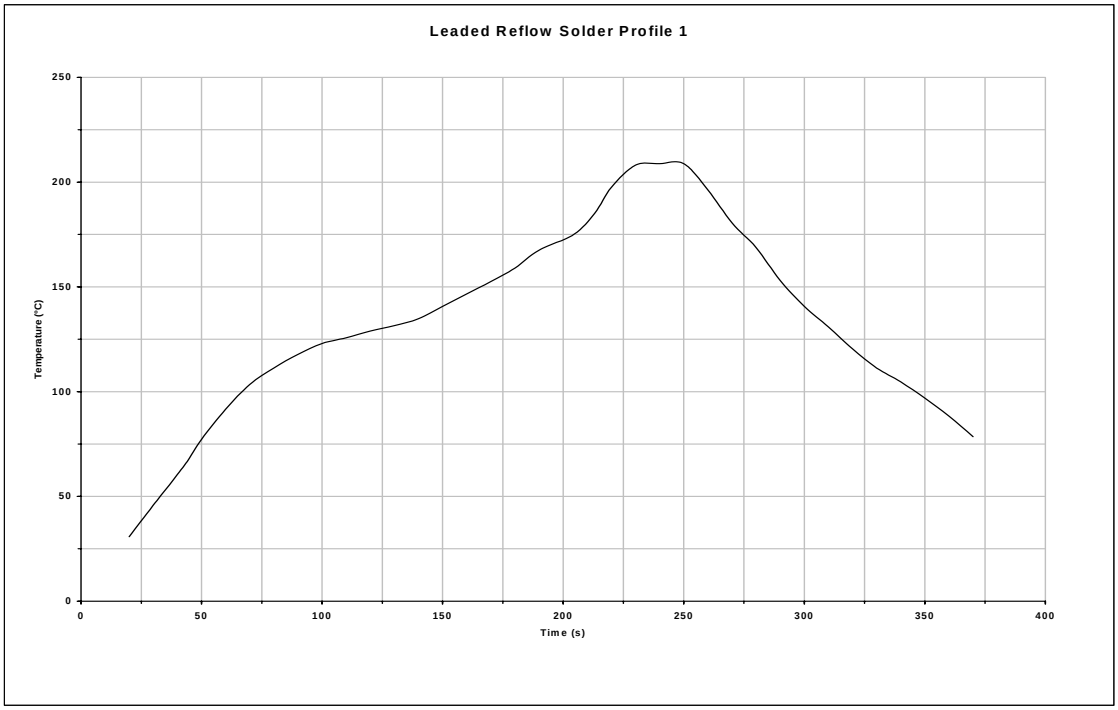


Figure 12.1: Typical Re-flow Solder Profile

Key features of the profile:

- Initial Ramp = 1-2.5°C/sec to 125°C±25°C equilibrium
- Equilibrium time = 60 to 120 seconds
- Ramp to Maximum temperature (210°C to 220°C) = 3°C/sec max.
- Time above liquidus (183°C): 45 to 90 seconds
- Device absolute maximum re-flow temperature 240°C

Devices will withstand the specified profile.

Lead-free devices will withstand up to three reflows to a maximum temperature of 240°C.

12.2 Solder Reflow Profile for Devices with Lead-Free Solder Balls

Composition of the solder ball: Sn 95.5%, Ag 4.0%, Cu 0.5%

Figure 12.2: Typical Lead-Free Re-flow Solder Profile

Key features of the profile:

- Initial Ramp = 1-2.5°C/sec to 175°C±25°C equilibrium
- Equilibrium time = 60 to 180 seconds
- Ramp to Maximum temperature (250°C) = 3°C/sec max.
- Time above liquidus temperature (217°C): 45-90 seconds
- Device absolute maximum reflow temperature: 260°C

Devices will withstand the specified profile.

Lead-free devices will withstand up to 3 reflows to a maximum temperature of 260°C.

13 Product Reliability Tests

Die	Test Conditions	Specification	Sample Size
ESD	Human Body Model	JEDEC	3
Latch-up	±120mA	JEDEC	6
Early Life	125°C	48 hours	800
Hot Life Test	125°C	1000 hours	231

Package	Test Conditions	Specification	Sample Size
Moisture Sensitivity Precon JEDEC Level 3	(125°C 24 hours) 30°C/60%RH	192 hours five re-flow simulation cycles	770
Temperature Cycling	-65°C to +150°C	500 cycles	231 from Precon
AutoClave (Steam)	121°C at 100% RH	96 hours	231 from Precon
Temperature Humidity Bias	85°C/85% RH	1000 hours	77 from Precon
Thermal Shock	-55°C to 125°C	100 cycles	231 From Precon
High Temperature Storage	150°C	1000 hours	77

14 Product Reliability Tests for BlueCore Automotive

The reliability tests in this section follow the tests outlined in the AEC-Q100 and were performed on BlueCore2-External in VFBGA 10 x 10mm 96IO (tin-lead solder balls). Samples are electrically tested at ambient temperature.

This package qualification will (where moisture sensitivity preconditioning is required) use IPC/Jedec MSL3, i.e., the finished product is allowed a maximum exposure to a ≤30°C/60%RH environment for 168 hours before mounting.

As part of CSR's automotive test program, customers will have access to the initial device reliability test report. They will also have access to a quarterly reliability test report update for automotive parts.

Die	Test Conditions	Specification	Sample Size	Result
ESD	Human Body Model	JEDEC	24	Pass
Early Life	125°C Vddmax	48 hours	2400	Pass
Hot Life Test	125°C Vddmax	1000 hours	90, 77, 77	Pass

Package	Test Conditions	Specification	Sample Size	Result
Moisture Sensitivity Precon JEDEC Level 3	(125°C 24 hours) 30°C/60%RH	192 hours five re flow simulation cycles	783	Pass
Temperature Cycling	-65/150°C	500 cycles	231 from Precon	Pass
Autoclave (Steam)	121°C/100%RH	96 hours	231 from Precon	Pass
Temperature Humidity Bias	85°C/85%RH Vddmax	1000 hours	231 from Precon	Pass
Thermal Shock	-55/125°C	100 cycles	77 from Precon	Pass
High Temperature Storage	150°C	1000 hours	77	Pass

Other	Test Conditions	Sample Size	Result
Bond Shear	Acid decapsulationof finished product	30 bonds	Pass
Wire Pull	Acid decapsulationof finished product	60 wires from Preconand temperature cycling	Pass
Solder Ball Shear	Two reflow cycles	150 balls	Pass
Visual Inspection and Dimensions	n/a	30 devices	Pass

15 Tape and Reel Information

Tape and reel is in accordance with EIA-481-2.

15.1 Tape Orientation and Dimensions

Figure 15.1 shows the general orientation of BlueCore2-External in the tape.

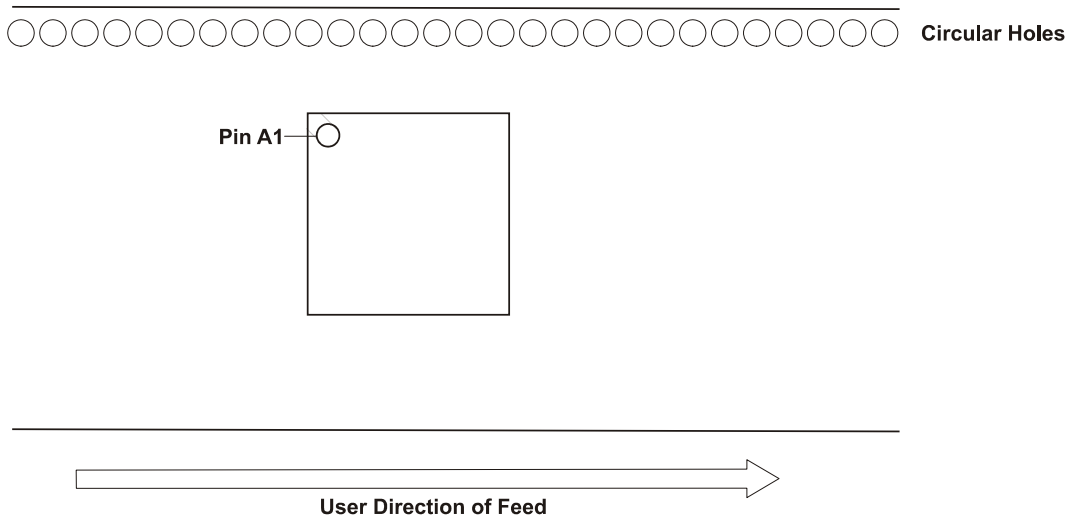
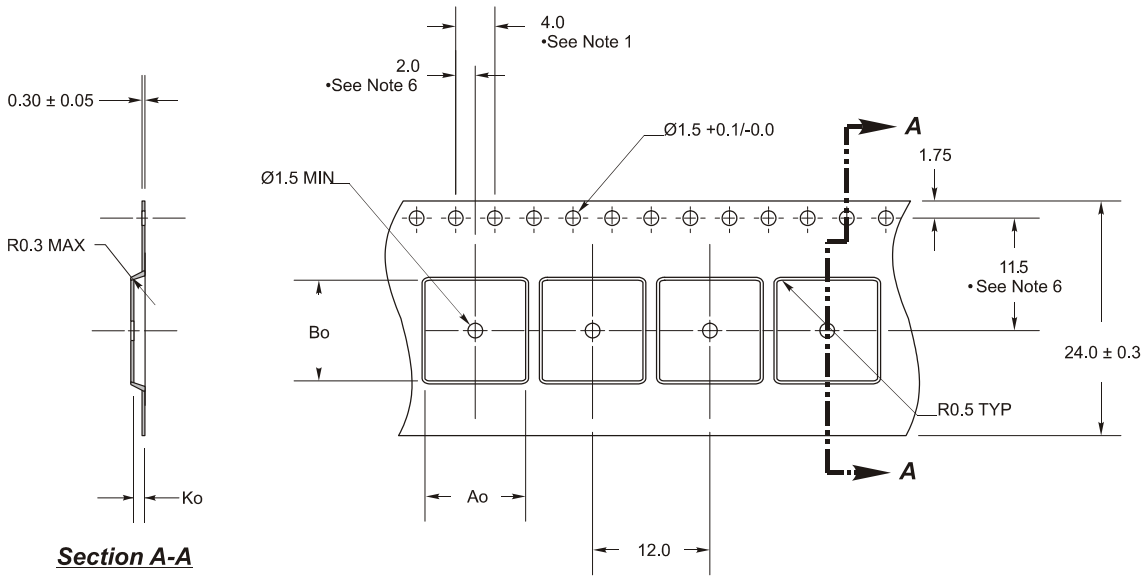


Figure 15.1: Tape and Reel Orientation

Figure 15.2 outlines the dimensions of the tape used for 10 x 10 x 1.4mm LFBGA devices.



Notes:
1. 10 sprocket hole pitch cumulative tolerance ±.02.
2. Camber not to exceed 1mm in 100mm.
3. Material: PS + C.
4. Ao and Bo measured on a plane 0.3mm above the bottom of the pocket
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Ao = 10.3 mm
Bo = 10.3 mm
Ko = 1.5 mm

Figure 15.2: Tape Dimensions

The cover tape has a total peel strength of 0.1N to 1.3N. The direction of the pull should be opposite to the direction of the carrier tape such that the cover tape makes an angle of between 165° and 180° with the top of the carrier tape. The carrier and/or cover tape should be pulled with a velocity of 300±10mm/minute during peeling.

Maximum component rotation inside the cavity is 10° in accordance with EIA-481-2. The cavity pitch tolerance (dimension P1) is ±0.1mm.

The reel is made of high impact injection molded polystyrene. The carrier tape is made of polystyrene with carbon. The cover tape is made of antistatic polyester film and an antistatic heat activated adhesive coating.

15.2 Reel Information

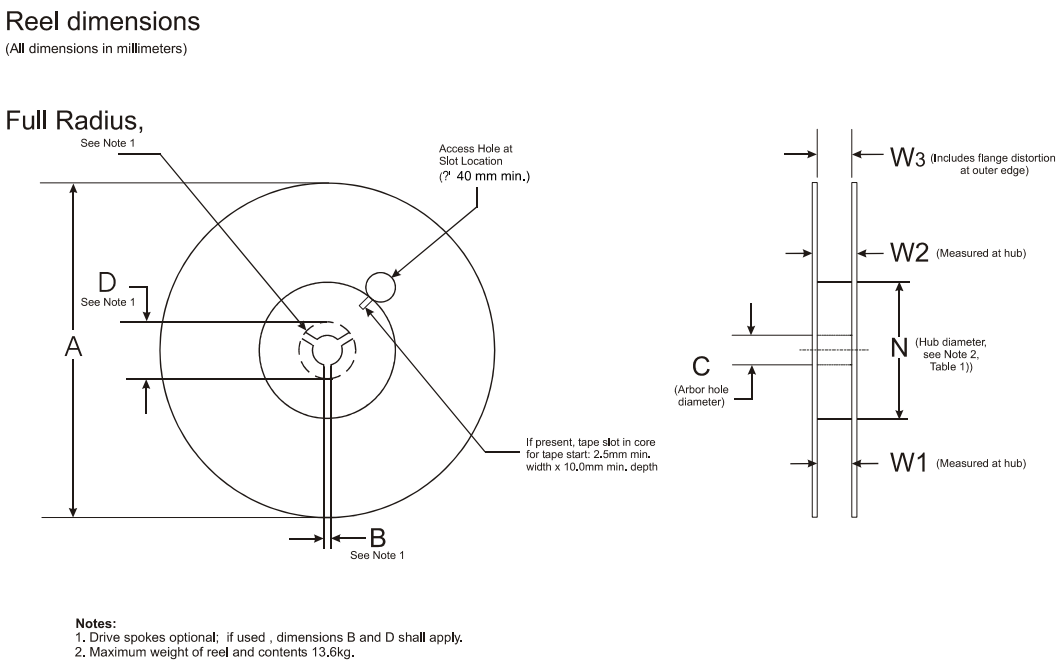


Figure 15.3: Reel Dimensions

Package Type	Tape Width	B Min	C	D Min	N Min	W1	W2 Max	W3
10 x10 LFBGA	24mm	1.5mm	13.0+0.5/ -0.2mm	20.2mm	50mm	16.4+2.0/ -0.0mm	22.4mm	15.9mm Min 19.4mm Max

Table 15.1: Reel Dimensions

15.3 Dry Pack Information

The primary packed product is dry packed in accordance with Joint IPC / JEDEC J-STD-033.

All materials used in dry packing conform to EIA-541 and EIA-583.

Figure 15.4 shows some illustrative views of reel dry packs.

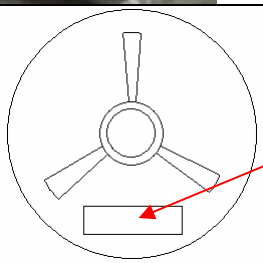
	Humidity Indicator Card 10% ~ 30% Desiccant: two units bags each containing 2 units of desiccant Cube of pink foam to protect tape from crushing
	Desiccant and Humidity Indicator Card are put on the bottom side of the reel.
	Position of label on reel.
	Caution Label is printed on dry pack bag. Dry pack bag.

Figure 15.4: Tape and Reel Packaging

Devices shipped in dry-pack bags will withstand storage in normal environmental conditions, such as 30°C and 70% RH for a minimum of one year as long as the dry-pack bag has not become punctured. Humidity indicators inside the dry-pack bag will confirm this when the bag is opened.

15.3.1 Baking Conditions

Devices may, if necessary, be re-baked at 125°C for 24 hours. If devices are still on the reel, which cannot withstand such high temperatures, they should be baked at 45°C for 192 hours at relative humidity less than 5%.

Solder wettability of parts will be unaffected by three such bakes.

15.3.2 Product Information

Figure 15.5 shows example product information labels.

Figure 15.5: Product Information Labels

A product information label is placed on each reel, primary package and shipment package.

16 Ordering Information

BlueCore2-External Standard Packaging Options

Firmware: HCI/on-chip RFCOMM

Interface Version	Package			Order Number
	Type	Size	Shipment Method	
UART and USB	96-ball LFBGA	10 x 10 x1.4mm	Tape and reel	BC212015BBN-E4
	96-ball VFBGA	8 x 8 x 1mm	Tape and reel	BC212015BDN-E4
	96-ball VFBGA	6 x 6 x 1mm	Tape and reel	BC212015BEN-E4
	96-ball VFBGA Lead Free	6 x 6 x 1mm	Tape and reel	BC212015BRN-E4
	96-ball VFBGA Lead Free	8 x 8 x 1mm	Tape and reel	BC212015BQN-E4
	96-ball LGA	6 x 6 x 0.65mm	Tape and reel	BC212015BLN-E4

Table 16.1: BlueCore2-External Standard Package Options

BlueCore2-External is available with additional software options, as Table 16.2 shows. To order one of these versions attach the appropriate order code to the main packaging order number, e.g., BC212015BDN-E4-0112.

Additional Software Options

Product Family	Description	Order Code
BlueCore2-Ext-PC	Bluetooth for Windows v1.2 English	-0112
BlueCore2-Ext-Embedded	Bluetooth Embedded v1.2	-4012
BlueCore2-Ext-BCHS(1)	BlueCore Host Software	-8010

Table 16.2: Additional Software Options

Note:

(1) Only available for UART interface versions.

Packaging Option

2kpcs Taped and Reeled

17 Contact Information

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To contact a CSR representative, go to http://www.csr.com/contacts.htm

18 Document References

Document References	Version
Specification of the Bluetooth system	v1.1, 22 February 2001 and v1.2, 05 November 2003
Universal Serial Bus Specification	v1.1, 23 September 1998

Acronyms and Definitions

Term:	Definition:
ACL	Asynchronous Connection-Less. A Bluetooth data packet
AC	Alternating Current
ADC	Analogue to Digital Converter
AGC	Automatic Gain Control
A-law	Audio encoding standard
API	Application Programming Interface
ASIC	Application Specific Integrated Circuit
BCSP	BlueCore™ Serial Protocol
BER	Bit Error Rate. Used to measure the quality of a link
BGA	Ball Grid Array
BIST	Built-In Self-Test
BlueCore™	Group term for CSR's range of Bluetooth wireless technology chips
Bluetooth®	Set of technologies providing audio and data transfer over short-range radio connections
BOM	Bill of Materials. Component part list and costing for a product
BMC	Burst Mode Controller
BSC	Basic. Represents theoretical exact dimension or dimension target
C/I	Carrier Over Interferer
CFI	Common Flash Interface
CMOS	Complementary Metal Oxide Semiconductor
CODEC	Coder Decoder
CPU	Central Processing Unit
CQDDR	Channel Quality Driven Data Rate
CSB	Chip Select
CSR	Cambridge Silicon Radio
CTS	Clear to Send
CVSD	Continuous Variable Slope Delta Modulation
DAC	Digital to Analogue Converter
dBm	Decibels relative to 1mW
DC	Direct Current
DFU	Device Firmware Upgrade
FSK	Frequency Shift Keying
GCI	General Circuit Interface. Standard synchronous 2B+D ISDN timing interface
GSM	Global System for Mobile communications
HCI	Host Controller Interface
Host	Application's microcontroller
Host Controller	Bluetooth integrated chip
HV	Header Value
IQ Modulation	In-Phase and Quadrature Modulation
IAC	Inquiry Access Code
IF	Intermediate Frequency
ISDN	Integrated Services Digital Network

ISM	Industrial, Scientific and Medical
ksamples/s	kilosamples per second
L2CAP	Logical Link Control and Adaptation Protocol (protocol layer)
LC	Link Controller
LCD	Liquid Crystal Display
LGA	Land Grid Array
LNA	Low Noise Amplifier
LSB	Least-Significant Bit
μ-law	Encoding standard
MMU	Memory Management Unit
MISO	Master In Serial Out
OHCI	Open Host Controller Interface
PA	Power Amplifier
PCB	Printed Circuit Board
PCM	Pulse Code Modulation. Refers to digital voice data
PDA	Personal Digital Assistant
Persistent Store	Storage of BlueCore's configuration values in non-volatile memory
PIO	Parallel Input Output
PLL	Phase Lock Loop
ppm	parts per million
PS Key	Persistent Store Key
RAM	Random Access Memory
REB	Not Read enable
REF	Reference. Represents dimension for reference use only.
RF	Radio Frequency
RFCOMM	Protocol layer providing serial port emulation over L2CAP
RISC	Reduced Instruction Set Computer
rms	root mean squared
ROM	Read Only Memory
RSSI	Receive Signal Strength Indication
RTS	Ready To Send
RX	Receive or Receiver
SCO	Synchronous Connection-Oriented. Voice oriented Bluetooth packet
SD	Secure Digital
SDK	Software Development Kit
SDP	Service Discovery Protocol
SIG	Special Interest Group
SMS	Short Message Service
SOC	System On Chip
SPI	Serial Peripheral Interface
SPP	Serial Port Profile
SRAM	Static Random Access Memory
SS	Supplementary Services
SSI	Signal Strength Indication
SSL	Secure Sockets Layer

SUT	System Under Test
SW	Software
SWAP	Shared Wireless Access Protocol
TA	Terminal Adaptor
TAE	Terminal Adaptor Equipment
TBD	To Be Defined
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus or Upper Side Band (depending on context)
VCO	Voltage Controlled Oscillator
VFBGA	Very Fine Ball Grid Array
VM	Virtual Machine
W-CDMA	Wideband Code Division Multiple Access
WEB	Write Enable

Record of Changes

Date	Revision	Reason for Change
5 March 2002	BC212015-ds-001a	Original publication of this document
5 May 2002	BC212015-ds-001b	Additions made to RF characteristics
18 June 2002	BC212015-ds-001c	Additions made to RF characteristics and 10 x 10 packaging information added
December 2002	BC212015-ds-001d	Additional electrical and RF data added
March 2003	BC212015-ds-001e	Changes made to 10 x 10 package order code
February 2004	BC212015-ds-001f	Amendment to specification v1.1 and v1.2 compliant statement.
February 2004	BC212015-ds-001g	Removed incorrectly added CSP references.
27 July 2004	BC212015-ds-001h	Added reference to BC212015BQN product; updated section 9.7, Serial Peripheral Interface; updated section 17, Contact Information.
24 August 2004	BC212015-ds-001Pi	Added section 14, Product Reliability Tests for BlueCore Automotive; corrected formatting errors.

BlueCore™2-External

Product Data Sheet

BC212015-ds-001Pi

August 2004