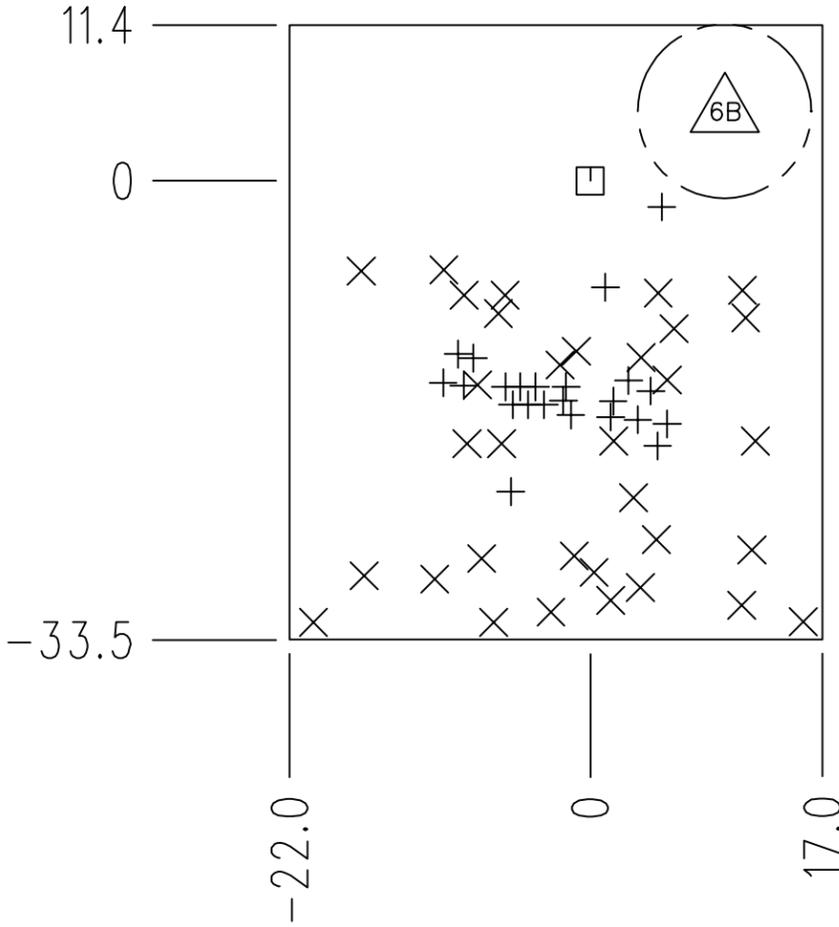


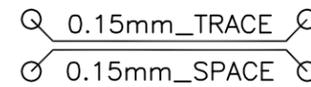
NOTES: UNLESS OTHERWISE SPECIFIED

1. MILLIMETERS (MM) ARE THE CONTROLLING DIMENSIONS FOR THE DRAWINGS AND SUPPLIED DATA. INCH DIMENSIONS ARE FOR REFERENCE ONLY.
2. FABRICATE PCB IN ACCORDANCE WITH IPC-6012, CLASS 2; PER IPC-6011 USING CUSTOMER SUPPLIED DATA FILES.
3. MATERIALS:
 - A. LAMINATE SHALL BE PER IPC-2221 PAR 4.3; IN ACCORDANCE WITH IPC-4101/25 OR /26, LAMINATED SHEET, FLAME RESISTANT (MEETING UL 94V-0). TG RATING: 170° TO 200°.
 - B. PREPREG SHALL BE PER IPC-2221 PAR 4.2; IN ACCORDANCE WITH IPC-4101/25 OR /26, PREPREG (B-STAGE), FLAME RESISTANT (MEETING UL 94V-0). TG RATING: 170° TO 200°. REFER TO CROSS-SECTION FOR COPPER FOIL WEIGHTS.
4. ALL HOLES SHALL BE LOCATED WITHIN ±0.08mm OF TRUE POSITION. LAYER-TO-LAYER REGISTRATION SHALL BE WITHIN ±0.08mm. ADD TEARDROPS AS REQUIRED SO THAT ALL HOLES SURROUNDED BY LAND HAVE A MINIMUM ANNULAR RING OF 0.08mm.
5. FINISH:
 - A. ALL EXPOSED CONDUCTIVE PATTERN AREAS NOT COVERED WITH SOLDERMASK OR OTHER PLATING SHALL BE HOT AIR SOLDER LEVELED (HASL) USING SN63A TIN LEAD SOLDER PER ANSI/J-STD-006.
 - B. APPLY LIQUID PHOTO IMAGEABLE SOLDER MASK PER IPC-SM-840, CLASS H, TO BOTH SIDES OF THE BOARD OVER BARE COPPER. VIA HOLES COVERED WITH SOLDERMASK DO NOT NEED TO BE PLUGGED. ONLY SOLDER MASK IMAGES THAT ARE THE SAME SIZE AS THE COMPONENT PADS MAY BE ENLARGED, AND SHALL NOT BE ENLARGED BEYOND 0.08 PER SIDE OR 0.15 OVERALL. ALL OTHER SOLDER MASK IMAGES SHALL NOT BE ENLARGED.
 - C. SILKSCREEN SHALL BE WHITE, PERMANENT, ORGANIC, NON-CONDUCTIVE INK. THERE SHALL BE NO SILKSCREEN ON ANY SOLDERABLE COMPONENT PAD.
6. MARKING:
 - A. BOARD PART NUMBER AND REVISION LETTER SHALL BE RENDERED IN ETCH ON THE BOTTOM SIDE OF THE BOARD. REVISION LETTER SHALL BE IDENTICAL TO THIS DRAWING.
 - B.  UL LOGO, MANUFACTURER'S IDENTIFICATION AND DATE CODE LETTER SHALL BE RENDERED IN SILK SCREEN ON THE BOTTOM SIDE OF THE BOARD APPROXIMATELY WHERE SHOWN.
7. TEST REQUIREMENTS:
 - A. 100% NETLIST ELECTRICAL VERIFICATION USING VENDOR SUPPLIED IPC-D-356 NETLIST FOR OPENS AND SHORTS. ALL NETS SHALL BE ACCESSED SIMULTANEOUSLY OR AS OTHERWISE MUTUALLY AGREED UPON.
8. TOLERANCES:
 - A. WARP OR TWIST OF BOARD SHALL NOT EXCEED 1%.
 - B. CONDUCTOR WIDTHS AND SPACING SHALL BE WITHIN +/- 0.02 OF GERBER DATA.
 - C. REMOVE ALL BURRS AND BREAK SHARP EDGES 0.4 MAXIMUM.
 - D. SURFACE MOUNT PAD PLATING MUST BE FLAT TO A MAXIMUM OF 0.08 ABOVE BOARD SURFACE.

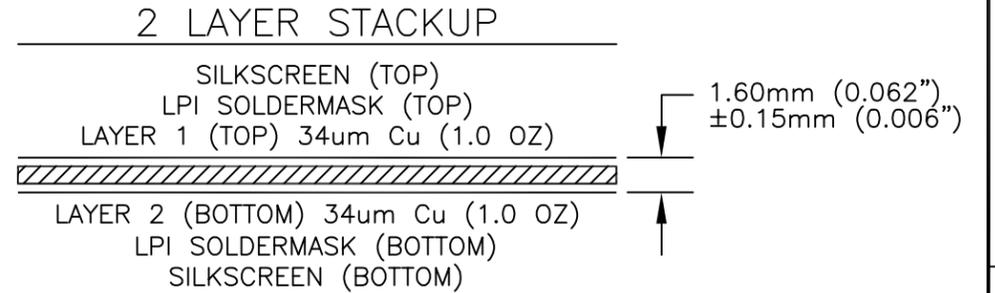
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	INITIAL RELEASE	APR-19-04	



SIZE	QTY	SYM	PLTD
0.3	23	+	PLTD
0.5	33	X	PLTD
3.2	1		NPLTD



SCALE: NONE
 DETAIL X - SMALLEST TRACE WIDTH



<small>UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE METRIC. TOLERANCES ARE: FRACTIONS DECIMALS ± .X ±0.1 .XX ±0.01</small> <small>DO NOT SCALE DRAWING</small> <small>TREATMENT</small> <small>FINISH</small> <small>SIMILAR TO MARKING SYMBOL</small>	APPROVALS		DATE	A7 ENGINEERING PCB FABRICATION EB505		
	DRAWN AMERICADPCB.COM		4/19/04			
	ENGINEER B HALL			TITLE		
	CHECKED			SIZE DWG NO. REV		
APPROVED			B 0000048 A			
ISSUED			SCALE: NONE 0000048ADD.DWG SHEET 1 OF 1			