# Xicor Real Time Clock Features & Applications

by Peter Chan, March 1999

## WHAT IS A REAL TIME CLOCK ?

A real time clock (RTC) is a device that provides the host system with a BCD representation of the time and date with crystal controlled accuracy. The host communicates with the RTC through either a parallel port or serial port. Parallel devices offer speed at the expense of board space and cost. Serial devices take more time to read and write the data, but are very small.

An RTC usually gets it's power from the main power supply, but often has a separate backup power supply that keeps the clock running even during system power failure. Operating at 32.768KHz, the real time clock consumes much less current than keeping time with the CPU (which has a clock operating in the MHz range) and greatly simplifies the programming task.

## SINGLE CHIP SOLUTION

Xicor's serial real time clock integrates a full function real time clock with 16kbits of EEPROM memory into a single small 8L TSSOP or SOIC package. EEPROM provides storage of critical configuration and user data that will not be lost even under catastophic failure of main and backup power supplies. In addition to the RTC and memory some versions of Xicor's RTC provide integrated CPU supervisory functions. The supervisory functions of power on reset, low voltage reset and watchdog timer, provide system management capabilities and make sure the voltage applied to the system is correct and the CPU is operating properly. In the event of a power or CPU failure the supervisor part of the device resets the system and prevents data corruption to the on-chip EEPROM and clock registers. This single chip solution saves board space, reduces component count, increases reliability and decreases the overall cost of the system.

## Y2K COMPLIANT

The X1203/X1243/X1240 RTCs and X1202/X1241/ X1242 RTC supervisors are controllable, readable, and programmable through an I2C serial interface and a set of registers. The RTC provides the system with seconds, minutes, hours, day, date, month and years plus a "century byte" for year 2000 compliance. The clock also has leap year correction, and automatic adjustment for months with less than 31 days.

The RTC oscillator circuit requires an external oscillator network that includes a 32.768KHz crystal. The accuracy of a real time clock is directly dependent upon the frequency of the crystal and the combination of components in the external network, see Figure 1 for recommended components. (Refer also to AN 121 for more information on selecting crystal for RTC).

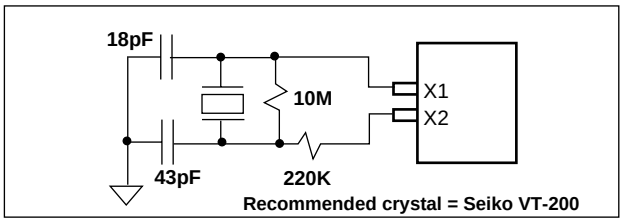


**Figure 1. Recommended Crystal Connection**

## DUAL ALARMS

An especially powerful function of the Xicor RTC is the provision for dual alarms. These alarms give the user flexibility to program separate events at a specific times of the day. The X12xx can be programmed to generate a single or dual alarm through the use of its alarm enable bits. The RTC can generate an alarm as often as once every minute (with one second accuracy) or as long as once per year. Alarms can be set for 1999 or 2000. The alarm is functional either when the device is powered by main supply or when powered by backup battery.

As an example, set alarm 0 to interrupt the system once per minute and set alarm 1 to interrupt the system every Tuesday at 8:00am. Referring to the Clock Control Register table below, Alarm 0 is set with the enable seconds alarm bit (ESC0) set to '1'. All other bits in the Alarm 0 register are set to '0'. For alarm 1, set the enable day of week bit (EDW1), the enable hours bit (EHR1), and the enable minutes bit (EMN1) to '1'. Also, load in the

value ‘2h’ to the day of week alarm register (DWA1) least significant nibble and the value ‘8h’ to the hour alarm register (HRA1) least significant nibble. All other bits of alarm register 1 should be ‘0’ The table below shows the contents of the registers for this configuration.

| Addr. | Type | Reg Name | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 (optional) | Range | Default |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| xx3F | Status | SR | BAT | AL1 | AL0 | x | x | RWEL | WEL | RTCF | | 00h |
| xx37 | RTC (SRAM) | Y2K | 0 | 0 | Y2K21 | Y2K20 | Y2K13 | 0 | 0 | Y2K10 | 19/20 | 20h |
| xx36 | | DW | 0 | 0 | 0 | 0 | 0 | DY2 | DY1 | DY0 | 0-6 | 06h |
| xx35 | | YR | Y23 | Y22 | Y21 | Y20 | Y13 | Y12 | Y11 | Y10 | 0-99 | 00h |
| xx34 | | MO | 0 | 0 | 0 | G20 | G13 | G12 | G11 | G10 | 1-12 | 01h |
| xx33 | | DT | 0 | 0 | D21 | D20 | D13 | D12 | D11 | D10 | 1-31 | 01h |
| xx32 | | HR | T24 | 0 | H21 | H20 | H13 | H12 | H11 | H10 | 0-23 | 12h |
| xx31 | | MN | 0 | M22 | M21 | M20 | M13 | M12 | M11 | M10 | 0-59 | 00h |
| xx30 | | SC | 0 | S22 | S21 | S20 | S13 | S12 | S11 | S10 | 0-59 | 00h |
| xx11 | Control (E2PROM) | INT | IM | AL1E | AL0E | FRQ0 | FRQ1 | x | x | x | | 00h |
| xx10 | | BL | BP2 | BP1 | BP0 | WD1 | WD0 | x | x | x | | 00h |
| xx0F | Alarm1 (E2PROM) | Y2K1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 19/20 | 20h |
| xx0E | | DWA1 | EDW1=0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0-6 | 80h |
| xx0D | | YRA1 | Unused - Default = RTC Year value (No EEPROM) - Future expansion | | | | | | | | | |
| xx0C | | MOA1 | EMO1=0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1-12 | 80h |
| xx0B | | DTA1 | EDT1=0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1-31 | 80h |
| xx0A | | HRA1 | EHR1=1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0-23 | 80h |
| xx09 | | MNA1 | EMN1=1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0-59 | 80h |
| xx08 | | SCA1 | ESC1=0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0-59 | 80h |
| xx07 | Alarm0 (E2PROM) | Y2K0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 19/20 | 20h |
| xx06 | | DWA0 | EDW1=0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0-6 | 80h |
| xx05 | | YRA0 | Unused - Default = RTC Year value (No EEPROM) - Future expansion | | | | | | | | | |
| xx04 | | MOA0 | EMO1=0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1-12 | 80h |
| xx03 | | DTA0 | EDT1=0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1-31 | 80h |
| xx02 | | HRA0 | EHR1=0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0-23 | 80h |
| xx01 | | MNA0 | EMN1=0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0-59 | 80h |
| xx00 | | SCA0 | ESC1=1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0-59 | 80h |

In it’s normal configuration the X1203 generates an external interrupt that goes active to notify the host CPU of an event. This interrupt remains active until the host reads the alarm status. The X12x2 devices do not have an interrupt output, but the CPU can “poll” the alarm bits to determine that an alarm has occurred. This is much simpler that implementing an alarm compare routine in software.

When an alarm occurres, the RTC sets an alarm flag. The X12x3 activates an interrupt (IRQ) pin with an active low output. The host CPU responds to this IRQ output by reading the alarm status register. This read operation resets the alarm flag and turns off the interrupt output. An alternative alarm function provides a pulsed interrupt for a preset timebase. The pulsed interrupt mode outputs a 31.25ms wide pulse when alarm 0 matches the RTC register. This operation does not require a reset from the microcontroller. This pulse will recur at intervals programmed into the alarm 0 register. Pulse rates can range from once per minute to once per year. This can serve as a very long watchdog timer function or provide syncronization of systems at periodic intervals. An example of the pulsed interrupt is shown in figure 2.

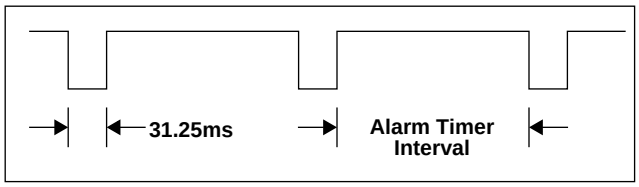


**Figure 2. Pulsed interrupt waveform**

## BATTERY-BACKUP SWITCHOVER CIRCUIT

The X12xx contains internal circuitry to automatically switch over to use a backup battery when the main Vcc supply fails and switch back to use Vcc when the main supply returns. When Vcc is lower than Vback by 0.2V, the comparator issues a low signal output which turns on transistor 2, and turns off transistor 1 as shown in Figure 3. This will switch to the backup battery mode. When Vcc goes above Vback, the comparator issues a high signal output which turns on transistor 1, and turns off transistor 2 as shown in Figure 3. This will switch back to the main battery mode. Graphically, this is shown in Figure 4 .

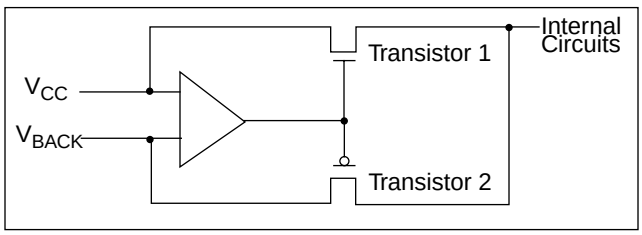


**Figure 3. Battery-backup switchover circuit**

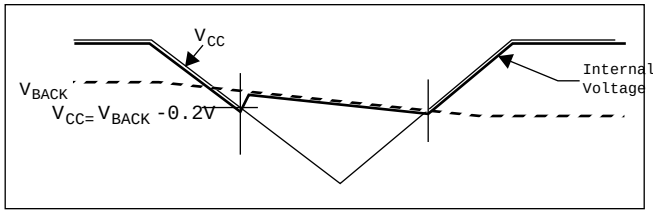


**Figure 4. Battery Backup Switch Operation**

## NONVOLATILE EEPROM

The X124x integrates 2K bytes of non-volatile EEPROM memory, operating independently from the RTC. Using EEPROM attached to the RTC (rather than battery backed RAM) protects critical system data during main and battery power failures. This makes it safer than storing data to RAM. The X124x EEPROM looks like a standard 400kHz I2C EEPROM operating at a data transfer rate of 400KHz. During a read or write operation, the RTC will not be affected. This EEPROM array can store configuration and collected data. On the X124x, Xicor has enhanced the Block Lock operation. These devices now provide the end-user the ability to Block Lock none of the array, 1/4, 1/2, or the entire array or to protect the first page, first 2 pages, first 4 pages or first 8 pages of the array. By setting three bits in the Status Register, the user can prevent a write operation from changing data in the Block Locked region. This is especially important when there are configuration parameters, critical data or manufacturing information on the same device as other data that is being changed more often or is of less significance.

In order to reduce the likelihood of inadvertent changes to the Clock Control Registers, prior to any register write operation, the following steps are required:

— Perform a Write Enable Operation to set the "Write Enable Latch" (WEL) in the status register.

— Perform a Write Enable Operation to set both the "Register Write Enable Latch" (RWEL) and the "Write Enable Latch" (WEL) in the status register.

— Write one to eight bytes of data to the Clock Control Registers or to the memory array with the desired values.

**Table 5. Status Register (SR)**

| Addr | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 3Fh | BAT | AL1 | AL0 | 0 | 0 | RWEL | WEL | RTCF |

### LOW POWER

The features of the X12xx are certainly a great benefit to many system designers, but equally important in portable systems is low power to insure long battery life. The RTC can operate as low as 1.8V. It is probable that the majority of the time the X12xx will sit idle in a powered up system. In this type of standby operation, the X12xx will consume a maximum of 12µA. During a nonvolatile write operation (maximum 10ms) the X12xx will typically consume 3mA maximum.

### APPLICATIONS

#### Data logging

Generating an alarm is especially useful because the interrupt (IRQ) enable signal can be used to "wake up" a sleeping system. For example, a portable datalogger that needs to collect data once every hour. This system is in a low power "sleep mode" when idle. The alarm from the RTC "wakes up" the system at the appropriate time to collect data. After the completing the data collection, software places the system back into sleep mode where it remains until the next alarm interrupt.

#### Time and Attendance

In a portable system such as a data collection terminal or smart card reader which tracks certain tasks taking place, the X124x can keep a record of the time of the event. After a tasks is complete, most portable systems return to a standby mode to conserve power. The dual alarm of the X12xx can be set to wake up the system at certain time interval to perform other tasks. For example, in an access control application, the system records the day and time when a person tries to access the building through certain doors, then periodically reports this information for accounting or security purposes.

#### Time Stamping

In today's telecommunication system such as a LAN, FAX, and router, timekeeping and security is an important issue. For example, FAX machines use a real time clock to stamp the time when a document was sent and received. This timekeeping provides the user the ability to proof the delivery of the documents. In conjunction with the RTC, the EEPROM can contain critical system data (such as number of copies, last service date, manufacturing information) and user information (such as telephone or node numbers). After a system power fails, all configuration data is auto recalled from the EEPROM memory to provide “seemless” operation.

#### Synchronous Systems & Service reminders

The RTC can provide a complex system a mechanism for maintaining system synchronicity through the use of long time period interrupts. These interrupts, when occuring at known time intervals, can “wake up” remote or isolated system components to keep all elements of a system operating together.

Xicor's X12x2 RTC provides low power sense circuitry to monitor sudden power failures in order to prevent the system processor lockup and loss of system communication or synchronization. This results in a more reliable system.

The RTC can also notify the user of the expiration of service or warranty periods. This could be applicable in all kinds of equipment and for many types of events such as oil change or engine tune-up in automobile, calibration of test equipment, the need for replacement sensors in inductrial equipment and similar applications.

### SUMMARY

Overall, the X12xx real time clock with EEPROM plus CPU supervisor functions provides many of the functions necessary in a variety of desktop and portable products. The integration of these features onto a single piece of silicon replaces several separate integrated circuits improving system reliability, board usage and overall system cost. This combination of features provides benefit in many common applications and will set the standard for future serial real time clocks.