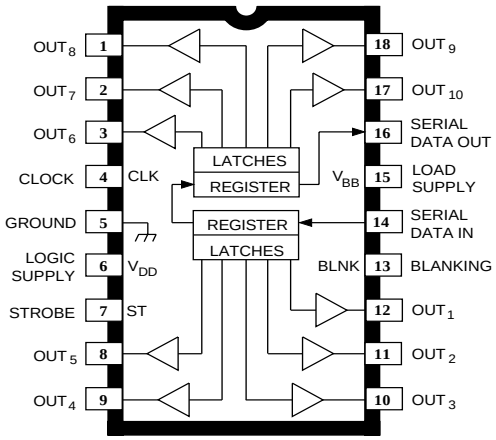
5810-F

BiMOS II 10-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE-DMOS PULL-DOWNS

UCN5810AF



Dwg. PP-029

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Logic Supply Voltage, V_{DD} ..... **15 V**
Driver Supply Voltage, V_{BB} ..... **60 V**
Continuous Output Current Range,
I_{OUT} ..... **-40 mA to +15 mA**
Input Voltage Range,
V_{IN} ..... **-0.3 V to V_{DD} + 0.3 V**
Package Power Dissipation, P_D
(UCN5810AF) ..... **2.27 W***
(UCN5810EPF) ..... **1.78 W***
(UCN5810LWF) ..... **1.56 W***
Operating Temperature Range,
T_A ..... **-20°C to +85°C**
Storage Temperature Range,
T_S ..... **-55°C to +150°C**

*Derate linearly to 0 W at +150°C.

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Note that the UCN5810AF (dual in-line package) and UCN5810LWF (small-outline IC package) are electrically identical and share a common pin number assignment.

The UCN5810AF, UCN5810EPF, and UCN5810LWF combine a 10-bit CMOS shift register and accompanying data latches, control circuitry, bipolar sourcing outputs with DMOS active pull-downs. Designed primarily to drive vacuum-fluorescent displays, the 60 V and -40 mA output ratings also allow these devices to be used in many other peripheral power driver applications. The UCN5810AF/EPF/LWF feature reduced supply requirements (active DMOS pull-downs) and lower saturation voltages when compared with the original UCN5810A.

The CMOS shift register and latches allow direct interfacing with microprocessor-based systems. With a 5 V logic supply, serial-data input rates are typically over 5 MHz, with significantly higher speeds obtainable at 12 V. Use with TTL may require appropriate pull-up resistors to ensure an input logic high.

A CMOS serial data output enables cascade connections in applications requiring additional drive lines. Similar devices are available as the UCN5811A (12 bits), UCN5812AF/EPF (20 bits), and UCN5818AF/EPF (32 bits).

The UCN5810AF/EPF/LWF output source drivers are NPN Darlingtons capable of sourcing up to 40 mA. The DMOS active pull-downs are capable of sinking up to 15 mA. For inter-digit blanking, all of the output drivers can be disabled and the DMOS sink drivers turned on by the BLANKING input high.

The UCN5810AF is furnished in an 18-pin dual in-line plastic package. The UCN5810EPF is furnished in a 20-lead plastic chip carrier. The UCN5810LWF is furnished in a wide-body, small-outline plastic package (SOIC) with gull-wing leads and 0.300" lead row spacing. Copper lead frames, reduced supply current requirements, and lower output saturation voltages allow all devices to source 25 mA from all outputs continuously, over the entire operating temperature range. All devices are also available for operation between -40°C and +85°C. To order, change the prefix from 'UCN' to 'UCQ'.

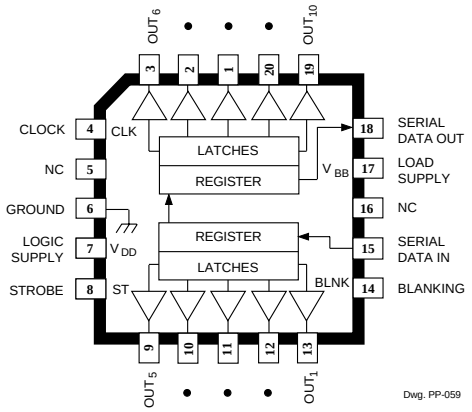
FEATURES

- High-Speed Source Drivers
- 60 V Minimum Output Breakdown
- Improved Replacements for TL4810B
- Low Output Saturation Voltages
- Low-Power CMOS Logic and Latches
- To 3.3 MHz Data Input Rate
- Active DMOS Pull-Downs

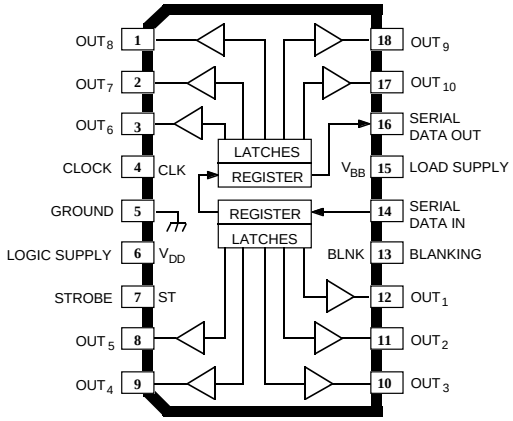
Always order by complete part number, e.g., **UCN5810AF** .

5810-F
10-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE-DMOS PULL-DOWNS

UCN5810EPF

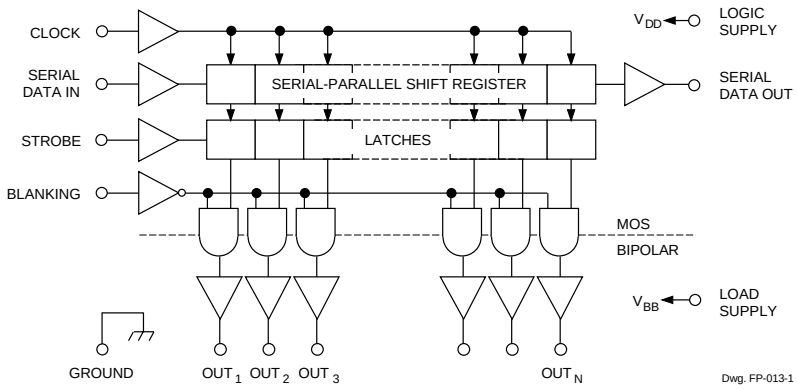


UCN5810LWF



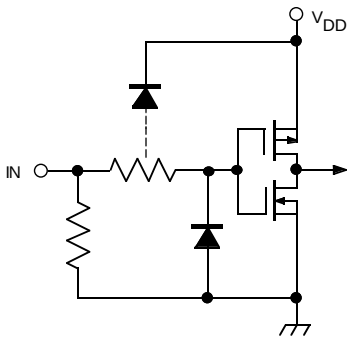
Dwg. PP-029-1

FUNCTIONAL BLOCK DIAGRAM

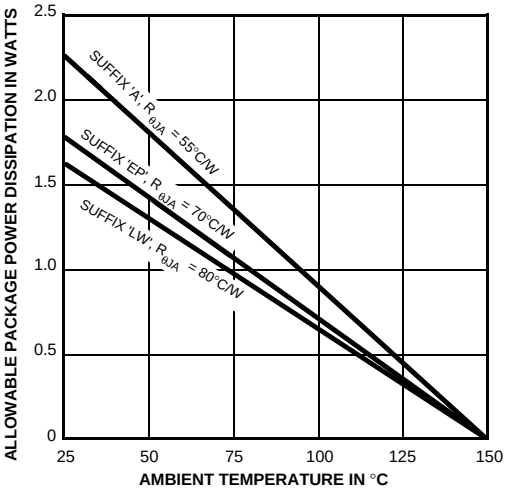


Dwg. FP-013-1

TYPICAL INPUT CIRCUIT

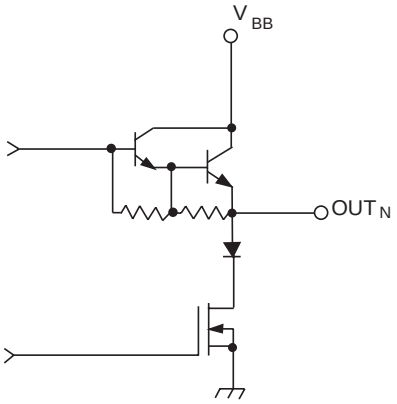


Dwg. EP-010-4A



Dwg. GP-024A

TYPICAL OUTPUT DRIVER



Dwg. No. A-14,219

Allegro MicroSystems, Inc.

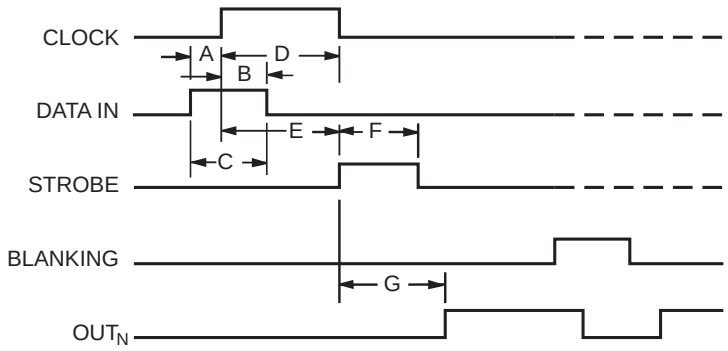
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 60 V unless otherwise noted.

Characteristic	Symbol	Test Conditions	Limits @ V_{DD} = 5 V			Limits @ V_{DD} = 12 V			Units
			Mln.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{OUT} = 0 V, T_A = +70°C	—	-5.0	-15	—	-5.0	-15	µA
Output Voltage	$V_{OUT(1)}$	I_{OUT} = -25 mA	58	58.5	—	58	58.5	—	V
	$V_{OUT(0)}$	I_{OUT} = 1 mA	—	1.0	1.5	—	—	—	V
		I_{OUT} = 2 mA	—	—	—	—	1.0	1.5	V
Output Pull-Down Current	$I_{OUT(0)}$	V_{OUT} = 5 V to V_{BB}	2.0	3.5	—	—	—	—	mA
		V_{OUT} = 20 V to V_{BB}	—	—	—	8.0	13	—	mA
Input Voltage	$V_{IN(1)}$		3.5	—	5.3	10.5	—	12.3	V
	$V_{IN(0)}$		-0.3	—	+0.8	-0.3	—	+0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = V_{DD}	—	—	100	—	—	240	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	-0.05	-0.5	—	-0.1	-1.0	µA
Serial Data Output Voltage	$V_{OUT(1)}$	I_{OUT} = -200 µA	4.5	4.7	—	11.7	11.8	—	V
	$V_{OUT(0)}$	I_{OUT} = 200 µA	—	200	250	—	100	200	mV
Maximum Clock Frequency	f_{clk}		3.3	5.0	—	—	7.5	—	MHz
Supply Current	$I_{DD(1)}$	All Outputs High	—	100	300	—	200	500	µA
	$I_{DD(0)}$	All Outputs Low	—	100	300	—	200	500	µA
	$I_{BB(1)}$	Outputs High, No Load	—	0.7	2.0	—	0.7	2.0	mA
	$I_{BB(0)}$	Outputs Low	—	10	100	—	10	100	µA
Blanking to Output Delay	t_{PHL}	C_L = 30 pF, 50% to 50%	—	2000	—	—	1000	—	ns
	t_{PLH}	C_L = 30 pF, 50% to 50%	—	1000	—	—	850	—	ns
Output Fall Time	t_f	C_L = 30 pF, 90% to 10%	—	1450	—	—	650	—	ns
Output Rise Time	t_r	C_L = 30 pF, 10% to 90%	—	650	—	—	700	—	ns

Negative current is defined as coming out of (sourcing) the specified device terminal.

5810-F
10-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE-DMOS PULL-DOWNS



Dwg. No. A-12,649A

TIMING CONDITIONS

(T_A = +25°C, V_{DD} = 5.0 V, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) ..... **75 ns**

B. Minimum Data Active Time After Clock Pulse (Data Hold Time) ..... **75 ns**

C. Minimum Data Pulse Width ..... **150 ns**

D. Minimum Clock Pulse Width ..... **150 ns**

E. Minimum Time Between Clock Activation and Strobe ..... **300 ns**

F. Minimum Strobe Pulse Width ..... **100 ns**

G. Typical Time Between Strobe Activation and Output Transition ..... **500 ns**

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, the output source drivers are disabled (OFF); the DMOS sink drivers are ON. The information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Blanking	Output Contents
H	↑	H R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
L	↑	L R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
X	↓	R_1 R_2 R_3 ... R_{N-1} R_N	R_N				
		X X X ... X X	X	L	R_1 R_2 R_3 ... R_{N-1} R_N		
		P_1 P_2 P_3 ... P_{N-1} P_N	P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N	L	P_1 P_2 P_3 ... P_{N-1} P_N
					X X X ... X X	H	L L L ... L L

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

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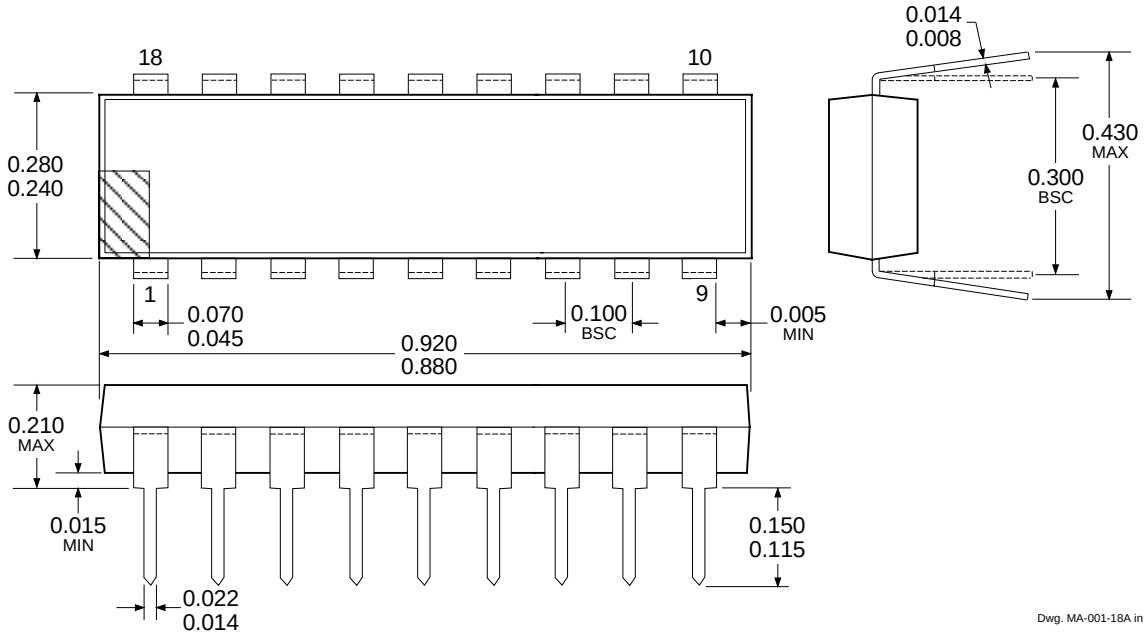
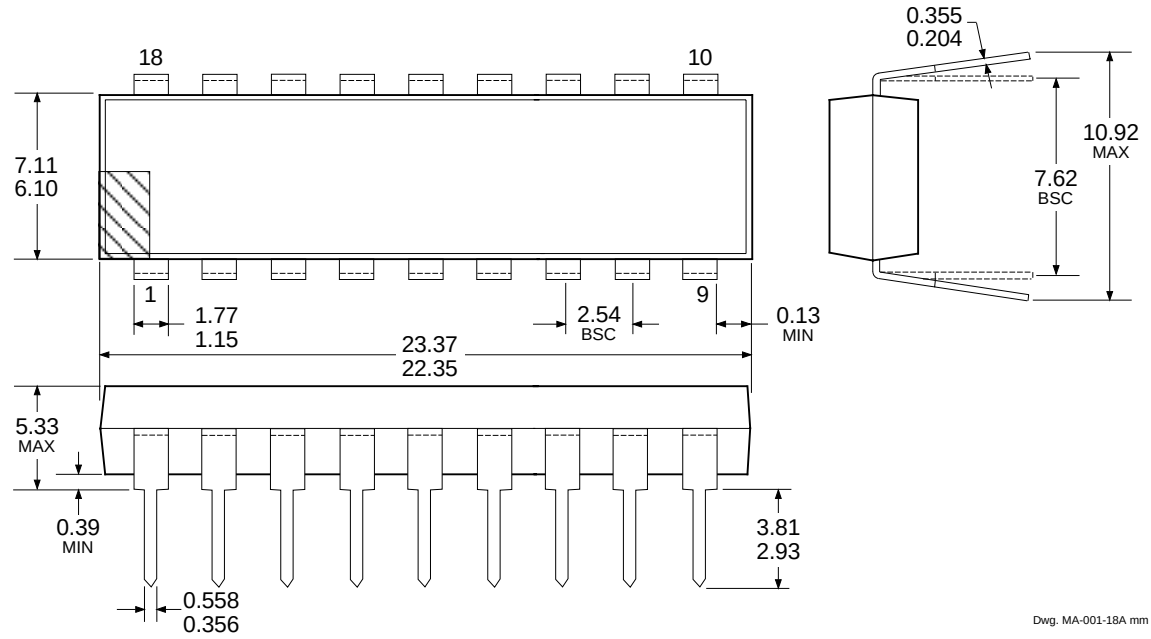
UCN5810AF

Dimensions in Inches



Dwg. MA-001-18A in

Dimensions in Millimeters (Based on 1" = 25.4 mm)

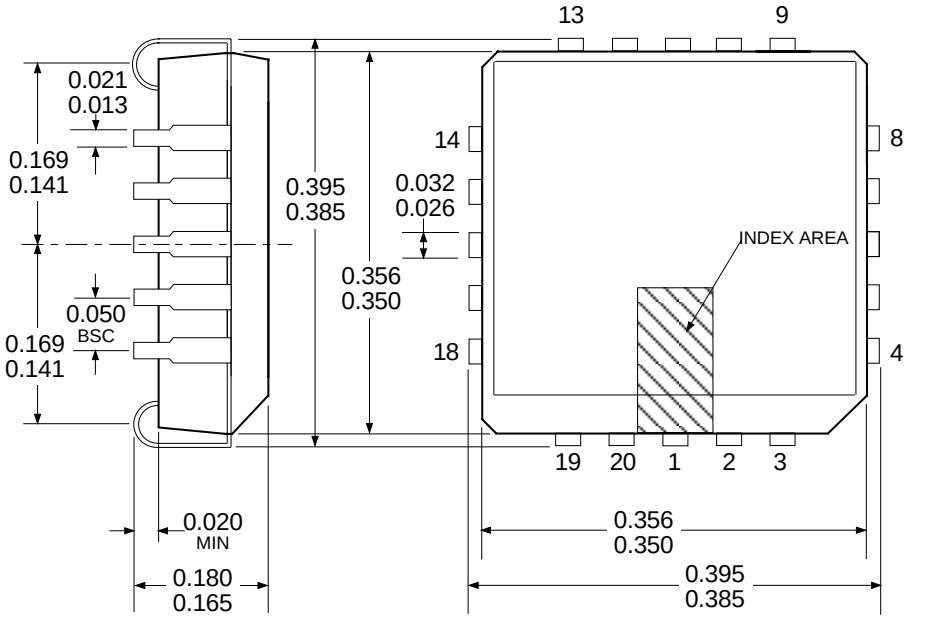


Dwg. MA-001-18A mm

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.
3. Lead thickness is measured at seating plane or below.

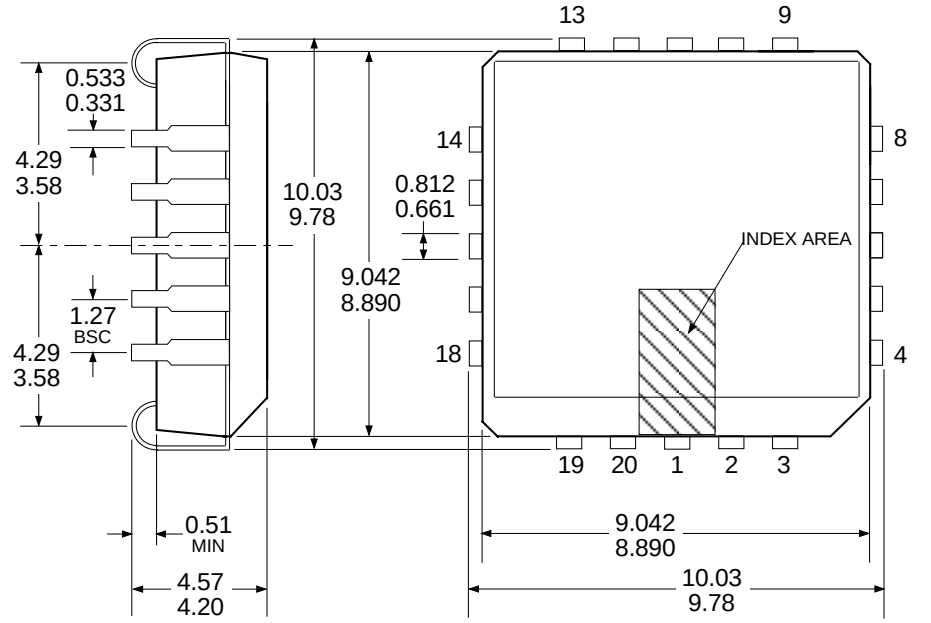
UCN5810EPF

Dimensions in Inches



Dwg. MA-005-20A in

Dimensions in Millimeters (Based on 1" = 2.54 mm)



Dwg. MA-005-20A mm

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.

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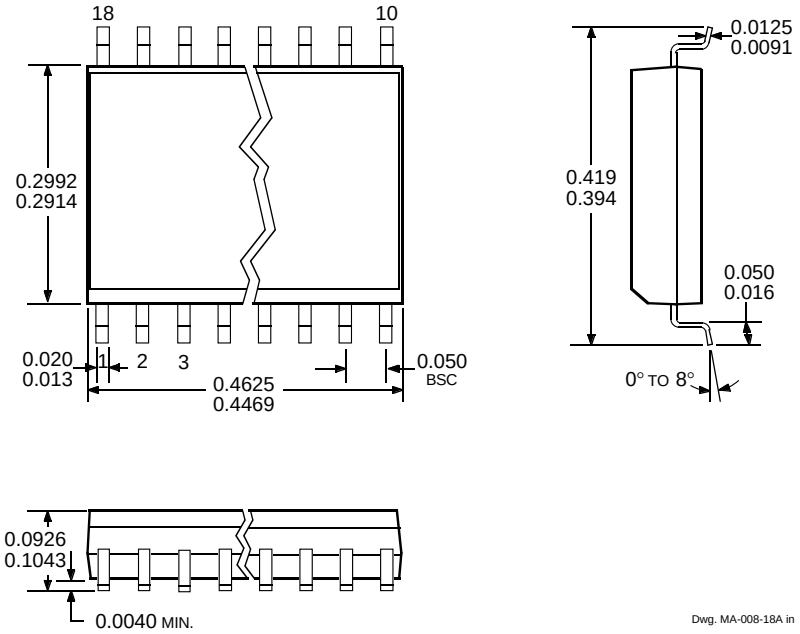
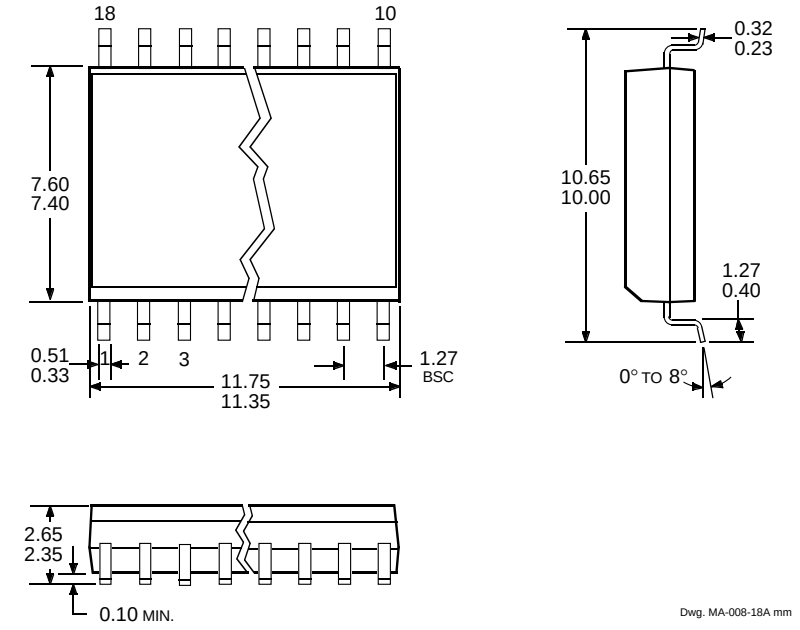
UCN5810LWF

Dimensions in Inches (Based on 1 mm = 0.03937")



Dwg. MA-008-18A in

Dimensions in Millimeters



Dwg. MA-008-18A mm

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.

5810-F
10-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE-DMOS PULL-DOWNS

BiMOS II (Series 5800) & DABiC IV (Series 6800) INTELLIGENT POWER INTERFACE DRIVERS SELECTION GUIDE

Function	Output Ratings *		Part Number †
SERIAL-INPUT LATCHED DRIVERS			
8-Bit (saturated drivers)	-120 mA	50 V‡	5895
8-Bit	350 mA	50 V	5821
8-Bit	350 mA	50 V‡	5841
8-Bit	350 mA	80 V‡	5842
9-Bit	1.6 A	50 V	5829
10-Bit (active pull-downs)	-25 mA	60 V	5810-F
12-Bit (active pull-downs)	-25 mA	60 V	5811
20-Bit (active pull-downs)	-25 mA	60 V	5812-F
32-Bit (active pull-downs)	-25 mA	60 V	5818-F
32-Bit	100 mA	30 V	5833
32-Bit (saturated drivers)	100 mA	40 V	5832
PARALLEL-INPUT LATCHED DRIVERS			
4-Bit	350 mA	50 V‡	5800
8-Bit	-25 mA	60 V	5815
8-Bit	350 mA	50 V‡	5801
SPECIAL-PURPOSE FUNCTIONS			
Unipolar Stepper Motor Translator/Driver	1.25 A	50 V‡	5804
Addressable 28-Line Decoder/Driver	450 mA	30 V	6817

* Current is maximum specified test condition, voltage is maximum rating. See specification for sustaining voltage limits. Negative current is defined as coming out of (sourcing) the output.

† Complete part number includes additional characters to indicate operating temperature range and package style.

‡ Internal transient-suppression diodes included for inductive-load protection.

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