DATA SHEET

TDA8351
DC-coupled vertical deflection circuit

Preliminary specification
Supersedes data of June 1992
File under Integrated Circuits, IC02

January 1995

Philips Semiconductors

PHILIPS

DC-coupled vertical deflection circuit — TDA8351

FEATURES

- Few external components
- Highly efficient fully DC-coupled vertical output bridge circuit
- Vertical flyback switch
- Guard circuit
- Protection against:
  - short-circuit of the output pins (7 and 4)
  - short-circuit of the output pins to V_P
- Temperature (thermal) protection
- High EMC immunity because of common mode inputs
- A guard signal in zoom mode.

GENERAL DESCRIPTION

The TDA8351 is a power circuit for use in 90° and 110° colour deflection systems for field frequencies of 50 to 120 Hz. The circuit provides a DC driven vertical deflection output circuit, operating as a highly efficient class G system.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC supply						
V_P	supply voltage		9	–	25	V
I_q	quiescent supply current		–	30	–	mA
Vertical circuit						
$I_{O(p-p)}$	output current (peak-to-peak value)		–	–	3	A
$I_{diff(p-p)}$	differential input current (peak-to-peak value)		–	600	–	μA
$V_{diff(p-p)}$	differential input voltage (peak-to-peak value)		–	1.5	1.8	V
Flyback switch						
I_M	peak output current		–	–	±1.5	A
V_{FB}	flyback supply voltage		–	–	50	V
		note 1	–	–	60	V
Thermal data (in accordance with IEC 747-1)						
T_{stg}	storage temperature		–55	–	+150	°C
T_{amb}	operating ambient temperature		–25	–	+75	°C
T_{vj}	virtual junction temperature		–	–	150	°C

Note

1. A flyback supply voltage of >50 V up to 60 V is allowed in application. A 220 nF capacitor in series with a 22 Ω resistor (dependent on I_O and the inductance of the coil) has to be connected between pin 7 and ground. The decoupling capacitor of V_{FB} has to be connected between pin 6 and pin 3. This supply voltage line must have a resistance of 33 Ω (see application circuit Fig.6).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8351	SIL9P	plastic single-in-line power package; 9 leads	SOT131-2

BLOCK DIAGRAM

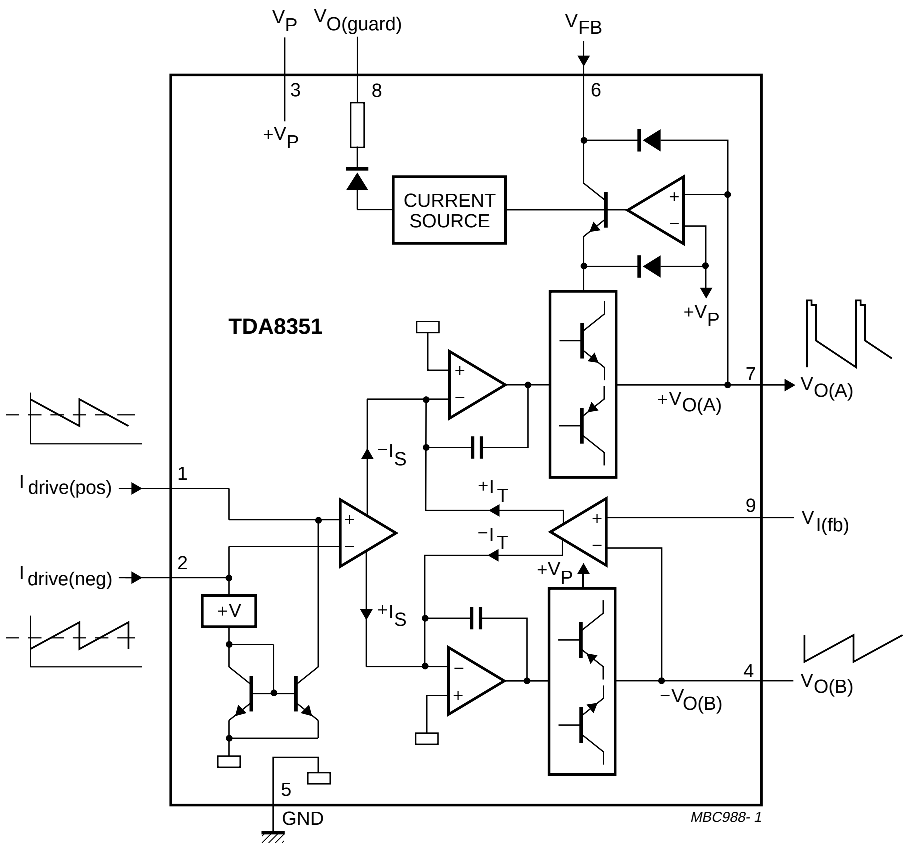
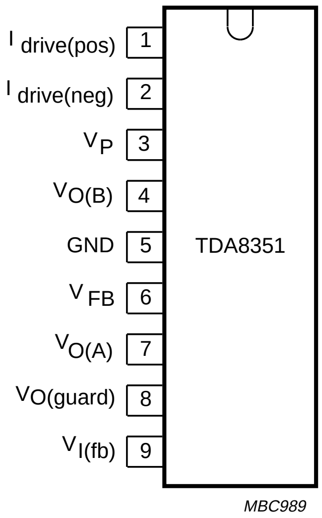


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$I_{drive(pos)}$	1	input power-stage (positive); includes $I_{I(sb)}$ signal bias
$I_{drive(neg)}$	2	input power-stage (negative); includes $I_{I(sb)}$ signal bias
V_P	3	operating supply voltage
$V_{O(B)}$	4	output voltage B
GND	5	ground
V_{FB}	6	input flyback supply voltage
$V_{O(A)}$	7	output voltage A
$V_{O(guard)}$	8	guard output voltage
$V_{I(fb)}$	9	input feedback voltage



Metal block connected to substrate pin 5.
Metal on back.

Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The vertical driver circuit is a bridge configuration. The deflection coil is connected between the output amplifiers, which are driven in phase opposition. An external resistor (R_M) connected in series with the deflection coil provides internal feedback information. The differential input circuit is voltage driven. The input circuit has been adapted to enable it to be used with the TDA9150, TDA9151B, TDA9160A, TDA9162, TDA8366 and TDA8376 which deliver symmetrical current signals. An external resistor (R_{CON}) connected between the differential input determines the output current through the deflection coil. The relationship between the differential input current and the output current is defined by: $I_{diff} \times R_{CON} = I_{coil} \times R_M$. The output current is adjustable from 0.5 A (p-p) to 3 A (p-p) by varying R_M. The maximum input differential voltage is 1.8 V. In the application it is recommended that V_{diff} = 1.5 V (typ). This is recommended because of the spread of input current and the spread in the value of R_{CON}.

The flyback voltage is determined by an additional supply voltage V_{FB}. The principle of operating with two supply voltages (class G) makes it possible to fix the supply voltage V_P optimum for the scan voltage and the second supply voltage V_{FB} optimum for the flyback voltage. Using this method, very high efficiency is achieved.

The supply voltage V_{FB} is almost totally available as flyback voltage across the coil, this being possible due to the absence of a decoupling capacitor (not necessary, due to the bridge configuration). The output circuit is fully protected against the following:

- thermal protection
- short-circuit protection of the output pins (pins 4 and 7)
- short-circuit of the output pins to V_P.

A guard circuit $V_{O(guard)}$ is provided. The guard circuit is activated at the following conditions:

- during flyback
- during short-circuit of the coil and during short-circuit of the output pins (pins 4 and 7) to V_P or ground
- during open loop
- when the thermal protection is activated.

This signal can be used for blanking the picture tube screen.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
DC supply					
V_P	supply voltage	non-operating	–	40	V
			–	25	V
V_{FB}	flyback supply voltage		–	50	V
		note 1	–	60	V
Vertical circuit					
$I_{O(p-p)}$	output current (peak-to-peak value)	note 2	–	3	A
$V_{O(A)}$	output voltage (pin 7)		–	52	V
		note 1	–	62	V
Flyback switch					
I_M	peak output current		–	±1.5	A
Thermal data (in accordance with IEC 747-1)					
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–25	+75	°C
T_{vj}	virtual junction temperature		–	150	°C
$R_{th\ vj-c}$	resistance v_j-case		–	4	K/W
$R_{th\ vj-a}$	resistance v_j-ambient in free air		–	40	K/W
t_{sc}	short-circuiting time	note 3	–	1	hr

Notes

1. A flyback supply voltage of >50 V up to 60 V is allowed in application. A 220 nF capacitor in series with a 22 Ω resistor (dependent on I_O and the inductance of the coil) has to be connected between pin 7 and ground. The decoupling capacitor of V_{FB} has to be connected between pin 6 and pin 3. This supply voltage line must have a resistance of 33 Ω (see application circuit Fig.6).
2. I_O maximum determined by current protection.
3. Up to V_P = 18 V.

CHARACTERISTICS

V_P = 17.5 V; T_{amb} = 25 °C; V_{FB} = 45 V; f_i = 50 Hz; $I_{I(sb)}$ = 400 μA; measured in test circuit of Fig.3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC supply						
V_P	operating supply voltage		9.0	–	25	V
V_{FB}	flyback supply voltage		V_P	–	50	V
		note 1	V_P	–	60	V
I_P	supply current	no signal; no load	–	30	55	mA
Vertical circuit						
V_O	output voltage swing (scan)	I_{diff} = 0.6 mA (p-p); V_{diff} = 1.8 V (p-p); I_O = 3 A (p-p)	19.8	–	–	V
LE	linearity error	I_O = 3 A (p-p); note 2	–	1	2	%
		I_O = 50 mA (p-p); note 2	–	1	2	%
V_O	output voltage swing (flyback) $V_{O(A)}$ - $V_{O(B)}$	I_{diff} = 0.3 mA; I_O = 1.5 A (M)	–	39	–	V
V_{DF}	forward voltage of the internal efficiency diode ($V_{O(A)}$ - V_{FB})	I_O = –1.5 A (M); I_{diff} = 0.3 mA	–	–	1.5	V
$\|I_{os}\|$	output offset current	I_{diff} = 0; $I_{I(sb)}$ = 50 to 500 μA	–	–	30	mA
$\|V_{os}\|$	offset voltage at the input of the feedback amplifier ($V_{I(fb)}$ - $V_{O(B)}$)	I_{diff} = 0; $I_{I(sb)}$ = 50 to 500 μA	–	–	18	mV
$\Delta V_{os}T$	output offset voltage as a function of temperature	I_{diff} = 0	–	–	72	μV/K
$V_{O(A)}$	DC output voltage	I_{diff} = 0; note 3	–	8.0	–	V
G_{vo}	open-loop voltage gain (V_{7-4}/V_{1-2})	notes 4 and 5	–	80	–	dB
	open loop voltage gain (V_{7-4}/V_{9-4}; V_{1-2} = 0)	note 4	–	80	–	dB
V_R	voltage ratio V_{1-2}/V_{9-4}		–	0	–	dB
f_{res}	frequency response (–3 dB)	open loop; note 6	–	40	–	Hz
G_I	current gain (I_O/I_{diff})		–	5000	–	
ΔG_cT	current gain drift as a function of temperature		–	–	10^{-4}	K
$I_{I(sb)}$	signal bias current		50	400	500	μA
I_{FB}	flyback supply current	during scan	–	–	100	μA
PSRR	power supply ripple rejection	note 7	–	80	–	dB
$V_{I(DC)}$	DC input voltage		–	2.7	–	V
$V_{I(CM)}$	common mode input voltage	$I_{I(sb)}$ = 0	0	–	1.6	V
I_{bias}	input bias current	$I_{I(sb)}$ = 0	–	0.1	0.5	μA
$I_{O(CM)}$	common mode output current	$\Delta I_{I(sb)}$ = 300 μA (p-p); f_i = 50 Hz; I_{diff} = 0	–	0.2	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Guard circuit						
I_O	output current	not active; $V_{O(guard)}$ = 0 V	–	–	50	μA
		active; $V_{O(guard)}$ = 4.5 V	1	–	2.5	mA
$V_{O(guard)}$	output voltage on pin 8	I_O = 100 μA	–	–	5.5	V
	allowable voltage on pin 8	maximum leakage current = 10 μA;	–	–	40	V

Notes

1. A flyback supply voltage of >50 V up to 60 V is allowed in application. A 220 nF capacitor in series with a 22 Ω resistor (dependent on I_O and the inductance of the coil) has to be connected between pin 7 and ground. The decoupling capacitor of V_{FB} has to be connected between pin 6 and pin 3. This supply voltage line must have a resistance of 33 Ω (see application circuit Fig.6).
2. The linearity error is measured without S-correction and based on the same measurement principle as performed on the screen. The measuring method is as follows:
   Divide the output signal I_4 - I_7 (V_{RM}) into 22 equal parts ranging from 1 to 22 inclusive. Measure the value of two succeeding parts called one block starting with part 2 and 3 (block 1) and ending with part 20 and 21 (block 10). Thus part 1 and 22 are unused. The equations for linearity error for adjacent blocks (LEAB) and not adjacent blocks (NAB) are given below
   $$LEAB = \frac{a_k - a_{(k+1)}}{a_{avg}};\ NAB = \frac{a_{max} - a_{min}}{a_{avg}}$$
3. Referenced to V_P.
4. V values within formulae, relate to voltages at or between relative pin numbers, i.e. V_{7-4}/V_{1-2} = voltage value across pins 7 and 4 divided by voltage value across pins 1 and 2.
5. V_{9-4} AC short-circuited.
6. Frequency response V_{7-4}/V_{9-4} is equal to frequency response V_{7-4}/V_{1-2}.
7. At $V_{(ripple)}$ = 500 mV eff; measured across R_M; f_i = 50 Hz.

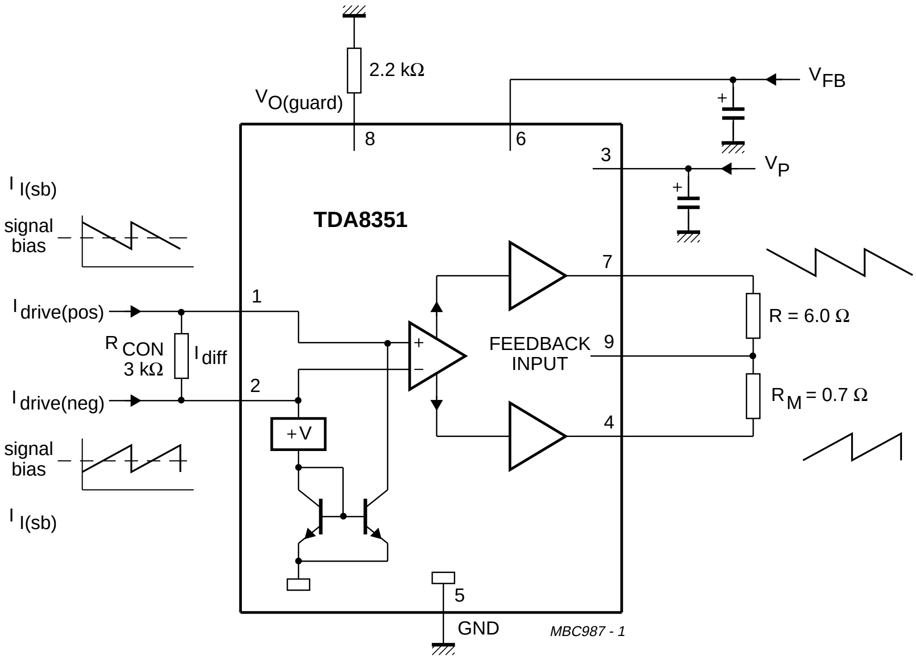


Fig.3 Test diagram.

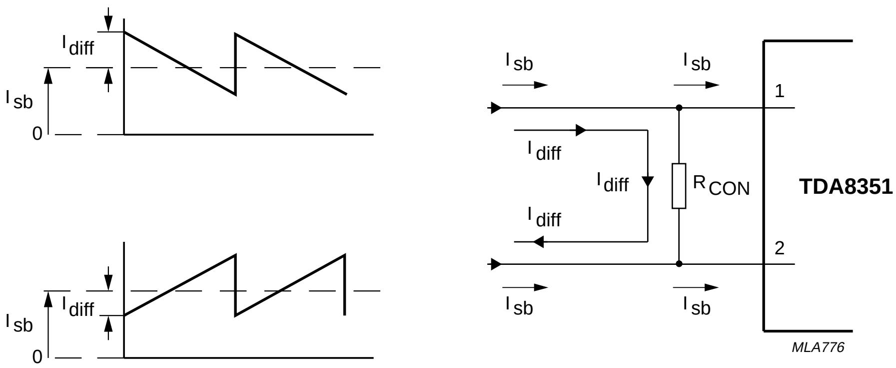
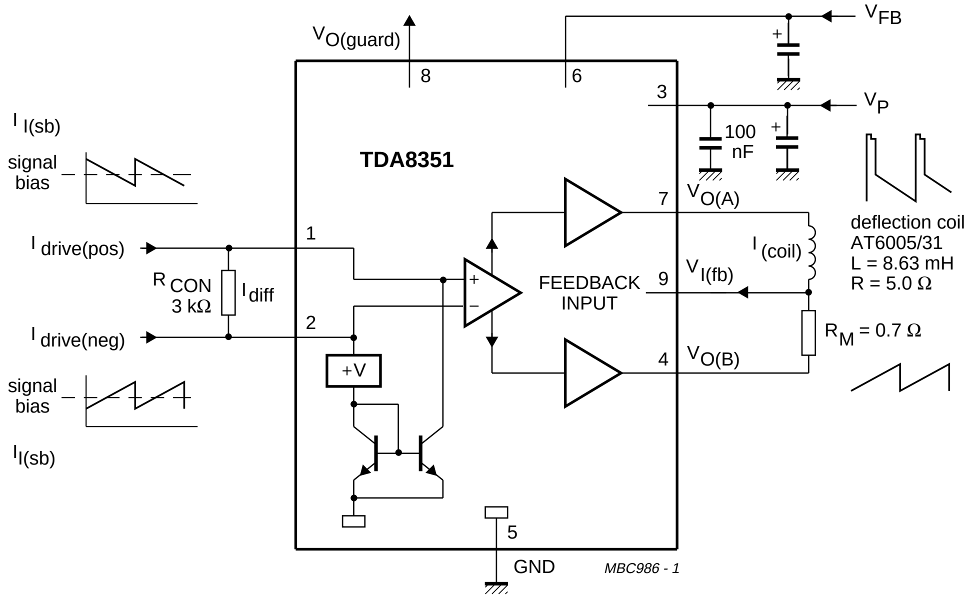


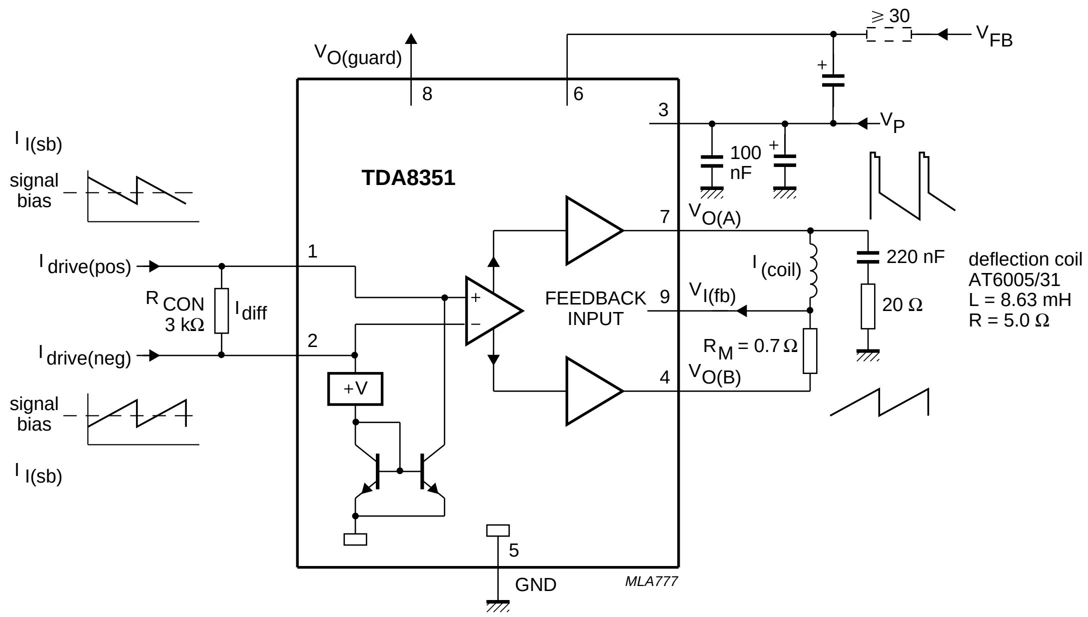
Fig.4 Input currents.

APPLICATION INFORMATION



V_P = 14 V; $I_{O(p\text{-}p)}$ = 2.14 A; $I_{I(sb)}$ = 400 µA; $I_{diff(p\text{-}p)}$ = 500 µA; V_{FB} = 42 V; t_{FB} = 0.6 ms.

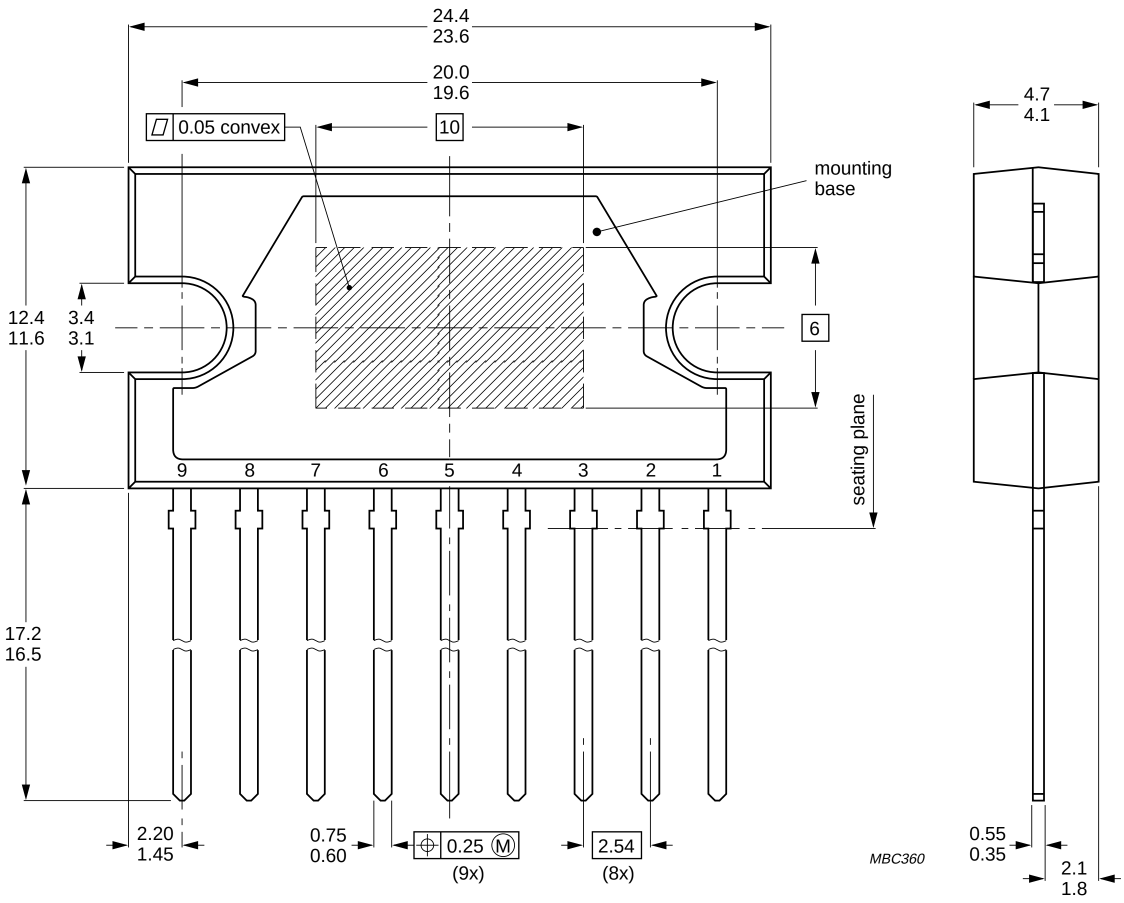
Fig.5 Application diagram.



V_P = 14 V; $I_{O(p-p)}$ = 2.14 A; $I_{I(sb)}$ = 400 μA; $I_{diff(p-p)}$ = 500 μA; V_{FB} = 60 V; t_{FB} = 0.4 ms.

Fig.6 Application circuit; 50 V ≤ V_{FB} ≤ 60 V.

PACKAGE OUTLINE



Dimensions in mm.

Fig.7 Plastic single-in-line power package; 9 leads (SIL9P; SOT131-2).

SOLDERING

Plastic single in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply the soldering iron below the seating plane (or not more than 2 mm above it. If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Printed in The Netherlands

533061/1500/02/pp16 Date of release: January 1995

Document order number: 9397 745 10011

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