Data and Application

Contents

1 INTRODUCTION AND CHARACTERISTICS 2

1.1 Features 2

1.2 Application 2

1.3 Block Diagram 2

1.4 Pin Configuration 3

1.5 Pin Description 3

1.6 Special Pins 4

2 FUNCTIONAL DESCRIPTION 5

2.1 Circuit Description 5

2.2 Funktional Flows 7

3 ELECTRICAL SPECIFICATIONS 11

3.1 Absolute Maximum Ratings 11

3.2 Recommended Operating Conditions 11

3.3 DC Characteristics 11

4 APPLICATION CIRCUIT 12

5 TIME CHARACTERISTICS 15

5.1 Time Characteristics Load of Parameters 15

5.2 Time Characteristics A/D converter RAM-Mode 15

5.3 Time Characteristics A/D converter RAM-Bypass- Mode 15

5.4 Time Characteristics Shift Register 15

5.5 Timing Load of Parameters (Figure 2) 16

5.6 Timing A/D converter RAM- Mode (Figure 3 17

5.7 Timing A/D converter RAM-Bypass- Mode (Figure 4) 18

5.8 Timing Shift Register (Figure 5) 19

1 Introduction and characteristics

The Graphic Signal Monitor IC was developed for visualization of the time behavior of electric signals. After loading of the parameters of time basis, trigger level and trigger mode into the control registers, the recording is started as soon as the trigger condition occurs. It ends when 128 data words have been written from the A/D converter into the internal SRAM. An externally connected microcontroller can then read the data and prepare it for an LC display or for transfer via an interface.

1.1 Features

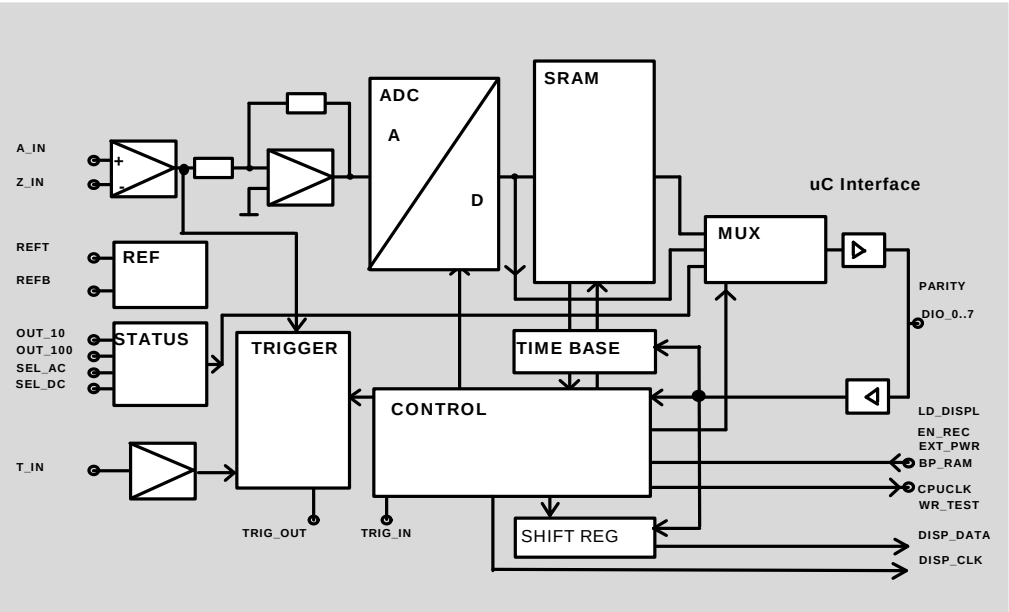
- A/D conversion with 6-bit resolution
- Time base programmable from 50ns to 3.27 ms (at a clock frequency of 20 MHz)
- Trigger Modes: Auto, Internal + /-, External + /-
- 5 discrete trigger levels
- Internal SRAM for 128 values
- SRAM bypass mode
- Shift of base line by adjustable offset
- Supply voltage 5 Volts
- Bidirectional µC interface
- Power-down for analog part
- PLCC44 package

1.2 Application

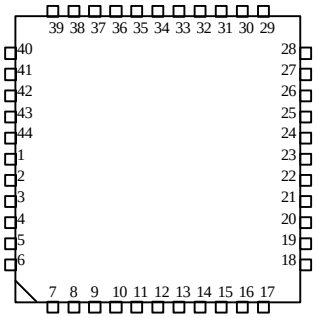
The small size as well as a minimum of external elements to be connected to the SCOPE IC facilitate both use in miniaturized measuring devices for service and test field purposes and also placement near the front panels of operator consols and switch cabinets.
Operating together with an external microcontroller, the function characteristics of a one-channel storage oscilloscope with additional DVM function can be implemented.

1.3 Block Diagram

Figure1.



1.4 Pin Configuration



1.5 Pin Description

Pin	Name	IN/OUT	Description
Power Supply Connections			
29	VDD		positive Power Supply Voltage, digital
38	VDDA		positive Power Supply Voltage, analog
17	VSS		negative Power Supply Voltage, digital
3	VSSA		negative Power Supply Voltage, analog
44	AGND		Signalground
Analog Inputs			
43	A_IN	I	Analog signal input
42	T_IN	I	Trigger analog signal input
41	Z_IN	I	Zero Level input
Digital Inputs			
1	OUT_10	I (puc)	Status 1 (10V Range switch status)
2	OUT_100	I (puc)	Status 2 (100V Range switch status)
10	SEL_AC	I (pu)	Status 3 (AC switch status)
9	SEL_DC	I (pu)	Status 4 (DC switch status)
34	N_MODE	I (pu)	Control1 (operating mode)
35	TRIG_IN	I	Trigger digital signal input
19	EN_REC	I	Enable Record
18	LD_DISPL	I	Load Display Data / Start Record / Read Data
16	EXT_PWR	I	Control 2 (External Power)
15	BP_RAM	I	Bypass Ram Mode
Digital Outputs			
8	PD	O (ub)	Analog power down (No output buffer !)
31	CPUCLK	O	5 MHz Clock (for external processor)
30	WR_TEST	O	Busy (RAM-Write-Mode activ)
36	TRIG_OUT	O	Trigger output
32	DISP_CLK	O	1,25 MHz Clock (for external display)
33	DISP_DATA	O	Display data serial
Data I/Os			
20	PARITY	bid	Bidirectional data pin (Control Out, Parity In)
28...21	DIO_0...DIO_7	bid	Bidirectional data interface
Analog Outputs			
6	REFT	O	Reference voltage (top)
5	REFB	O	Reference voltage (bottom)
4	VED	O	Internal base potential Ved

External Components			
12	XOUT		Crystal output
13	XIN		Crystal input
40	CF		Follower stage, Connection to trim-C
39	CZ		Amplifier, Connection to trim-C
7	CW		A/D converter power bypass capacitor
Test Pins			
11	TRESULT	O	Test mode output
14	TEST	I (pd)	Test mode input

pu = Internal Pull-Up puc = Internal Pull-Up Controlled pd= Internal Pull-Down
ub = Unbuffered output, drives only small current

1.6 Special Pins

N_MODE, EXT_PWR

Control pins for special applications, no internal processing. Both signals are combined internally, and the result is put out at the bidirectional PARITY pin during the SRAM readout.
Combination: N_MODE * /PWR_EXT = PARITY

CF, CZ, CW

Pins for connection of capacitors correcting the frequency response or blocking capacitor.
The pins are to be connected to:
CF= 47pF, CZ= 22pF, CW= 0,1µF

TRESULT, TEST

Pins for circuit test by manufacturer
Connect TEST to Ground, do not connect TRESULT

PD

High level at this pin signalizes the power-down state of the analog part. Since there is no output driver, the pin can be used for measurement purposes only.

2 Functional Description

2.1 Circuit Description

2.1.1 Input amplifier

The input amplifier has got two stages. It consists of a non-inverting operational amplifier (OPAMP) with subsequent inverting OPAMP.
The input amplifier serves for impedance transformation, amplifying the input signal by a factor of 2.5. A level shift is necessary to facilitate processing of bipolar input signals with only one supply voltage being available. This is implementd by using a pair of one enhancement NFET and one depletion NFET resulting in an artifical offset of 2.5 V. Such level shift can be varied by means of an external potentiometer, which results in a shift of the base line.
In order to facilitate short signal rise and fall times and to minimize overshoots, the integrated operational amplifiers have got a signal bandwith of approx. 40 MHz, and a slew rate of 60 V/µs.

2.1.2 A/D converter

The analog-to-digital converter is digitizing the measured signal.
It operates according to the flash principle, converting the input signal into a 6-bit digital word at a fixed conversion rate of 20 MHz when measurement is activated.

2.1.3 SRAM

The integrated circuit contains an **SRAM**, 6 bit wide and 128 values deep, for storaging measured data.

2.1.4 Trigger logic

The trigger logic consists of an analog and a digital circuit part.
The central element of the analog circuit part is a comparator, the reference level of which can be selected in five discrete stages. The reference level is generated by a resistor string between REFB and REFT and switching stages.
In the INTERNAL Trigger Mode, the non-inverting OPAMP of the input amplifier is switched to the comparator input, while the buffer OPAMP of pin T_IN pin is the source in the EXTERNAL Mode. The comparator has been provided with a hysteresis for noise rejection.
The comparator output signal is available at the TRIG_OUT pin.
In the basic application, the TRIG_IN input of the digital circuit part is connected with TRIG_OUT of the digital circuit part.
In the digital circuit part, the start of measurement is triggered, controlled by the parameters of trigger edge and trigger mode.

2.1.5 Time Base

Using a programmable counter, the **Time Base** unit generates the SRAM Write signal.
The 16 -bit time base information is loaded into the counter during the serial parameter transfer.
After the start of the measurement, the counter is clocked by the clock at XIN until the FFF Code is reached, then, a write signal is generated and the time base information is re-loaded into the counter.
The time base can be selected within the range from 2^0 to 2^{16} times the clock period t_{XIN}. Connection of a 20-MHz crystal oscillator will result in a range from 50ns to 3.27ms.

2.1.6 Control

The Control unit coordinates the circuit functions, parameter transfer, start of measurement, A/D conversion, writing into the SRAM and data exchange via the interface.
The Control logic activates the analog part of the circuit only during the short period of data recording.
The total power consumption of the integrated circuit therefore varies in dependence on the selected time base. The faster the 128 values are recorded, the shorter is the activation period of the analog part of the circuit and thus, power consumption is reduced. The analog part, when activated, typically consumes approx. 30 mA, while power consumption is significantly lower in the Power Down Mode.

2.1.7 Switch status

The measurement range can be extended by series connection of an external voltage divider. An AC input can be implemented by means of an additional external capacitor.
Two special inputs of the integrated circuit can be connected with the external voltage divider. In the measurement pauses, they supply a low current. The voltage resulting at the pins indicates the selected measurement range.
Two more pins, internally connected with pull-up resistors, have been provided for detection of the selected type of signal coupling. The external AC/DC switch should tie the pins to ground.
The status information from the four pins is applied to the multiplexer and is put out at the bidirectional interface, controlled by the Control logic.

2.1.8 Multiplexer

The multiplexer, controlled by the Control unit, switches one out of the three signal groups of "Status Signals", "SRAM Data", "A/D Converter Data", which are available at the input, to the output drivers of the bidirectional interfaces.

2.1.9 Bidirectional interface

Data exchange with a microcontroller is carried out via the bidirectional interface.
The transfer of parameters from the microcontroller into the SCOPE IC is serial, DIO(0) being used as clock inputand DIO(1) as data input. In contrast to this, the information intended for control of the shift register (see 2.1.10) are transmitted in parallel to DIO(0 to 7) and PARITY.
In the output direction, the data at DIO(0 to 7) and PARITY, provided by the multiplexer in parallel, is supplied to the bidirectional interface.

2.1.10 Shift register

The information applied to DIO(0 to 7) and PARITY is loaded in parallel into a shift register located in the IC. Adding a start and stop bit, the shift register puts out this information serially at the pins DISP_CLK (clock) and DISP_DATA (data).

2.1.11 Reference voltage generation

The reference voltages Vreft and Vrefb are provided, which are also available at the corresponding pins for external use, e. g. for implementation of a base line shift.

2.2 Funktional Flows

2.2.1 Loading of parameters

Principle

The parameters of time base, trigger level, trigger operation mode, trigger edge and trigger source are loaded into the integrated circuit.
This serial procedure takes place at the bidirectional DIO interface with DIO(0) being used as the clock input and DIO(1) as the data input.

Procedure

The data is applied to DIO(1). Upon the rising edge of the Clock, it is written into a 25-bit shift register at DIO(0).
For the programming of the parameters it is necessary to transfer exactly 25 data bits.

The timing is shown in Appendix **Figure 2** .

Serial bit sequence format:

TRG_EXT, TRG_INT, TRG+ /-, T_LEV4, T_LEV3, T_LEV2, T_LEV1, T_LEV0,VH_SPEED, LD15, LD14,.....LD1,LD0

Bit Code

Bits TRG_EXT und TRG_INT Trigger Mode

Function	**TRG_EXT**	**TRG_INT**
Trigger Extern- Mode ---> T_IN Trigger Input	1	0
Trigger Intern- Mode ---> T_IN dont care	0	1
Trigger Auto- Mode---> Start without trigger	0	0
No measuring	1	1

TRG+ /- Trigger Edge Selection

Funktion	**TRG+ /-**
Trigger low/high- transition on TRIG_IN	1
Trigger high/low- transition on TRIG_IN	0

VH_SPEED High Speed Time Base on/off

Function	**VH_SPEED**
Contents of LD15..LD0 ---> Time Base information	0
Time Base = t_{XIN}	1

T_LEV4..T_LEV0 Trigger Level selection

Trigger Level/mV	**T_LEV4**	**T_LEV3**	**T_LEV2**	**T_LEV1**	**T_LEV0**
-320	0	0	0	0	0
-140	1	0	0	0	0
+ 40	0	1	0	0	0
+ 220	0	0	1	0	0
+ 400	0	0	0	1	0
no trigger	0	0	0	0	1

The Bits LD15..LD0 contains the time base information.

Attention: If VH_SPEED = High, then LD15..LD0 dont care !

VH_SPEED	LD15..LD0	Time Base
0	LD15..LD0	t_{XIN} * (/LD15 * 2^{16} + /LD14 * 2^{15} + .../LD1 * 2^{2} + /LD0 * 2^{1})
1	XXXXXX	t_{XIN}

Example: LD15..LD2 = High, LD1 = Low, LD0 = High ---> Time Base = 200ns (bei f_{XIN}= 20MHz)

2.2.2 A/D converter internal RAM- Mode

Principle

The parameters have to be provided again before the start of each individual measurement. (see 2.2.1). After the start of the measurement series by a trigger signal, 128 measured values supplied by the A/D converter are written into the internal SRAM.

Procedure

The clock diagram can be seen from **Fig. 3** of the Appendix.

1. EN_REC = 1
The analog part leaves the Power-Down Mode, and the A/D converter starts working.
At each t_{XIN}, a measured value is provided. At this stage, however, the measured values are not yet written into the SRAM.
The Control Logic switches asynchronous to XIN the signals applied to the status pins via the output multiplexer to the bidirectional DIO port and activates the output drivers.

2. LD_DISPL = 1
DIO output driver asynchronous to XIN disabled.

3. LD_DISPL = 0
The circuit is registering the new state with the next L/H-transition of XIN and then waiting for trigger signal.

4.The internal Start State is entered by next rising edge on XIN when there was been an rising edge in the TRG **+** mode on TRIG_IN , or by a falling edge in the TRG **-** mode.

In the AUTO Trigger Mode the input signal TRIG_IN is dont care. The transition in internal Start-State is done automatic with the next rising edge on XIN.

Exact one clock later the circuit changes in the write state, output WR_Test= High and A/D-data available for writing in SRAM (in Bypass Mode output to DIO[5:0].
SRAM data and adresses are chanching every falling edge of XIN.

Clocked by the selected time base, 128 values are written into the internal SRAM, then the Control Logic goes into the Read state (int. Read Mode) switching the analog part to the Power-Down state.
Simultaneously, readiness for data transfer is indicated by WR_TEST = Low synchronous after L/H transition of XIN clock.

5. Read SRAM contents
The SRAM can readout at DIO(5:0] by an external LD_DISPL clock asynchronous to XIN.
Data changes with every rising edge of LD_DISP. The new data byte is available after an short setup time.

Output format:
Bits: DIO(0) LSB ....DIO(5) MSB, DIO(6)= High (int. Read Mode acive, DIO(7)= EXT_PWR
Bytes: Byte0, Byte1, Byte2,...Byte127

6. EN_REC = Low
Internal Read Mode off.

Coding of measured values

The A/D converter has a 6-bit resolution, corresponding to 64 stages.
Ahead of the A/D converter, there is the input amplifier.
The valency of a bit directly depends on the values of the reference voltages Vreft and Vrefb.

Equation 2.1shows the dependence of reference voltages, pre amplifier gain, input voltage and digital word

V_{A_IN} = - (Vreft-Vrefb)/64 *1/Gain * (DIO(5..0)hex -1F hex) (Equation 2.1)

With the typical values for Vreft, Vrefb and Gain we can write easy:

V_{A_IN} = - 16 mV * (DIO(5..0)hex -1F hex) (Equation 2.2)

The table shows the resulting values:

A_IN / V	DIO(5..0) HEX	A_IN / V	DIO(5..0) HEX
0,5	00	-0,1	25
0,4	06	-0,2	2B
0,3	0D	-0,3	31
0,2	13	-0,4	38
0,1	19	-0,5	3E
0	1F		

2.2.3 Operation of the A/D converter in the RAM Bypass Mode

Principle

Prior to the start of each measurement, the parameters have to be loaded newly (see 2.2.1).
After the start of the measurement series by a trigger signal, the results of the A/D converter, clocked by the frequency applied to XIN, are put out at the DIOs.
The integrated circuit functions as a universal flash A/D converter.

Procedure

The clock diagram is shown in **Fig. 4** of the Appendix.

A High potential is to be applied to the pin Pin BP_RAM.
At the beginning, the processes correspond to the ones of the RAM Mode, however, the data of the A/D converter is not put out into the SRAM, but to the bidirectional port.
Upon the falling edge of the clock at XIN, the data can be latched into the external circuit and the adresscounter can be after it incremented.
The code format, too, corresponds to the one of the RAM Mode.

2.2.4 Use of the shift register

Operating principle

The information applied to DIO(0 to 7) and PARITY is loaded in parallel into the shift register available in the IC. Adding a start and stop bit, e. g. for control of an LCD module, the shift register puts it out serially.

Procedure

The timing is shown in Appendix **Figure 5** .
The shift register clock DISK_CLK (L/H edge) is generated by use of XIN diveded by 16.
1. EN_REC= Low
2. LD_DISP= High
preparation of mode

3. EN_REC = High
With the first rising edge of DISP_CLK the circuit is registring EN_REC= High. With the next rising edge the data available at DIO(0 to 7) and PARITY are clocked in.
Behind it, the further state of the data lines and of EN_REC is of no importance.

4. With the next L/H transition of DISP_CLK is beginning the serial data output on DISP_DATA synchrounous to DISP_CLK. Data are certainly true during H/L-transition of DISP_CLK.

Output format:
STARTBIT (Low), DIO(0), DIO(1), ..., DIO(7), PARITY, STOPBIT (High)

5. Leaving the mode with LD_DISPL = Low.
EN_REC can be reseted in step 4 or step 5.

3 Electrical Specifications

3.1 Absolute Maximum Ratings

Parameter (VSS measurement ground)	**Symbol**	**Min**	**Max**	**Unit**
Power Supply Voltage	VDD	-0,3	7,0	V
Power Supply Voltage Analog Part	VDDA	-0,3	7,0	V
Power Supply Voltage Differenz VDD-VDDA		-0,3	0,3	V
Input-/Output- Voltages		-0,3	VDD+ 0,3	V
Input Voltages Inputs A_IN, T_IN, OUT_10, OUT_100		-2	VDD+ 0,3	V
Power Consumption	Pv		0,5	W
Operating Temperature Range	T_a	0	70	^oC
Storage Temperature Range	T_{stg}	-55	120	^oC

3.2 Recommended Operating Conditions

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Power Supply Voltage (VDDA= VDD)	VDD	4,75	5,0	5,25	V
Oszillator frequency	fq	5 *1)		20	MHz

*1) Smaller frequency possible but not guaranted.

3.3 DC Characteristics

(VDD= 5V,T_a= 25 ^oC)

Maximum Rating Parameters	**Conditions**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Power Supply Current	I_{VDD} + I_{VDDA}	IS		60 *2)	100	mA
Digital Inputs/Outputs						
Input-H-Level		VIH	VDD-0,8			V
Input-L-Level		VIL			0,8	V
Output-H-Level	IOH= -2mA (Pin32: -8mA)	VOH	2,4			V
Output-L-Level	IOL= 2mA (Pin32: 8mA)	VOL			0,4	V
Analog Inputs						
Input operating voltage		Vis,Vit	-0,5		+ 0,5	V
Input resistance		Ris,Rid	100			MΩ
Input capacity		Cis,Cit			5	pF
Signal input and trigger parameters						
Preamplifier Gain		Gain	2	2,28	2,5	
Zeroshift		Vz	Vrefb		Vreft	
Trigger level		$V_{trg}1$		-320		mV
		$V_{trg}2$		-140		mV
		$V_{trg}3$		+ 40		mV
		$V_{trg}4$		+ 220		mV
		$V_{trg}5$		+ 400		mV
Reference Voltages						
Internal base potential		Ved	2,3	2,47	2,7	V
Reference Voltage Top	Vreft - Ved	Vreft	1,1	1,25	1,4	V
Reference Voltage Bottom	vrefb - Ved	Vrefb	-1,4	-1,25	-1,1	V
A/D converter						
Resolution		radc		6		Bit
Scan Rate		fadc		20		MHz
Diff. Linearity Error		DNL			0,8	LSB
Int. Linearity Error		INL			1	LSB

*1) Record active

4 Application circuit

The application circuit in Fig.6 shows that the requirements on the circuitry for use of the SCOPE IC are low. Except from the analog input signals, the **synchronity** of the whole circuit should be given attention.
The clock frequency for the microcontroller is therefore provided by the SCOPE IC via the CPUCLK pin.
The clock given out is ¼ of the clock applied to XIN.

Shift of the base line
By means of R1,R2,R3 a votage is delivered to Z_IN.
Please note that REFT and REFB can provide only small currents, otherwise there is an influence to the values of the reference voltage.

Input external trigger action
R4, together with D1, protects the input against negative overvoltages. A diode to VDDA is contained in the SCOPE IC. The dimension of the C3 capacitor is to be selected big enough so that the capacitance of the line leading to the T_IN pin as well as the input capacitance of the IC is compensated.
It can bes necessary to shiled the input.

Signal input
The information given for the external trigger input applies correspondingly. C4 is to be sized accordingly.
R6 and R7 are the base point resistors of the input voltage divider. They are tied to ground depending on the measurement range. Using OUT_10 and OUT_100 the switch position is tested during the measurement stops.
Together with the levels applied to SEL_DC and SEL_AC, a status word is formed, which can be read by the microcontroller.

Trigger
Normally, the pins TRIG_OUT and TRIG_IN are connected. If 2 or 3 SCOPE ICs are cascaded, for multi-channel recording, one TRIG_OUT can connected to several TRIG_IN pins.

Compensation
C6 and C7 prevent overshoots of the input amplifier.

Oscillator
For generation of the system clock, a crystal oscillator can be connected directly to XIN and XOUT. An externally generated clock can be supplied as well.

Shift register
An intelligent LCD module can be connected directly to the DISP_DATA and DISP_CLK pins.
The information is written parallel into the bidirectional data port and it is transmitted serially.

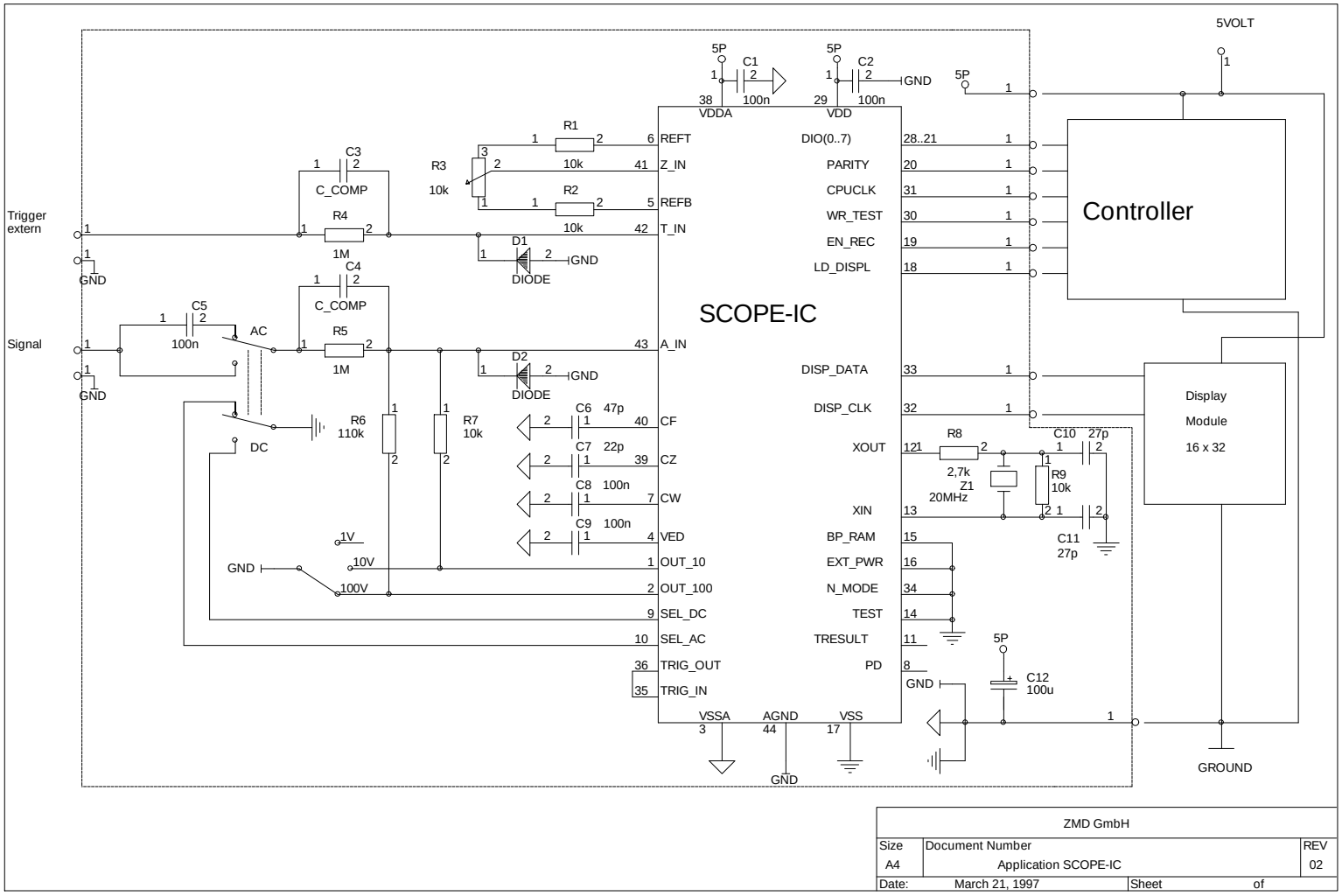
Grounding
In order to prevent oscillation and noise, all power supply pins should be bypassed with capacitors as close to the part as possible. The grounds are connected at one central point.

Communication with the microcontroller
Prior to every start of the measurement, the microcontroller has to load the parameters of time basis, trigger level and trigger mode serially to DIO(0) (clock) and DIO(1) (data).
The recording of measured values is prepared by activation of EN_REC.

Then, the IC puts out the status of the 4 pins for measurement range and AC/DC coupling in parallel at DIO(2 to 5), until a High pulse is applied to the LD_DISPL pin.
The integrated circuit is now prepared for the recording of measurement values, which starts as soon as the trigger condition occurs.
The trailing edge of WR_TEST signals the completion of the 128 SRAM Write cycles and the readiness of the SCOPE IC for readout.The evaluation of WR_TEST can be omitted, since the microcontroller "knows" the programmed time base. After 128 time base clocks, which always represent a multiple of the clock frequency of the microcontroller in the circuit as shown, the readout of the SRAM can start automatically.
By clocking of LD_DISPL, the microcontroller reads out the SRAM contents in bit-parallel and byte-serial form at DIO(0 to5).
The measured data and status information taken over are prepared in the external microcontroller in a way that allows to indicate them on the LC display or to transfer them to a computer, for instance, formatted according to the RS232 Protocol.

Shift Register
A shift register is available in the integrated circuit for special applications.
In the application as shown, it controls an LCD module of 16 x 32 pixels. The microcontroller loads the data applied in parallel to DIO(0 to 7) as well as the parity information into the register.
The process of loading is controlled by the EN_REC and LD_DISPL signals. A start and stop bit are added, then the serial output takes place at DISP_CLK (clock) and DISP_DATA (data).

Figure 6: Applikation SCOPE-IC



5 Time Characteristics

5.1 Time Characteristics Load of Parameters

Symbol	Parameter	Min	Max	Unit
t1	Dataq Setup Time	20		ns
t2	Data Hold Time		20	ns
t3	Clock	0,1	5	MHz

See Figure 2

5.2 Time Characteristics A/D converter RAM-Mode

Symbol	Parameter	Min	Max	Unit
t1	EN_REC to Status Valid		100	ns
t2	LD_DISPL to High-Z-Output	0		ns
t3	EN_REC to LD_DISP	$8*t_{XIN}$		
t4	LD_DISPL High Time	$4*t_{XIN}$		
t5	LD_DISPL back to TRIG_IN	0		ns
t6	TRIG_IN High	$2*t_{XIN}$		
t7	TRIG_IN to WR_TEST	$2*t_{XIN}$		
t8	WR_TEST Mode active	$128*t_{XIN}$		
t9	/WR_TEST to LD_DISPL	$2*t_{XIN}$		
t10	LD_DISPL High Time	50		ns
t11	LD_DISPL Low Time	50		ns
t12	/LD_DISPL to Data Valid	10		ns

See Figure 3

5.3 Time Characteristics A/D converter RAM-Bypass- Mode

Symbol	Parameter	Min	Max	Unit
t1	EN_REC to Status Valid		100	ns
t2	LD_DISPL to High-Z-Output	0		ns
t3	EN_REC to LD_DISP	$8*t_{XIN}$		
t4	LD_DISPL High Time	$4*t_{XIN}$		
t5	LD_DISPL back to TRIG_IN	0		ns
t6	TRIG_IN High	$2*t_{XIN}$		
t7	TRIG_IN to WR_TEST	$1*t_{XIN}$	$2*t_{XIN}$	
t8	WR_TEST Mode active to Data Valid	$1*t_{XIN}$	$1*t_{XIN}$	
t9	XIN fall to Data Valid	0	20	ns
t10	XIN	50		ns

See Figure 4

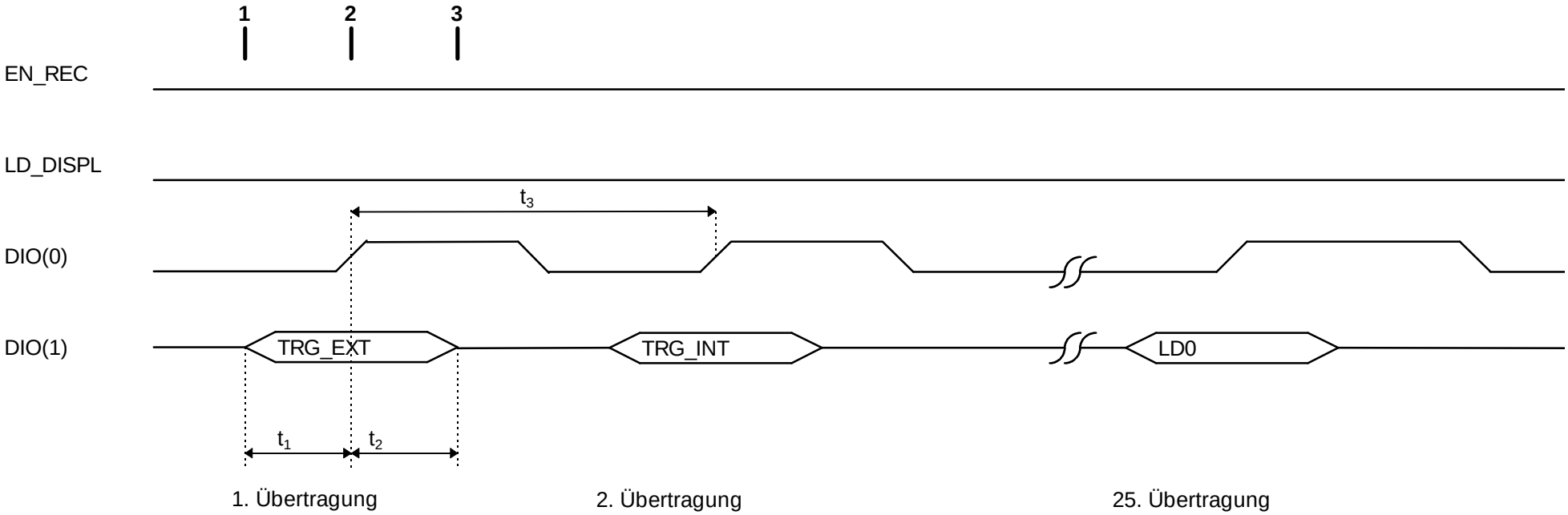
5.4 Time Characteristics Shift Register

$t_{DISP\_CLK} = 16 * t_{XIN}$

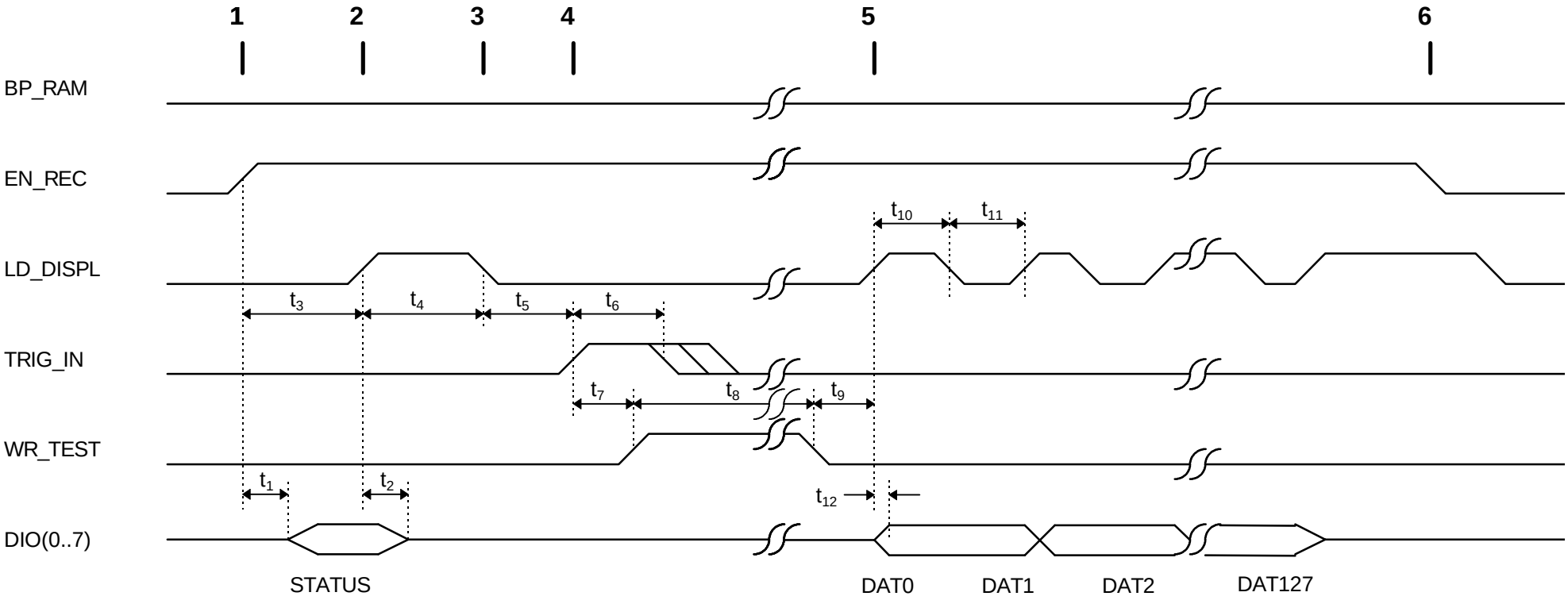
Symbol	Parameter	Min	Max	Unit
t1	LD_DISP High to EN_REC	$2*t_{XIN}$		
t2	Data Setup to EN_REC rise	0		
t3	Data Hold to EN_REC rise	$3*t_{DISP\ CLK}$		
t4	EN_REC active	$2*t_{DISP\ CLK}$		
t5	EN_REC rise to Serial Data Valid	$2*t_{DISP\ CLK}$	$3*t_{DISP\ CLK}$	
t6	LD_DISP active	$13*t_{DISP\ CLK}$		

See Figure 5

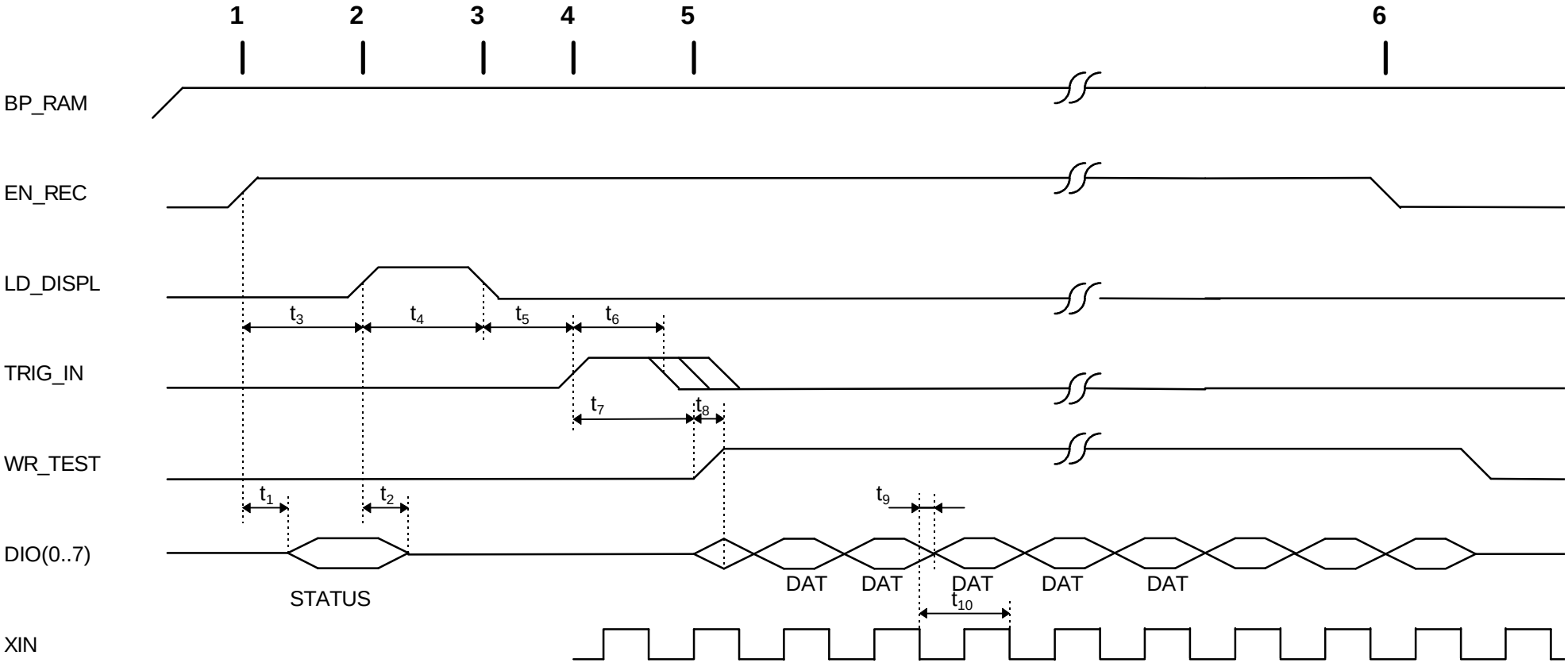
5.5 Timing Load of Parameters (Figure 2)



5.6 Timing A/D converter RAM- Mode (Figure 3



5.7 Timing A/D converter RAM-Bypass- Mode (Figure 4)



5.8 Timing Shift Register (Figure 5)