APPLICATION NOTE

ST7536

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SUMMARY

I - INTRODUCTION TO THE ST7536

The ST7536 is a half duplex synchronous FSK-modem, and has been designed to operate on powerline networks. For a complete communication system, a micro-controller and a powerline-interface (PLI) are needed (see Figure 1).

Such a system is able to transmit and receive on 4 different channels with 2 different data rates (600 and 1200 baud). The baudrate (BRS) and channel (CHS) selection is made, according to the Table 1:

Table 1

BRS	CHS	Bitrate	Xmit Freq (kHz) TxD = 1	Xmit Freq (kHz) TxD = 0
0	0	600	81.75	82.35
0	1	600	67.20	67.80
1	0	1200	71.40	72.60
1	1	1200	85.95	87.15

The ST7536 is a half duplex modem, as it has two operation modes; receive or transmit data. The mode selection is made with a Rx/Tx control input.

Data input and output are related to the clock signal ; it's a synchronous modem. This clock signal is generated by the ST7536.

Only a few external components have to be added for full operation of the ST7536 : a crystal, four resistors and five capacitors.

II - ST7536 DESCRIPTION

The ST7536 is a single chip modem; all the electrical circuits needed for a complete modem are inside the chip. The modem is available in 28 pins PLCC (see Figure 2).

In transmit mode the Transmit Data (TxD) is sampled on the positive edge of the clock (CLR/T). Then the data enters the FSK modulator. The frequency on which this modulator operates is set by the time base and control logic. In normal operation the multiplexer (MUX) selects the FSK modulator signal to be send to the transmit filter. This filter is a switched capacitor band-pass filter. The time base and control logic uses the Automatic Frequency Control (AFC) to set this filter at the transmit frequency, corresponding to the selected channel. After filtering, the transmit signal is sent to an Automatic Level Control (ALC). This control is used to overcome problems with line impedance variations. The powerlines on which the modem has to operate, have variations in their line characteristics, which are very frequent and totally unpredictable. The automatic level control uses a feed back signal (ALCI) from the powerline interface to adjust the transmit output (ATO).

In receive mode the signal enters the chip on the Receive Analog Input (RAI). The received signal is filtered in the receive band-pass filter. It's just like the transmit filter , a switched capacitor filter. The automatic frequency control is used to set it on the right frequency. After being amplified the signal is down converted and filtered in the intermediate frequency band-pass filter. The resulting signal is sent to the FSK demodulator. The coupling of the intermediate frequency filter output (IFO) to the FSK DEModulator Input (DEMI) is made by an external capacitor which cancels an eventual offset voltage. A clock recovery circuit extracts the receive clock (CLR/T) from the demodulated output (RxDEM) of the FSK demodulator. Synchronous received data (RxD) is delivered on the positive edge of the clock.

A time base section delivers all the internal clock signals from a crystal oscillator running at 11.0592MHz. The crystal is connected between the XTAL1 and XTAL2 pins. It is also possible to provide directly a clock signal on XTAL1 instead of using a crystal.

To debug the chip and test external circuits the ST7536 provides some test options. The transmit band-pass filter can be observed using a direct input on the filter. This input (TxFI) is selected by the multiplexer if TEST4 = 1. The Receive band-pass Filter Output (RxFO) is provided at pin 25. Finally the clock recovery can be observed when TEST1 = 1. In this case the TEST3 input gives a direct input to the clock recovery block.

Figure 1

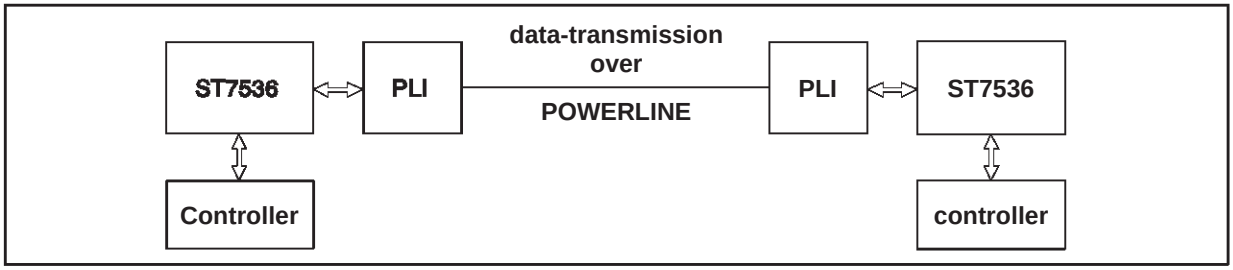
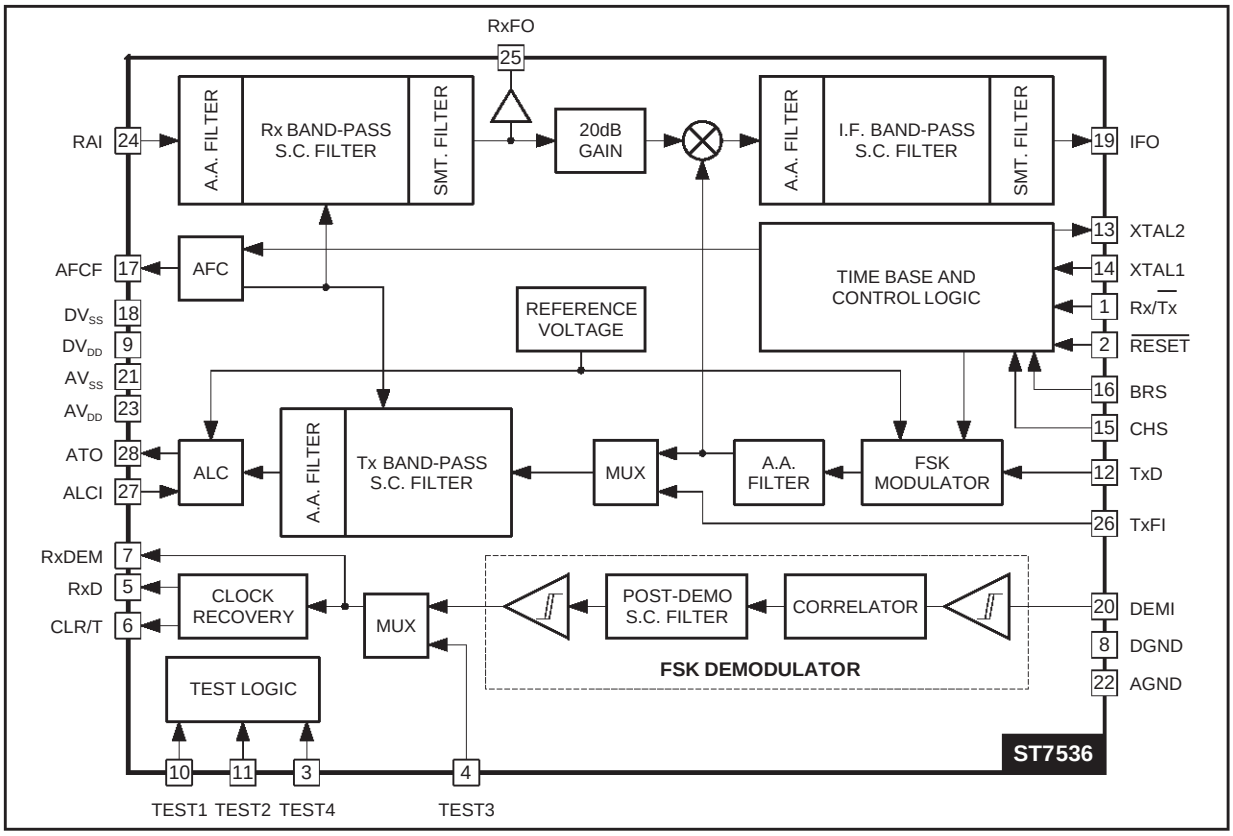


Figure 2 : Block Diagram



III - ST7536 PIN DESCRIPTION

The pin description is not given in numerical order, but the pins are described in relation with their function and consequently sometimes with other pins.

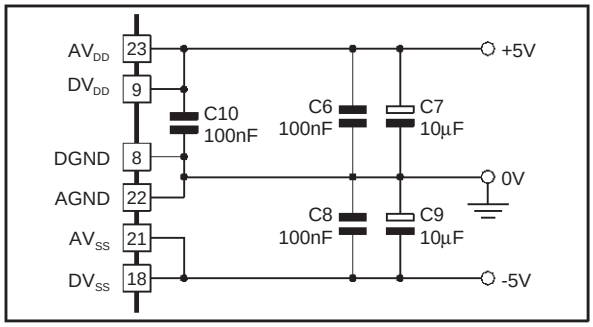
- power supply input
- channel selection
- crystal oscillator input
- AFCF stabilisation
- automatic level control input
- data input and output
- test inputs
- IFO/DEMI output/input
- transmit output and receive input
- Rx/Tx control input
- reset input

III.1 - Power Supply Input

- Pin 8 (DGND) : Digital ground (0V)
- Pin 9 (DV_{DD}) : Digital positive supply voltage (+5V)
- Pin 18 (DV_{SS}) : Digital negative supply voltage (-5V)
- Pin 21 (AV_{SS}) : Analog negative supply voltage (-5V)
- Pin 22 (AGND): Analog ground (0V)
- Pin 23 (AV_{DD}) : Analog positive supply voltage (+5V)

Internally the ST7536 has separated power supplies : the digital and analog circuits are separated. External the power supplies should be connected together. For decoupling, both the positive and negative supplies are decoupled with 2 capacitors. C6 and C7 decouple the positive, C8 and C9 the negative supplies. For proper operation the digital positive supply voltage should be decoupled with a capacitor (C10) mounted close to Pin 9. C6, C8 and C10 are 100nF/16V ceramic capacitors, C7 and C9 10µF/16V tantal capacitors (see Figure 3).

Figure 3



III - ST7536 PIN DESCRIPTION (continued)

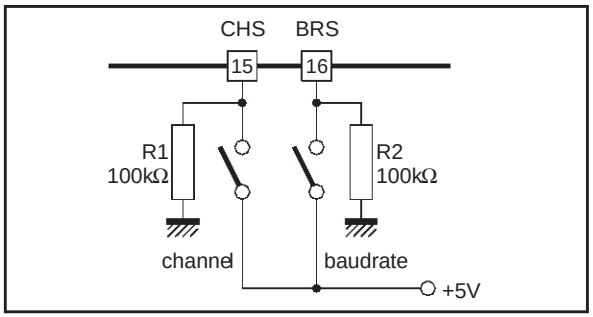
III.2 - Channel Selection

- Pin 15 (CHS) : Channel selection input
- Pin 16 (BRS) : Baudrate selection input

Both inputs are digital inputs (0/+5V). The ST7536 operates with two bitrates: 600 and 1200 baud. These bitrates are selected with pin 16 (BRS). For both bitrates the ST7536 offers two channels, which are selected with pin 15 (CHS).

A logical "0" is represented by 0V, a "1" by +5V. R1 and R2 are pull-down resistors, creating a logical "0". Closing a switch gives a "1". The selection is made according to Table 1.

Figure 4



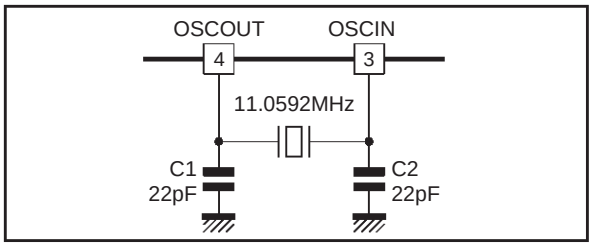
III.3 - Crystal Oscillator Input

- Pin 13 (XTAL2) : Crystal oscillator output
- Pin 14 (XTAL1) : Crystal oscillator input

The internal crystal oscillator of the ST7536 needs an external crystal. This one should be a 11.0592MHz crystal. Two capacitors (C1 and C2) have to be added for proper operation. They are typically 22pF/10V ceramic capacitors.

It is also possible to connect directly a clock signal to the oscillator input, in this case the crystal and the capacitors should be removed. On the application board this option is not used. The ST7536 clock signal is the time reference of the system.

Figure 5

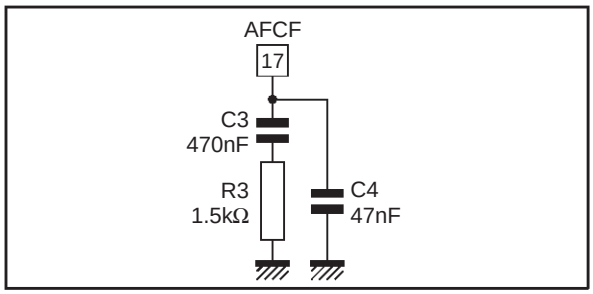


III.4 - AFCF Stabilisation

- Pin 17 (AFCF) : Automatic frequency control output

In the ST7536 an automatic control section adjusts the central frequency of the receive and transmit band-pass filters. The stability of this section has to be ensured with an external RC network.

Figure 6



III.5 - Automatic Level Control Input

- Pin 27 (ALCI) : Automatic level control input

The output stage of the transmit path consists of an automatic level control (ALC).
It offers the possibility to keep the output voltage of the power amplifier independent of variations of the powerline network. The impedance of these networks can be anywhere in the range of 5 - 100Ω. If the impedance of the powerline changes, the output of the amplifier will change. With the ALC input it is possible to correct these output variations. To control the output of the powerline interface a feed-back signal is needed. This signal is sent through an amplifier. The automatic level control can decrease the maximum transmit output in 32 steps of 0.84dB. The gain range is 0dB → -26dB. A peak detection is done on the signal presented on the ALCInput and the ALC compares it to two reference voltages, V_{T1} (1.87V) and V_{T2} (2.12V).

If max. VALCI < V_{T1} the next gain is increased by 0.84dB.

If V_{T1} < max. VALCI < V_{T2} there is no gain change.
If V_{T2} < max. VALCI the next gain is decreased by 0.84dB.

The gain of the feed-back amplifier is such that the feed-back signal peak voltage falls between V_{T1} and V_{T2}.

III - ST7536 PIN DESCRIPTION (continued)

Example:
The wanted interface output voltage is 0.5V(peak). For a 0.5V output peak voltage

$$G = \frac{V_{out\ peak}}{\left(\frac{V_{T1} + V_{T2}}{2}\right)} = \frac{0.5}{2} = 4\ (12dB).$$

Then the feed-back amplifier should have a gain of 4x (= +12dB). The ST7536 starts up. VALCI = 0V (VALCI < V_{T1}). The ATO output is increased with a gain of +0.84dB. On a certain moment the output voltage over the powerline will become 0.5V(peak). This signal is amplified to 2.0V(peak). Then the ALC stops increasing the ATO output, which will remain at its actual level. If the line impedance increases, the power amplifier of the interface might deliver more output voltage. If the output voltage of this amplifier increases, the ALCI voltage will be higher than V_{T2}. The ALC will then immediately decrease the ATO output. And so the output of the interface can be made independent of impedance variations of the powerline.

Of course this will operate only if the power amplifier in the interface is able to drive all the impedances at the required output voltage. Let's say the impedance of the line becomes 0.1Ω. The ALC will increase the output of the ATO. But if the power amplifier is not able to drive such low impedances, the only result will be an output signal with a large distortion. Therefore on the application board the ALC Input is set at 0V with a resistor (R4). The ATO will be always at maximum output (1.25 V_{RMS}). The powerline interface has been designed to drive all impedances from 0.5 - 100Ω with this input. To be able to do some experiments with the ALC, a resistor is used to set the ALCI at 0V. It gives the possibility to inject a signal on the ALCI. This would not have been possible if on the printed circuit board a short circuit to ground had been made (see Figure 7).

III.6 - Data Input and Output

- Pin 5 (RxD) : Synchronous receive data output
- Pin 6 (CLR/T) : Receive and transmit clock
- Pin 7 (RxDEM) : Demodulated data output
- Pin 12 (TxD) : Transmit data input

The ST7536 is a synchronous modem; data input and output are related to the clock (CLR/T). In transmit mode the ST7536 generates this clock signal. The transmit data are sampled on the positive edge of CLR/T. Therefore the TxD should be valid at that moment. In receive mode the demodulated (receive) data is available at pin 7 (RxDEM). A clock recovery circuit extracts the clock signal from the demodulated data and delivers synchronous data (RxD) on the positive edge of CLR/T.

On the application board the RxDEM data output is not used. All the data signals from and to the ST7536 (RxD, TxD) are related to the clock (CLR/T) (see Figure 8).

Figure 7

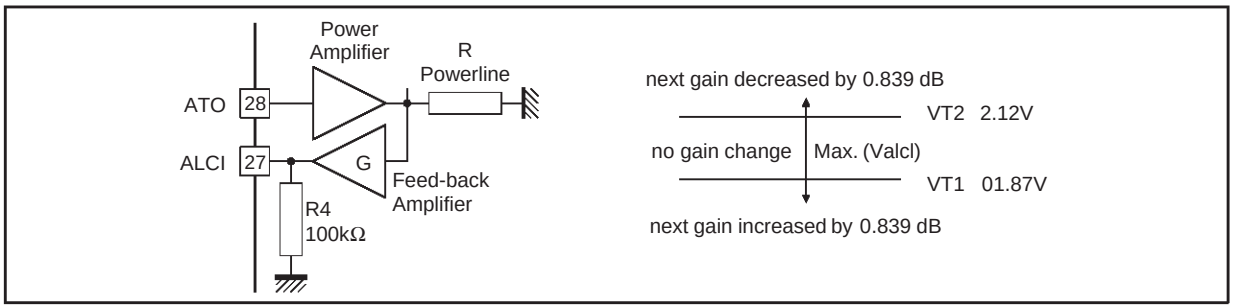
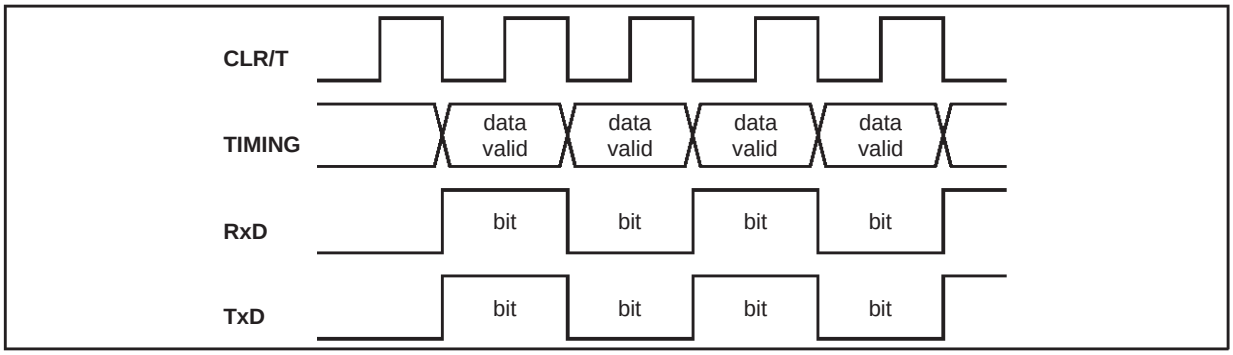


Figure 8



III - ST7536 PIN DESCRIPTION (continued)

III.7 - Test Inputs

- Pin 3 (TEST4) : Test input, with a "1" on this pin the multiplexer selects the transmit band-pass filter input (TXFI).
- Pin 4 (TEST3) : Test input which gives a direct acces to the clock recovery circuit.This input is selected when TEST1 = "1".
- Pin 10 (TEST1) : Test input, a "1" on this pin cancels the automatic switching from transmit to receive mode, and validates the TEST3 input to the clock recovery circuit.
- Pin 11 (TEST2) : Test input, a "1" on this pin reduces the automatic switching time (from transmit to receive mode) to 1.48ms.

On the application board TEST 2/3/4 are not used, and Pins 3, 4, and 11 are therefore set at 0V. With a switch TEST1 can be set at "0" or "1". See also the Rx/Tx control input.

III.8 - IFO/DEMI Output / Input

- Pin 19 (IFO) : Intermediate frequency filter output
- Pin 20 (DEMI) : FSK demodulator input

The connection between the intermediate frequency filter output and the FSK demodulator input should be made externally with a capacitor (C5, 1µF/10V).

III.9 - Transmit Output and Receive Input

- Pin 24 (RAI) : Receive analog input
- **pin 28 (ATO)** : Analog transmit output

Pin 24 is the receive input of the ST7536. The receive output of the powerline interface should be connected to this pin. The maximum input voltage is $2V_{RMS}$. The receive sensitivity of the ST7536 is $2mV_{RMS}$ f on channel 1 and 2 (600 baud), and $3mV_{RMS}$ on channel 3 and 4 (1200 baud).

Pin 28 is the transmit output of the ST7536. The transmit input of the powerline interface should be connected to this pin. The ATO output is regulated by the ALCI circuit. The maximum output voltage is $3.5V_{PP}$. The second harmonic distortion is about -53dB.

III.10 - Rx/$\overline{Tx}$ Control Input

- Pin 1 (Rx/$\overline{Tx}$) : Receive or transmit mode selection input

The ST7536 is a half duplex modem and has therefore two operation modes: receive and transmit. This mode selection is done with the Rx/$\overline{Tx}$ input. The transmit mode is selected when Rx/Tx is "0". If Rx/Tx is held at "0" longer than 3 seconds, the ST7536 switches back to receive mode. To set the ST7536 again in transmit mode, Rx/Tx should be held at "1" for a minimum of 3µs before being set to "0".

The carrier activation time is 1msec.

To be able to observe the transmit output of the ST7536 on the power line interface for a longer time than 3 seconds it is possible to use the test 1 Input. If this input is set at "1" the automatic switching is disactivated.

Then it is possible to transmit a signal but not to receive.

III.11 - Reset Input

- Pin 2 (RESET) : Logic reset and power-down input

When this input is set at "0" the ST7536 is in power-down mode. All the internal logic is then reset. For normal operation this input should be set at "1". On the application board this input is controlled by the micro-controller.

IV - POWERLINE INTERFACE

The power line interface (PLI) connects the ST7536 to the powerlines.The following PLI has been designed according to the ENEL (italian electricity distributor) specifications : (This PLI is suitable to CENELEC european specification and the FCC USA spec) (see Figure 9).

transmit output :

R powerline > 5Ω → 1 - 2 V_{RMS}
R powerline < 5Ω → 200-400mA_{RMS}
Second Harmonic Distortion ← 72dB
for R powerline = 18Ω
receive sensitivity : 1.5mV_{RMS}

In transmit mode the powerline interface amplifies and filters the transmit signal (ATO) from the ST7536. The maximum output current that can be taken from ATO is 1mA. Therefore a buffer is used to protect the ST7536 and in order to drive the next stages in the powerline interface. The Second Harmonic Distortion (HD2) of the transmit signal from the ST7536 is -53dB. To suppress the harmonics a low pass filter (LPF) is used. The filtered signal is then sent to a power amplifier, which must drive powerlines with impedances from 1 to 100Ω, via the transformer. The transformer is not only used to put signals on the powerlines. It's also used as a band pass filter, in order to suppress the second harmonic of the transmit signal to a level of less than -72dB.

In receive mode the transformer extracts the signal from the powerline. Before sending it to the receive input (RAI) of the ST7536, it is amplified with a level of 34dB in the preamplifier.

The buffer and power amplifier are switched off in receive mode, in order to avoid the low output impedance of the power amplifier attenuating the received signals.

IV.1 - Buffer and Low Pass Filter

These two functions are build up around UA1 (see Figure 10).

Figure 9

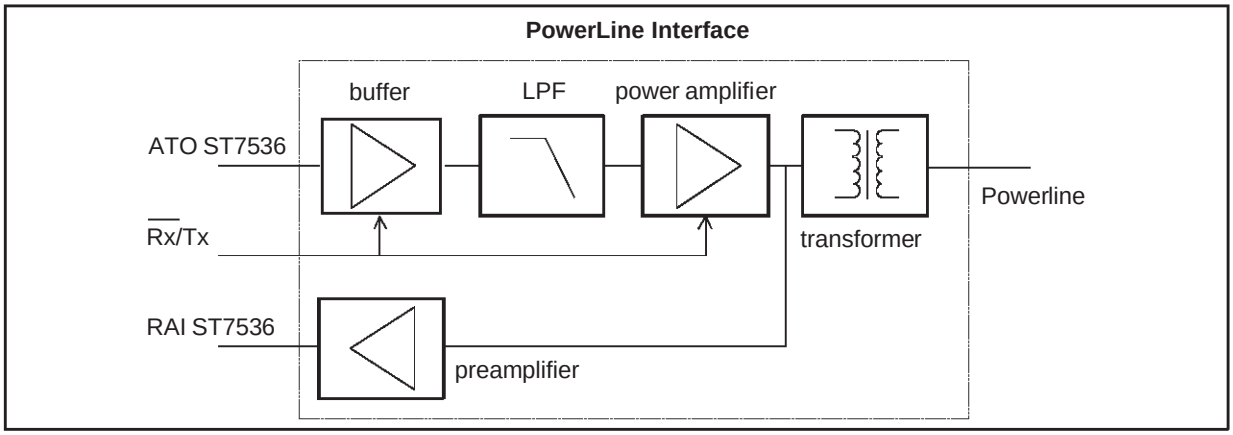
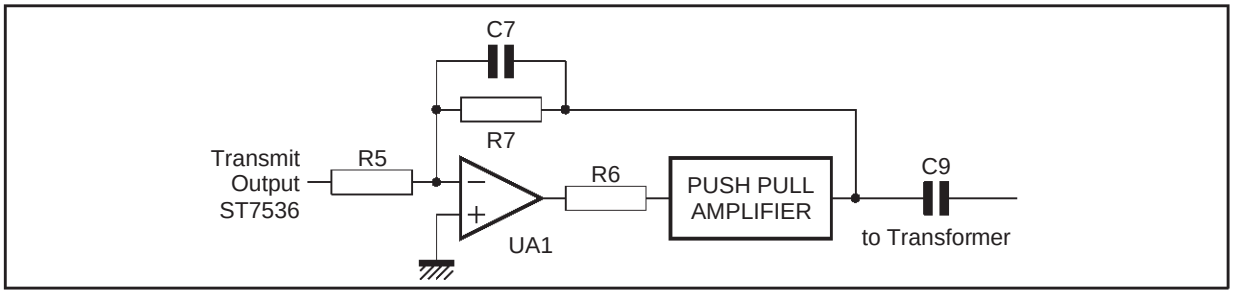


Figure 10



IV - POWERLINE INTERFACE (continued)

A feed back from the output of the power amplifier to the operational amplifier is done with R7/C7. This gives a low pass function and therefore the possibility to create a low pass filter.The ST7536 operates on 4 channels : 67, 72, 82 and 86kHz. With R7 and C7 the cut off frequency of this filter is set.If this frequency is set at 75kHz, the difference between 75kHz and 150kHz (second harmonic) signals is only 3dB,because such a filter has already an attenuation of 3dB at the cutoff frequency (see Figures 11 and 12).

Figure 11

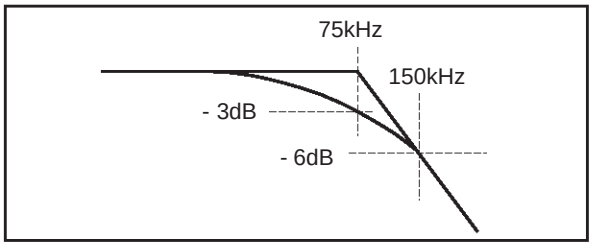
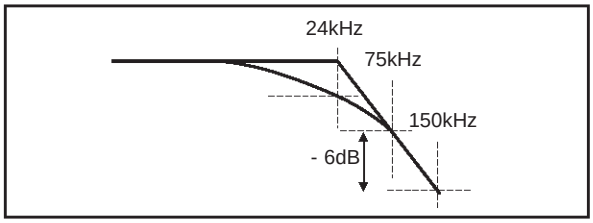


Figure 12



To ensure an attenuation of 6dB of the second harmonic, the cut off frequency has been set at 24kHz.

With ER7 = 10kΩ, f = 1/(6.28*R7*C7) = 24kHz and C7 = 680pF.

The ratio R7/R5 provides sufficient amplification on the transmit frequency, to drive the power amplifier at optimum performances.The frequency differences of the four channels result in a different output of the low pass filter. Therefore the ratio of R7/R5 is not the same for all the four channels.

Channel	R7 (Ω)	R5 (Ω)	ATO (V_{PP})
1	10k	1500	3.3
2	10k	1800	3.6
3	10k	1800	3.5
4	10k	1500	3.2

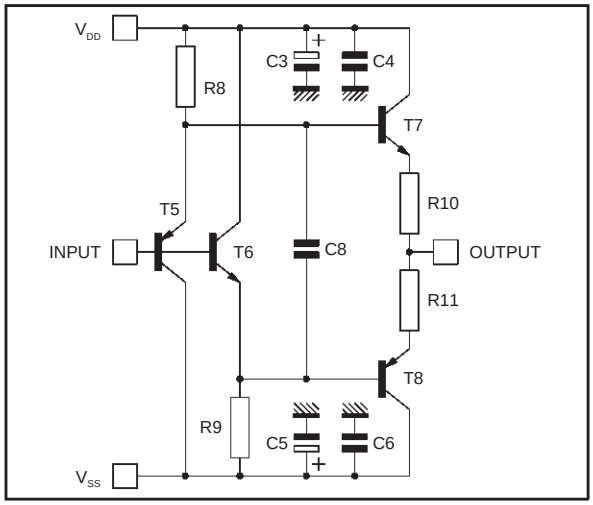
The connection of the operational amplifier to the power amplifier is done with R6. This resistor is added to avoid oscillation. Without this resistor stable operation cannot be guaranteed. The value of R6 is determinated with experiments to be 330Ω.

An other function of R6 is to increase the load impedance seen by the operational amplifier. The impedance is R6 plus the input impedance of the power amplifier. If this impedance is to low the operational amplifier will not be able to drive the power amplifier in optimum performances. The maximum voltage swing will decrease and the second harmonic distortion will increase. Different operational amplifiers have been tested. The TL071C gives the best performances.

IV.2 - Power Amplifier

The power amplifier increases the output signal of the operational amplifier and low pass filter (UA1).

Figure 13



The input impedance is increased because it's multiplied by the Beta of T5/6, which are no longer used as diodes. Therefore R8 and R9 could be decreased, to deliver more current to T7/T8. The optimum performances of the amplifier were obtained with a value of 820Ω for R8 and R9. An other solution to deliver more current to the output transistors is the addition of C8. It will decrease the input impedance, but also deliver extra current to T7 by T6, and to T8 by T5. Other transistors have been used also a BD237 for T6/T7, a BD238 for T5/T8. These transistors can deliver more output power, and are not much expensive than the 2N2222/2N2907.Furthermore, the collectors are connected to the (metal) package. This gives the possibility for a mechanical connection of T5/T8 and T6/T7. This will result in the same temperature in both transistors, what will avoid thermal runaway. To decouple the power supplies C3/C5 (22µF/16V) and C4/C6 (100nF/16V) are used, mounted close to T7 and T8.

Using this configuration, it is possible to provide $1 \rightarrow 2$ V_{RMS} in powerlines with impedances from $5 \rightarrow 100\Omega$.

IV - POWERLINE INTERFACE (continued)

IV.3 - Transformer

A transformer is used to connect the power amplifier and the preamplifier to the powerline.This transformer has to :
- separate the rest of the interface from the powerline,
- put the transmit signal on the powerline,
- extract the received signal from the powerline,
- filter the 50/60Hz signal coming from the powerline,
- filter the second harmonic of the transmit signal.

The transformer is a TOKO T1002N,which has two primary windings and one secondary winding. The ratios of the windings are 4:1:1 (turns) (see also the Figure 14).
Typical values of the transformer are :
- L1t windings : 9.4µH,
- L4t winding : 140µH.

The primary windings of the transformer are used to create a bandpass filter. The resonance frequency is set at the transmit frequency with C10/C11. These capacitors are in parallel with the primary windings (1t/4t). The equivalent value for those two windings can be calculated according to:

$$Leq = L1t + L4t + 2M \quad (16)$$

$$M = k \cdot \sqrt{L1t \cdot L4t} \quad \left(k = \frac{1}{\sqrt{2}}\right)$$

With the given values:

$M = (9.4\,\mu H * 140\,\mu H)^{0.5}$
$= (1316\,\mu H)^{0.5} = 36.3\,\mu H$
$Leq = L1t + L4t + 2 \cdot (L1t \cdot L4t)^{0.5}$
$= 9.4\mu H + 140\mu H + 2 \cdot 25.6\mu H = 200\mu H$

The resonance frequency of this LC network is dependent of Ceq = Cp = C10//C11 and Leq according to:

$$f_{res} = \frac{1}{2\pi \times \sqrt{L_{eq} \cdot C_p}} \quad (17)$$

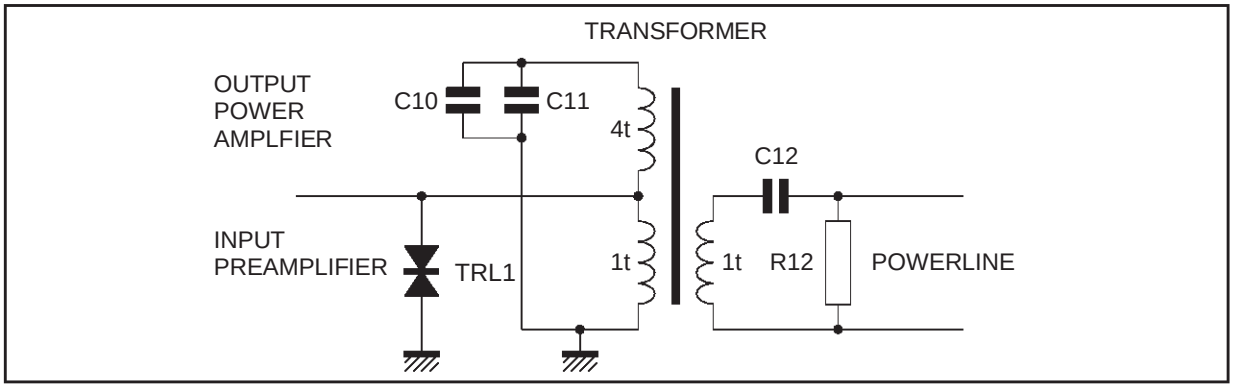
$$C_P = \frac{\left(\frac{1}{2\pi \cdot f_{res}}\right)^2}{Leq} \quad (18)$$

As this filter is very sharp, there are different values for C_P on each (transmit) frequency.

channel 1 : f = 82kHz → C_P = 18nF = 10nF // 6.8nF
channel 2 : f = 67kHz → C_p= 28nF = 22nF // 6.8nF
channel 3 : f = 72kHz → C_P = 24nF (only 1 capacitor)
channel 4 : f = 86kHz → C_P = 17nF = 10nF // 5.6nF

On channel 3 only 1 capacitor is needed and therefore C11 doesn't exist. On a printed circuit board the capacitors should be mounted close to the transformer. In order to get the best filter performances.The capacitors (C10/C11) have to be linear, such as the KS (styroflex) types.
C12 is used to filter the 50/60Hz signal from the powerline. The capacitor filters low frequencies 50/60Hz and lets the high (transmit) frequencies pass. The capacitor is a class X2 capacitor. These capacitors have a short circuit protection, which is absolutely necessary,because in case of a short circuit in the capacitor, the 50/60Hz filtering is lost, and the powerline interface will be destroyed, or might be dangerous for persons working with the interface and the ST7536.
As a final protection against any possible spikes, a transil (TRL1) is used. It is a 6.8V bipolar type. If a voltage 6.8V appears, the transil will act as a short circuit to ground, protecting the other parts of the powerline interface from damage.
R12 is added to discharge C12 after disconnecting the interface from the powerline. Without this resistor, C12 will not be discharged and shock hazard might occur if someone touches the powerline connector. This resistor is only usefull in evaluation systems. In all other cases when disconnecting from the powerline never takes place R12 can be removed.

Figure 14

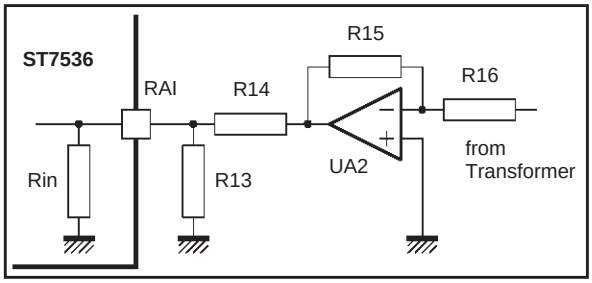


IV - POWERLINE INTERFACE (continued)

IV.4 - Preamplifier

Receive signals on the powerline are extracted by the transformer and (pre)amplified before sending them to the Receive Analog Input (RAI) of the ST7536. This is done to have, according to the specifications, a receive sensitivity of 1.5mV$_{RMS}$. The sensitivity of the ST7536 is 2mV$_{RMS}$ for channel 1 & 2, and 3mV$_{RMS}$ for channel 3 & 4. To increase the sensitivity the received signal is filtered in the transformer, and then amplified with a gain of 40dB. A limiter is used to protect the ST7536 against signals > 2V$_{RMS}$.

Figure 15



In receive mode the power amplifier is virtually disconnected from the power supply, in order to avoid its low output impedance attenuating the received signals. Signals that are extracted from the powerline are filtered in the transformer, in the same way that the transmitted signals.

After filtering, the signals are amplified. This is done with UA2, an inverting amplifier. The gain of this amplifier is set with R15 and R16.

gain = R15/R16 = 100k/1k = 100 x = +40dB

The maximum input level at the RAI is 2V$_{RMS}$. Therefore the signals coming from the preamplifier have to be limited to avoid transmodulation to the ST7536. Amplifier UA2 operates with a power supply of -5V and +5V. The maximum output voltage of the amplifier is then ± 4V. With R13 and R14 a simple limiter has been created. The output voltage of this limiter is the voltage over R13. The input resistance of the RAI (Rin) is 100kΩ.

The gain of the limiter
= (R$_{IN}$//R13) / (R$_{IN}$//R13 + R14)
= (100k//47k) / (100k//47k + 47k) = 0.4 x (= -8dB)

With a maximum output of the amplifier of 4V, the maximum output of the limiter is set at 0.4 x 4V = 1.6V. Strong input signals are clamped by UA2, but tests showed that this clamping has no effect on correct demodulation.

The total gain of the preamplifier is: +40dB + -8dB = +32dB providing the required receive sensitivity of 1.5mV$_{RMS}$.

IV.5 - Power on/off Switch

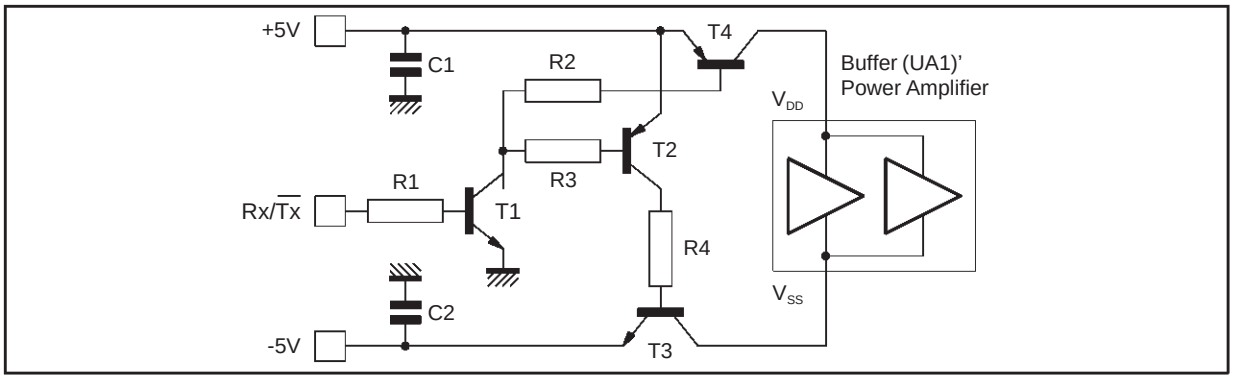
The powerline interface has two operation modes: transmit and receive. Normally the ST7536 system (and therefore the interface) is in received mode, waiting for commands or data requests from the master system. The interface will be used in transmit mode, only when the system has to respond to the master.

To save energy costs, the buffer and power amplifier in the transmit path are switched off. Also if the interface is used in a master system, which will be often in transmit mode, this switching can be usefull.

A second reason to switch off the transmit power amplifier is the fact that its low output impedance will attenuate the incoming signals in receive mode. Therefore the power amplifier is virtually disconnected from the power supply (see Figure 16).

Switching the positive (V$_{DD}$) and the negative (Vss) input voltage is done with T3 & T4. If these transistors are switched off the high resistance of the collectors will provide the virtual disconnection. In transmit mode these transistors are switched on, and the voltage lost over the transistors (V$_{CE}$) will be 0.2V.

Figure 16



IV - POWERLINE INTERFACE (continued)

The control of the switch is done with a Rx/$\overline{Tx}$ control line from the controller. In transmit mode this line is +5V, in receive mode 0V. The +5V will open T1, which delivers the base current for T2 and T4. T3 is switched by T2.

In transmit mode the buffer and power amplifier will operate with HF-signals (the transmit signals have frequencies67...86kHz). Therefore the input (± 5V) of the switching transistors has to be decoupled. This is done with C1 and C2, which have both a value of 100nF.

R1 is 47kΩ, to create a high input impedance. R2, R3 and R4 are 270Ω. T1 and T3 are a 2N2222, T2 and T4 the equivalent pnp version; a 2N2907. These transistors can deliver a maximum current of 0.8A, more than enough for the buffer and power amplifier.

IV.6 - Building-up the Powerline Interface

The whole described parts make a complete powerline interface. The interface has to be connected to the ST7536 as described before.

Because the interface is supposed to operate with the ST7536, the input and output names correspond to the related pin names of the ST7536. for instance : the ATO pin of the ST7536 should be connected to the ATO pin of the powerline interface.

The ATO and RAI are the analog output and input from/to the ST7536. The Rx/$\overline{Tx}$ control input is connected to the controller. The controller switches the interface from transmit mode to receive mode and vice versa. The ± 5V inputs are connected to the power supply connections of the application board. These inputs are HF-decoupled on the board. See also the schematic of the ST7536. If the interface has to operate separated from the application board, using an external power supply, the ± 5V inputs should be decoupled with four capacitors (see Figure 17).

The operation mode of the interface is set with the Rx/$\overline{Tx}$ input line. A high input (+5V) on this line selects the transmit mode, a low input (0V) selects the receive mode. A micro-controller has to be used to control this input.

The 'power line' outputs are the powerline connections. On the application board these connections are located close to C12 and the transformer, to avoid long tracks carrying high voltage.

IV.7 - Performances of the Powerline Interface

The following tests have been done on the powerline interface :
- power consumption
- transmit output
- receive sensitivity

All the tests are done with the powerline interface connected to the ST7536.

IV.7.1 - Power consumption

The power consumption is measured both in transmit and receive mode.
In both modes the powerline has been simulated with a 5Ω resistor (worse case simulation). In transmit mode the data input (TxD) was a logical 0 (0V).

The results remained the same for the four channels.

The current consumption :
The input voltage : - 5.00V, + 5.00V
- transmit mode : - $150mA_{RMS}$, + $180mA_{RMS}$
- receive mode : - $1mA_{RMS}$, + $1mA_{RMS}$

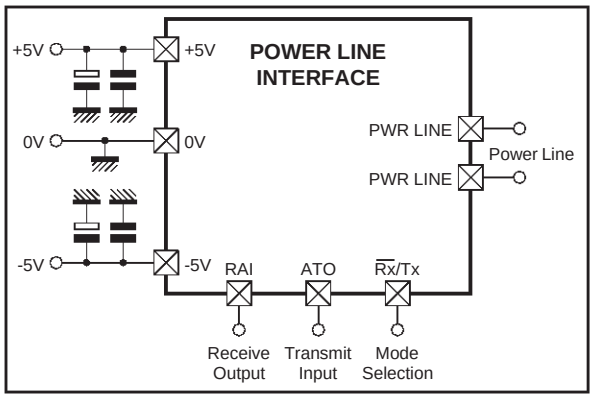
The power consumption :
- transmit mode : -5V x -150mA + +5V x +180mA
  0.75W + 0.9W = 1.65W
- receive mode : -5V x -1mA + +5V x +1mA
  5mW + 5mW = 10mW

In transmit mode the powerline interface delivered 0.340 W into a 5Ω load. With an input of 1.65 W the efficiency is 20%. This does not imply a waste of energy. A ST7536 system is almost allways in receive mode, and the lost of energy is consequently limited.

In receive mode the buffer and the power amplifier are switched off. Power is only consumed by the preamplifier. This explanes the low power consumption in receive mode.

Test equipment : Keithley 165 Multimeter
Test conditions : T = +25°C

Figure 17



IV - POWERLINE INTERFACE (continued)

IV.7.2 - Transmit output

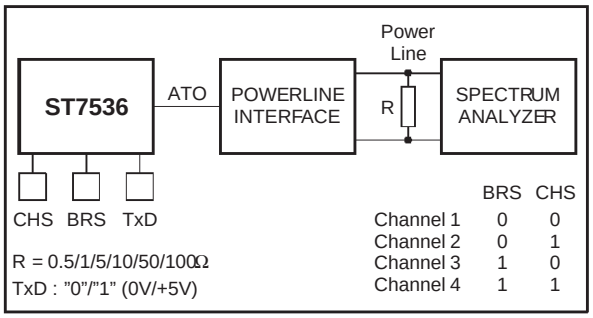
The transmit output of the powerline interface is measured with the powerline simulated by resistors.

The interface is tested on the four channels. On each channel the ST7536 uses two signals : one for TxD = 1 (lower freq.) and one or TxD = 0 (higher freq.) Therefore the output on each channel is measured for TxD = 1 and TxD = 0. This makes 4 (channels) x 2 (TxD 0/1) = 8 signals to test.

The powerline is simulated with resistors. Six different impedances are tested : R = 0.5, 1, 5, 10, 50, 100Ω.

A spectrum analyzer is used to test the output of the powerline interface It measures the output power and generates a frequency spectrum plot. With this plot the harmonic distortion can be calculated (see Figure 18)

Figure 18



Test results. (see ANNEXE B)

With the spectrum analyzer the output power on the transmit frequency (H1) is measured. Then the power of the harmonics is measured. The difference between those two signals is the harmonic distortion.

Example : TxD = CHS = BRS = 0
(channel 1, txd = 0 → 81.75kHz.)
R powerline = 5Ω.

H1 : f= 81.75kHz, measured power = +15.2dBm.
H2 : f = 163.5kHz, measured power = -58.8dBm.

The difference between H1 and H2 is + 15.2dB - -58.8dB = 74dB.
The second harmonic of the signal is in this case suppressed to a level of -74dB (compared to H1).

The measured output power of H1 = +15.2dBm. Then the output voltage can be calculated.

0 dBm is 1mW power into a resistor of 50Ω. So +15.2 dBm is 33mW power into a resistor of 50Ω. Vout(rms) is therefore (33mW * 50Ω)^0.5. In this case the output voltage is $1.29V_{RMS}$.

The output current is also calculated :
$I_{OUT(RMS)} = V_{OUT(RMS)} / R$.
For example; the output voltage with R powerline = 0.5Ω is $0.18V_{RMS}$. Then the output current is $360mA_{RMS}$.

Channel 1 : 82kHz

Rline (Ω)	Output (V_{RMS}) TxD = 1	Output (V_{RMS}) TxD = 0	H2 (dB) TxD = 1	H2 (dB) TxD = 0
0.5	0.18	0.18	-51	-54
1	0.31	0.31	-51	-55
5	1.29	1.29	-74	-76
10	1.70	1.68	-77	-81
50	2.06	2.02	-74	-77
100	2.09	2.06	-74	-76

Channel 2 : 67kHz

Rline (Ω)	Output (V_{RMS}) TxD = 1	Output (V_{RMS}) TxD = 0	H2 (dB) TxD = 1	H2 (dB) TxD = 0
0.5	0.16	0.16	-67	-68
1	0.28	0.28	-68	-68
5	1.21	1.20	-75	-75
10	1.70	1.65	-78	-75
50	2.16	2.11	-83	-75
100	2.21	2.16	-84	-75

Channel 3 : 72kHz

Rline (Ω)	Output (V_{RMS}) TxD = 1	Output (V_{RMS}) TxD = 0	H2 (dB) TxD = 1	H2 (dB) TxD = 0
0.5	0.16	0.16	-65	-67
1	0.28	0.28	-66	-67
5	1.17	1.16	-73	-76
10	1.62	1.56	-75	-79
50	2.02	1.95	-74	-75
100	2.06	2.00	-73	-75

Channel 4 : 86kHz

Rline (Ω)	Output (V_{RMS}) TxD = 1	Output (V_{RMS}) TxD = 0	H2 (dB) TxD = 1	H2 (dB) TxD = 0
0.5	0.17	0.17	-56	-52
1	0.29	0.30	-60	-57
5	1.21	1.18	-77	-77
10	1.55	1.53	-82	-82
50	1.86	1.80	-82	-78
100	1.88	1.84	-80	-78

IV - POWERLINE INTERFACE (continued)

Summary of the test results :

Channel 1 :
R < 5Ω : 310-360mA$_{RMS}$
R > 5Ω : 1.3 - 2.1$_{VRMS}$
R 10/50Ω : H2 < -74dB
Channel 2 :
R < 5Ω : 280-320 mA$_{RMS}$
R > 5Ω : 1.2 - 2.2 V$_{RMS}$
R 10/50Ω : H2 < -75dB
Channel 3 :
R < 5Ω : 280-320mA$_{RMS}$
R > 5Ω : 1.2 - 2.0V$_{RMS}$
R 10/50Ω : H2 < -74dB
Channel 3 :
R < 5Ω : 290-340mA$_{RMS}$
R > 5Ω : 1.2 - 1.9V$_{RMS}$
R 10/50Ω : H2 < -78dB

With impedances < 5Ω the output current is for all the four channels in the range 280-360mA$_{RMS}$.

The output voltage on impedances > 5Ω is both on channel 3 and 4 in the range 1.2 - 2.0V$_{RMS}$. On channel 1 and 2 it's in the range 1.2 - 2.2V$_{RMS}$.

On all the channels the second harmonic of the signals is < -74dB, on channel 4 the second harmonic is even < -78dB.

IV.7.3 - Receive sensitivity

The receive sensitivity of the powerline interface is measured with a Bit Error Rate (B.E.R.) test. The Bit Error Rate is the amount of wrong bits in a received bit pattern. For example, if 2 out of 1000 received bits is wrong detected, the B.E.R. is 2/1000 = 2 E-3. If the B.E.R. with an input of 1mV$_{RMS}$ is worse than with an input of 5mV$_{RMS}$, the receive sensitivity is not 1mV$_{RMS}$ but 5mV$_{RMS}$ (or more).

Test configuration

In this test two ST7536 boards are used. Each board has a ST7536 + powerline interface.

One board is in transmit mode, the other in receive mode. A Bit Error Rate Analyzer is used to generate bit patterns, and to compare these patterns with the receive patterns. Because the ST7536 is a synchronous modem, both the received data (RxD) and transmitted data (TxD) are related to the clock signal generated by the ST7536. Therefore the clock signals of the boards are delivered to the analyzer (see Figure 19).

The output of the transmitting board is a Frequency Shift Keying (FSK) signal. This signal is added with the signal from a noise generator. This to observe the B.E.R. under different Signal/Noise-ratio conditions. In the adder the FSK signal is attenuated to a level of 0.5 - 5mV$_{RMS}$. The output signal is then send to the receiving board.
A spectrum analyzer is used to measure all the signals.

Measurements

Two tests are done on channel 3 (72kHz/1200 baud).

First B.E.R. test is made with a FSK input of 1mV$_{RMS}$ (= -60dBV). With the noise level set at -68....-74dBV. This gives a S/N ratio from 8....14dB.

A second test is done with a FSK input of 5mV$_{RMS}$ (= -46dBV). With the noise level set at -54...-60dBV. These values are set by adjusting the mixer, and measured with the spectrum analyzer.

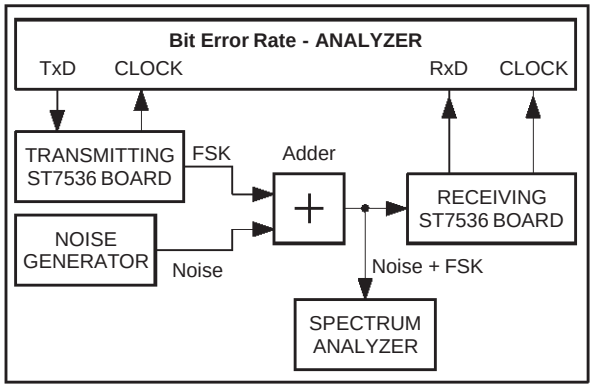
The spectrum analyzer measurements are made in a spectrum of 1200Hz. This is done because the FSK signal has two main frequencies on 1200Hz distance from each other. The noise signal is therefore measured in this band. In annexe B example plot are given from all the tests, with a S/N ratio of 10dB.

The B.E.R. is calculated from the number of errors counted by the B.E.R. analyzer.

Example : For instance the bit rate is 1200 baud. In 10 minutes the analyzer counted 800 errors. The measure time is then 10 x 60s is 600s. Each second 1200 bits are transfered, so in 600 seconds 720000 bits. Then the bit error rate is 800/720000 = 1.1 E-3.

→ B.E.R. = number of errors / (time in seconds x bit rate)

Figure 19



IV - POWERLINE INTERFACE (continued)

Test results (see ANNEXE A)

The results of the B.E.R. test are almost the same for both $1mV_{RMS}$ and $5mV_{RMS}$ (FSK signal level) input. Compared to B.E.R. test results of a stand alone ST7536, the results are even 1dB (S/N ratio) better. These results demonstrate that the receive sensitivity is at least $1mV_{RMS}$, and therefore the other channels are tested with an input of $1mV_{RMS}$.

Channel 1, 2 and 4 are tested with a FSK signal input of $1mV_{RMS}$. On those channels the results are also compared to B.E.R. test results of a stand alone ST7536. On channel 2 there is no difference between the B.E.R. of a stand alone ST7536 and a ST7536 + powerline interface. On channel 1 and 4 the B.E.R. is 0.5dB better than a stand alone ST7536.

Typical B.E.R. : (input FSK 1mV)

S/N (dB)	Channel 1	Channel 2	Channel 3	Channel 4
8	1.2E-2	1.2E-2	2.0E-2	1.0E-2
10	2.0E-3	2.0E-3	4.5E-3	1.2E-3
12	1.0E-4	1.0E-4	4.5E-4	1.0E-4
14	4.0E-6	4.0E-6	4.5E-5	3.0E-6

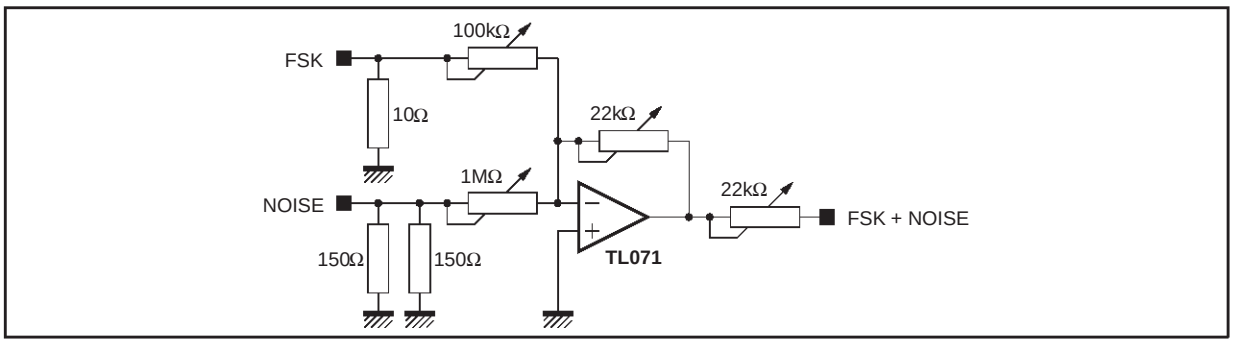
IV.7.4 - Conclusions

The B.E.R. tests confirm a receive sensitivity of $1mV_{RMS}$.
This is according to the specifications under which the powerline interface has to operate. Moreover, the B.E.R. tests showed that the powerline interface improved the performances of the ST7536 ; the results of a ST7536 in combination with the powerline interface are better than a stand alone ST7536.

Remark :
To test if these results are not only valid for a laboratory set up, both boards have been connected to the 220V powerline network. The distance between the two boards was 30 meter. After a measure period of 15 minutes, not even 1 error was detected !

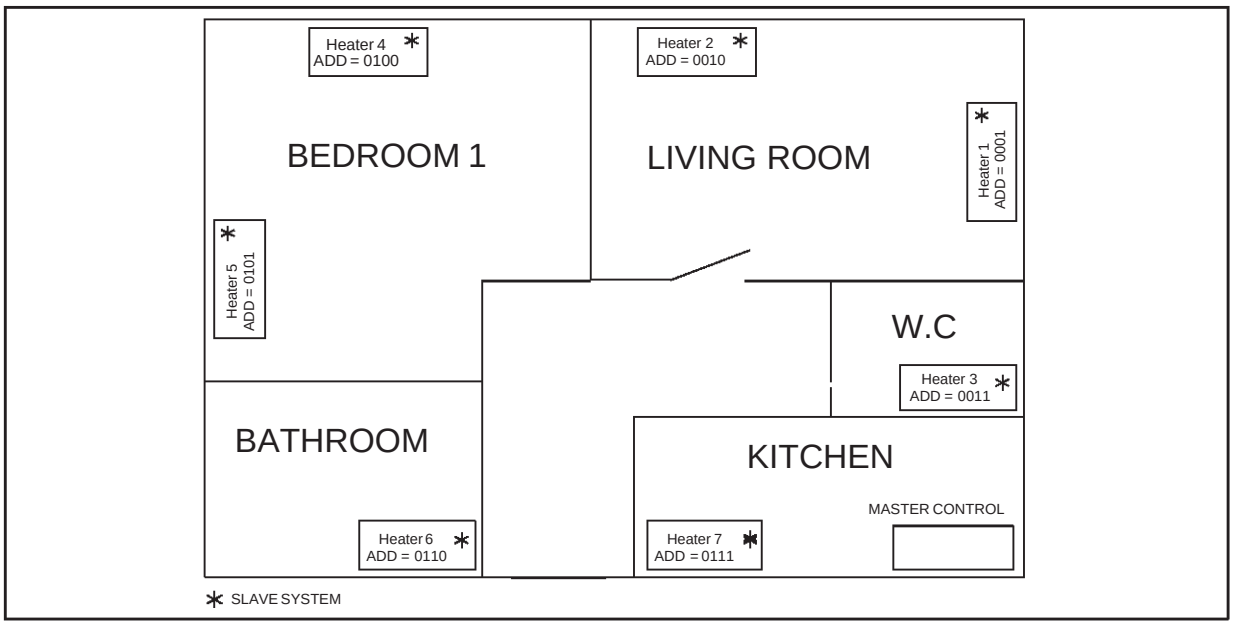
Test equipment : (see Figure 20)
Shlumberger SI 7703B B.E.R. analyzer
HP3562A Spectrum analyzer
Rohde & Schwarz SUF2 Noise generator
Mixer :

Figure 20



V - HEATING CONTROL APPLICATION

Figure 21



V.1 - Introduction

We will do a heating control system, using the ST7536 and a ST6 micro controller.

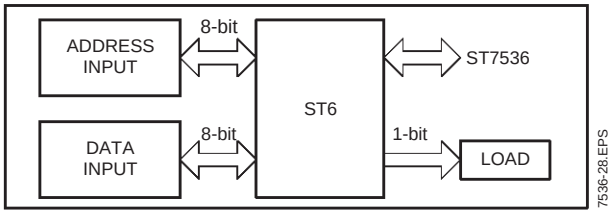
We have two boards (see Figure 21) :
- Master : control and set temperature in each room,
- Slave : temperature reading, switch-on/off of heater.

V.2 - Micro-controllers

Two different micro-controllers have been set up, one for the slave systems, and one for the master system. The main differences between the two controllers are the different input/output facilities.

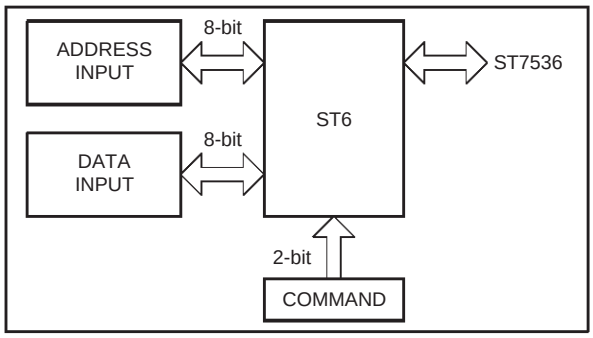
The slave version needs one 8-bit data input to initialize its own address, and one 8-bit input to read data from an external measure system. It should also provide an output that switches a load. This load will be simulated by a LED (see Figure 22).

Figure 22 : Slave Micro-controller



The master version will have its own address initialized in the software. Therefore no data input is needed for that. Data input (8-bit) is needed to read the destination (slave) address. To display data, an 8-bit data output has to be provided. Furthermore, it needs a 2-bit command input (see Figure 23).

Figure 23 : Master Micro-controller



Both the master and the slave version need also data exchange with the ST7536 ; the clock, transmit data, receive data, reset and Rx/Tx control lines.

V.3 - Hardware

As a micro-controller the ST6 has been chosen. This controller provides 20 data input/output pins, a reset and a non maskable interrupt input. Only a few external components have to be added to this micro-controller for full operation. The used ST6 is a 2Kbyte program memory EPROM version ; the ST62E15. The ST6 has an internal oscillator circuit. One machine cycle takes 13 oscillator pulses. This means that with a clock frequency of 8MHz a machine cycle takes 1.625µs. Most of the instructions (load instructions, bit manipulations) take 4 machine cycles. The maximum bitrate the ST6 has to serve is 1200 baud. One bit has a lenght of 833ms, which is equal to 512 machine cycles. This means that during each bit about 130 instructions can be executed.

V - HEATING CONTROL APPLICATION (continued)

The ST6 has an on chip watchdog circuit. There are two different versions of the ST62E15. On one there is a software selectable watchdog, and on the other (the hardware version) this watchdog is allways activated. The version that is used for these micro-controllers is the hardware version.

V.4 - Slave

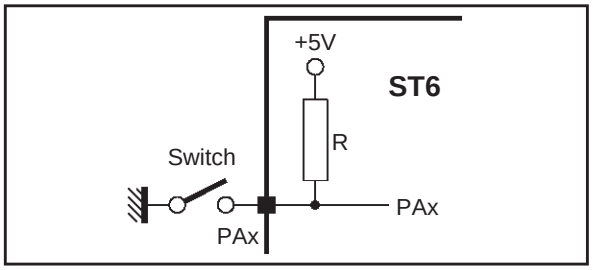
This micro-controller is in fact just an ST6 with a very few external components. A few switches, resistors, capacitors, a crystal and a 74LS04 are connected to have a complete controller. Each of these components is used to set the ST6 in the correct configuration.

Pin Configuration Slave Controller

For each pin a short discription is given, such as the configuration chosen for this microcontroller.

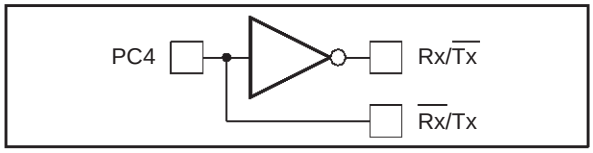
- **pin 27..20 (PA0..PA7) :** Input/output port A.
  Port A of the ST6 is used for reading the (8-bit) home address of the slave system. Switches are used to set each bit. The ST6 provides an internal pull-up resistor which will cause an "1". Closing a switch (to 0V) will cause a "0".

Figure 24



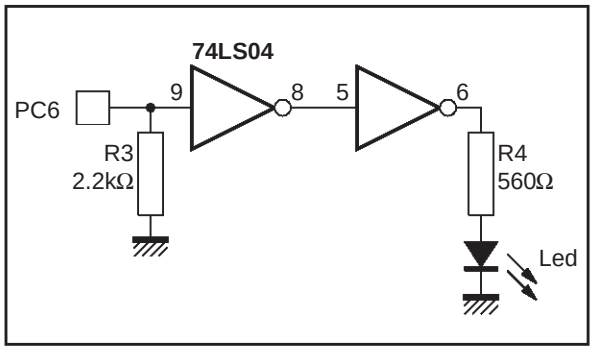
- **pin 19..12 (PB0..PB7) :** Input/output port B.
  Port B of the ST6 is used to read (8-bit) data from an external measure system. This system is simulated by switches. The same as for port A, the ST6 provides an internal pull-up resistor which will cause an "1". Closing a switch (to 0V) will cause a "0".
- **pin 9 (PC4) :** Port C bit4.
  This output is used as the Rx/$\overline{Tx}$ control. Transmit mode of the ST7536 and the powerline interface is selected if this output is "1". Receive mode is selected with an "0".
- **pin 8 (PC5) :** Port C bit5.
  This pin is used as the transmit data (TxD) output to the ST7536.

Figure 25



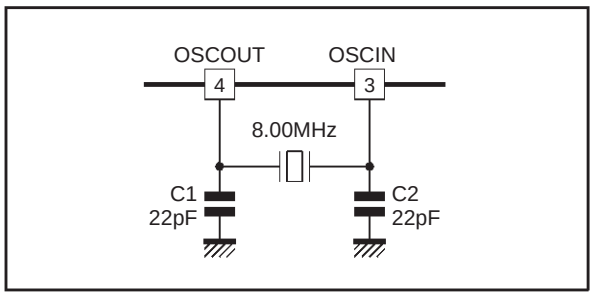
- **pin 6 (PC7) :** Port C bit7.
  This pin is used as the receive data input (RxD) from the ST7536.
- **pin 7 (PC6) :** Port C bit6.
  This is the load switching output. The load is simulated by a LED. Two inverters are used as a buffer between the ST6 and the LED. Because the ST6 outputs are in high impedance during a reset, a pull down resistor (R3/2k2) is used to avoid the load switching on.

Figure 26



- **pin 4 (OSCOUT) :** Oscillator output.
- **pin 3 (OSCIN) :** Oscillator input.
  Between these pins a 8.00MHz crystal has to be connected. If the internal oscillator of the ST6 runs at 8MHz, one machine cycle is 1.625µs. This speed is needed to be able to serve the 1200 baud bitrate from the ST7536.

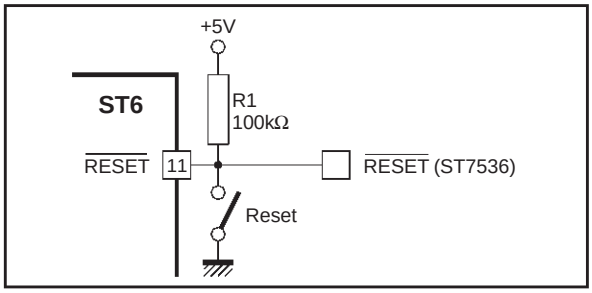
Figure 27



V - HEATING CONTROL APPLICATION (continued)

- **pin 5 (NMI) :** Non maskable interrupt.
  The NMI is used as input of the (inverted) clock of the ST7536. The NMI is falling edge sensitive. An external pull-up resistor (R2/100k) is added to provide +5V for debugging the controller without the 74LS04 (the inverter).
- **pin 11 (RESET) :** Reset input.
  The reset of the ST6 is active low. To restart the microcontroller at the beginning of its program, this pin should be set to 0V by closing the switch. For normal operation the +5V is provided by a pull-up resistor (R1/100k).

Figure 28



- **pin 2 (TIMER) :** Timer output, not used.
- **pin 10 (TEST) :** Test input.
  The test pin is used to set the ST6 in a special operation mode. For normal operation this pin is set at 0V.
- **pin 1 (V_{DD}) :** Power supply, +5V.
- **pin 28 (V_{SS}) :** Ground, 0V.

V.5 - Master

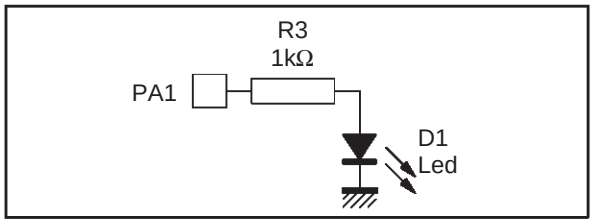
The main difference between the master and the slave version of the microcontroller is the fact that the master needs one extra input/output pin. The slave version has 1 output to control a load, where the master needs 2 inputs to read a command. Therefore one input/output (PC5) has been multiplexed, it serves both the RxD and TxD lines to the ST7536.

Pin Configuration Master Controller

The pin configuration of the master differs from the slave on the next pins :

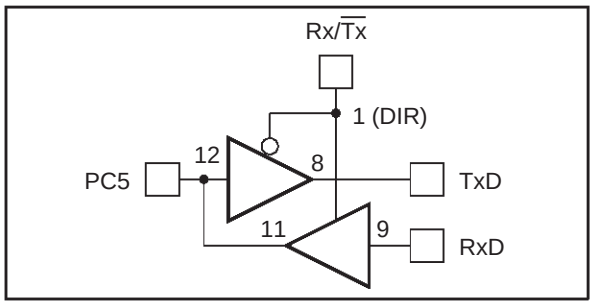
- **pin 27..20 (PA0..PA7) :** Port A.
  The master uses port A to display data. Light Emitting Diodes (LED's) are used to do this. The maximum current that can be taken from each pin is 5mA. Therefore the serial resistor has a value of 1kΩ (current = U/R = 5-0.6/1k = 4.4mA).

Figure 29



- **pin 19..12 (PB0..PB7) :** Port B.
  The hardware configuration of these pins is the same as on the slave, but on the master these pins are used to read a (destination) address.
- **pin 7/6 (PC6/7) :** Port C bit6/bit7.
  On the master these pins are used to read a command (see also the software discription). The hardware configuration is the same as for port B.
- **pin 9 (PC5) :** Port C bit5.
  The slave uses PC7 as received data input (RxD). Because the master already uses this pin for reading a command, PC5 has to be multiplexed. This is done with an 74LS245. It is a (8-bit) bus receiver/transceiver. The Rx/$\overline{Tx}$ line is used to select whether the RxD should be send to PC5, or the data from PC5 to the TxD (that's the opposite direction).

Figure 30



V - HEATING CONTROL APPLICATION (continued)

V.6 - Software

The software that has been developed for the micro-controllers has to be regarded as an introduction to more complex communication protocols. Therefore a very simple but effective protocol has been set up. With this protocol it should be possible to evaluate the performances and possible applications of a ST7536 system.

V.7 - Protocol

The protocol has been set up in such a way that all kind of features can be added easily. A simple but powerfull frame format is used. It gives the possibility to use error correction and detection.

Each frame consists of a preamble, a system address, a destination address, a control block and a data block. The preamble and the system address length is 2 bytes, the destination address, the control block and the data block are 3 bytes long.

The preamble is used to train both the transmitting and receiving ST7536. It consists of two 8-bit patterns (10101010). The receiving ST7536 needs it to train its clock recovering. Because the 3 first bits transmitted by an ST7536 are not guaranteed to be correct, the preamble is also used to overcome unreliable data in the beginning of a transmission. This because the preamble doesn't contain data.

The system address is used to be able to have more than one ST7536 system operating on a certain powerline network. For example a remote metering system and a traffic light control system. It is also used to avoid interference with other (no ST7536) systems. The lenght of the address is only 8 bits, and therefore it's send twice, to avoid unwanted activation of a group that has not been called.

The lenght of the preamble and system address together is 4 bytes (32 bits) (see Figure 31)

The preamble and the system address inside the frame (see Figure 32).

The received destination address, control block and data block should be very reliable, and therefore an error correction is done. To be able to do this all these data is send 3 times. The destination address has a lenght of 1 byte (8 bits), which is send 3 times: in block 1, block 2, and block 3. This is the same for the control byte and the data byte. As an example the destination address inside the frame (see Figure 33).

So all the blocks (block 1/2/3) contain the same byte. The error correction uses them to extract the correct byte out of the 3 that have been received.

The destination address is used to select 1 user (slave) in a system group. All the slaves in a system have their own 'home' address. To activate a slave, it has to recognize the received destination address inside a frame as its own 'home' address.

In this simple protocol there is only communication between a master and the slaves. Therefore the destination address is transmitted by each slave is the master address. In the frame which transmitted by the master, the destination address is the home address of the slave that is called.

The control byte can be used for all kind of information about the frame. In this protocol the control block is only used to say if the frame is a command or a response. This is done with bit 7. If this bit is set it means that the data byte contains a command (from the master to the slave), and the data byte will contain the command. If this bit is reset it means that the frame is a response (from the slave to the master), and the data byte will contain the requested data.

Control Byte	Status	Data Byte
10000000	command	command
00000000	response	requested data

In the control byte only bit 7 is used. Bit 0...6 are reset. They can be used to add severall features to the protocol.

Error detection and correction

A possible feature that can be added is error detection. In the protocol this feature is not available. This because, to be really usefull, error detection would require the possibility to send a message from the receiver to the transmitter, indicating that an error has been detected. It will need a more detailed protocol, which uses the free bits in the control byte. The intention of this protocol was to be very simple and clear. Therefore the error detection is not provided. Although there is no error detection, the protocol provides an error correction. It would be very unrealistic to assume that all the bits in a received frame are correct. Therefore the most important parts of the frame (destination address, control byte and data byte) are protected with an error correction.

The error correction is done with bit-overlay. This is a very powerfull method to correct bytes that are transmitted over very noise lines. Each byte is transmitted (and received) 3 times. The software uses the 3 received bytes to extract the (probably) correct byte. This is done by performing a bitwise majority decision on all the received blocks.

V - HEATING CONTROL APPLICATION (continued)

Figure 31

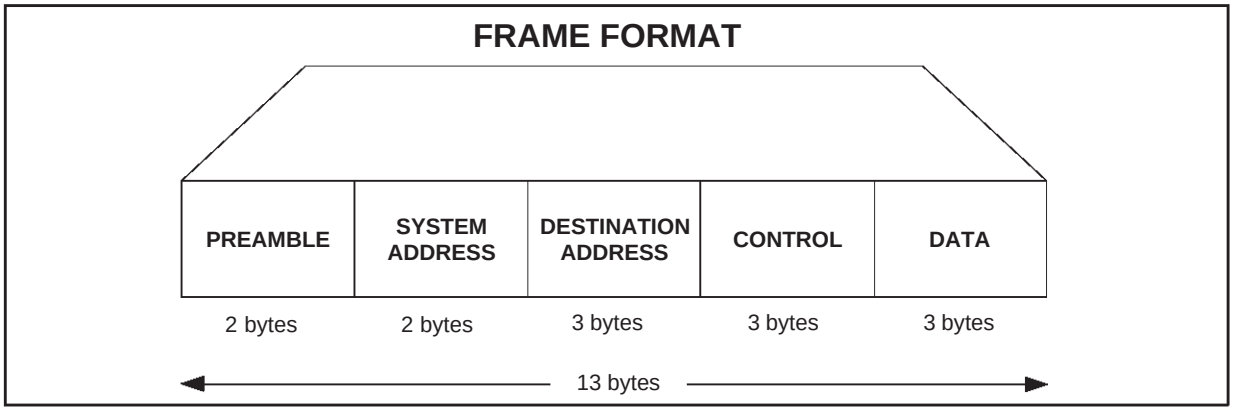


Figure 32

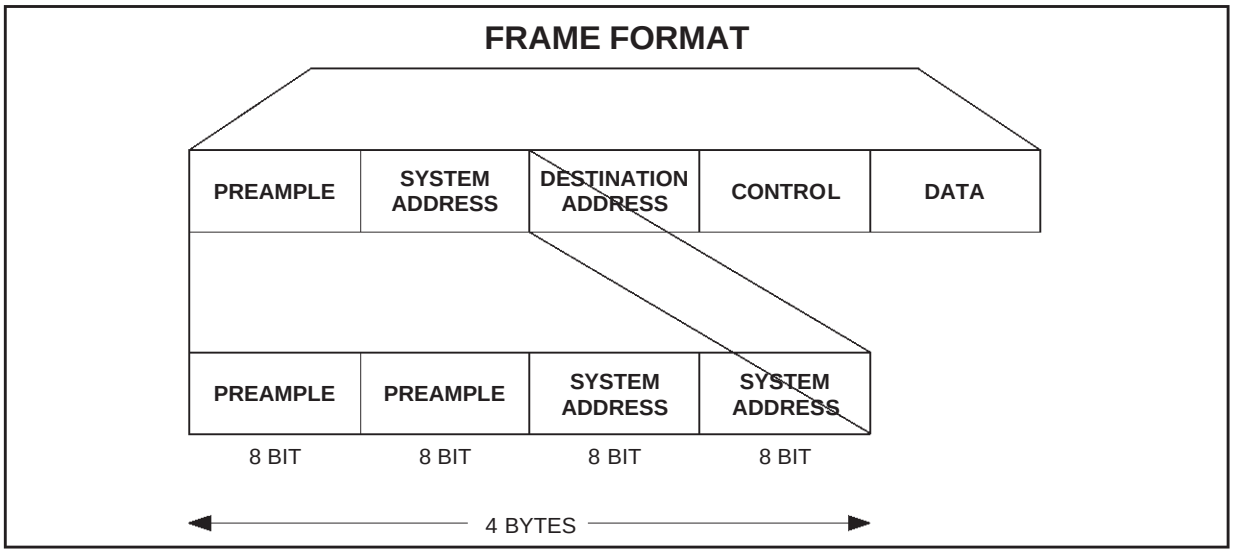
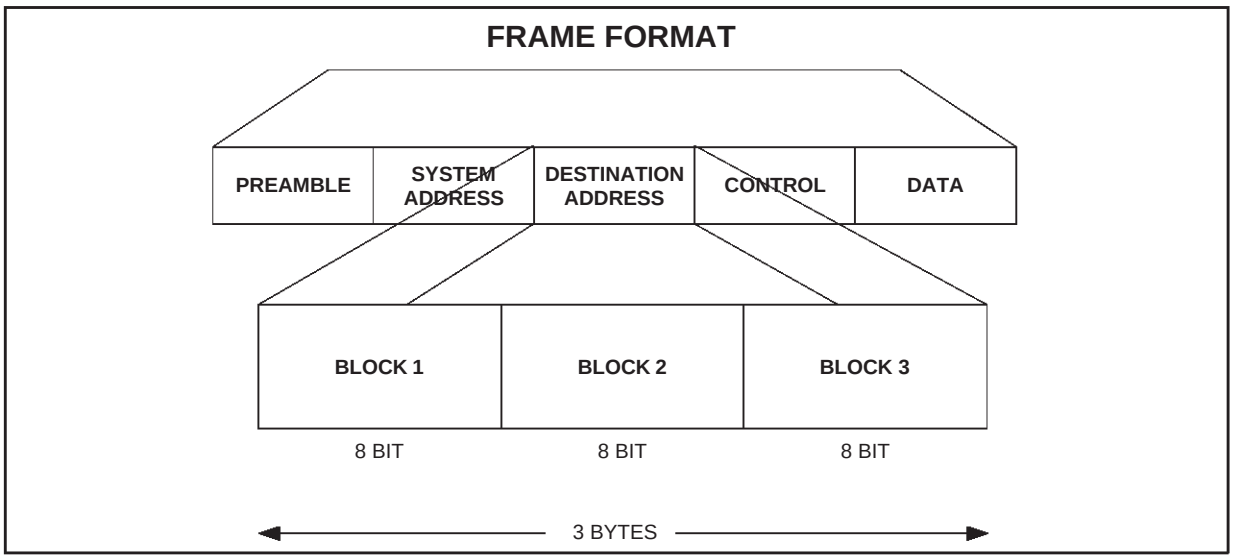


Figure 33



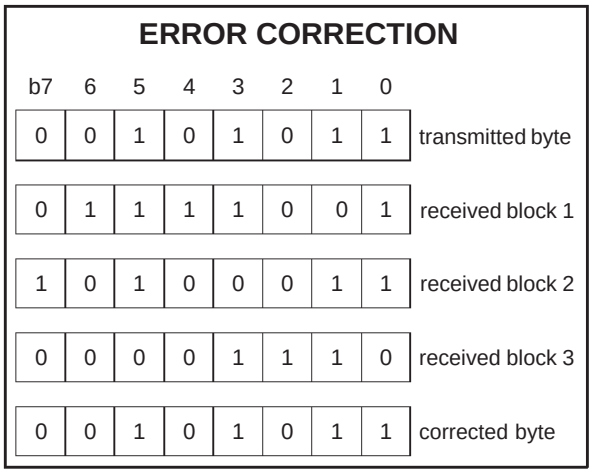
V - HEATING CONTROL APPLICATION (continued)

Even if all the 3 received blocks contain errors, it's still possible to extract the correct byte out of these blocks.
Example : The first received block contains 3 errors (b6/b4 and b1), the second block contains 2 errors (b7 and b3) and the third block contains 3 errors (b5/b2 and b0) (see Figure 34).

The error corrector will take bitwise a decision what is probably the correct bit. If two out of three bits are "1", the resulting bit will be "1". If two out of three bits are "0", the resulting bit will be "0".

This system can correct 1 error out of 3 bits. If more blocks are send, let's say 9, it would be possible to correct 4 out of 9 bits. This is a very interesting method to overcome problems on very noisy powerlines.

Figure 34



V.8 - Application software

The protocol has been designed to demonstrate typical applications of the ST7536.

All the slaves have been programmed with one program. With this program it is possible to set a load (simulated by a LED) on or off. This load can be for example (depending on the application) a traffic light. With this program it's also possible to read data (simulated by 8 switches) from an external measure system, and send this data to the master if requested. The measure system, for example, can be reading an electricity meter. Remote reading these meters, can save the costs for manual reading (such a system is allready operational in Italy). So there has been written 1 program for the slaves, that can simulate different applications.

Each typical application should be programmed in the master. It gives the possibilty to demonstrate different applications without reprogramming all the slaves.

One application program has been developed for the master.It demonstrates the good functioning of the system : a remote heater control. With this application it's possible to control in a building in each room the heater (which is equipped with an ST7536). The LED on the slave simulates in this case the heater. With the master each heater can be set manual on or off, and even more, the master can regulate automatically the heater, by reading out the room temperature. This temperature is simulated with the 8 switches on the slave.
The master has 4 different commands :

1:(00)	manual off	00000000	heater on
2:(01)	manual on Temperature :	00001111	
3:(10)	not used	00010000	
4:(11)	automatic control →	11111111	heater off

V.8.1 - ST6 programs

The programs for both the master and the slave have been written in assembly language. An assembler is used to create the executable code. A special ST6 kit is used to debug the programs. The EPROMs are also programmed with this kit. The program memory size of the ST62E15 is 2K byte. The slave program is 1.6K byte, the application program for the master 1.8K byte long.

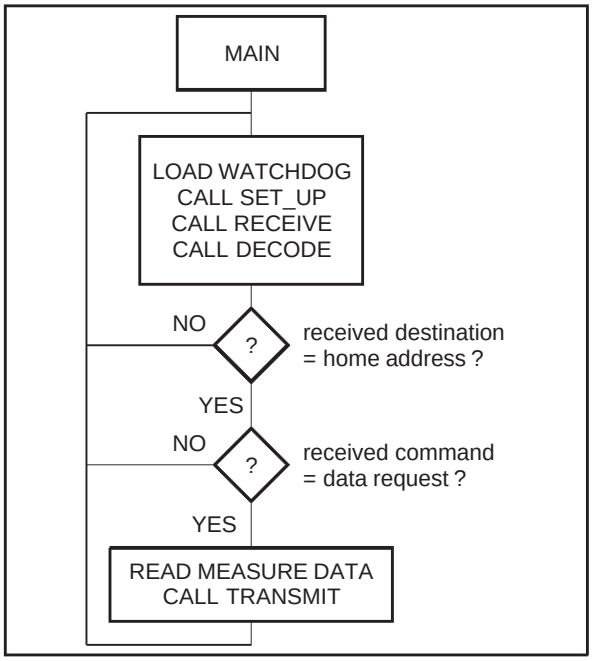
Some subroutines are used in both the master and the slave program, like the transmit/receive subroutines and the error decoding.

From both programs the most important subroutines are described on the next pages. The flow charts that are used do not give a detailed representation of the subroutines, but are used to explain the structure of the subroutine.

V - HEATING CONTROL APPLICATION (continued)

V.8.1.1 - Slave program

Figure 35



In the main program first of all the watchdog is (re)loaded. The watchdog is a down-counter that generates a reset when it's not in time reloaded. It provides a recovery from a software upset.

Then the home address is read from the switches in the set-up routine. The slave will go in receive mode and be maintened until a complete frame is received.

After that the contents of this frame is decoded. In the decode subroutine the bytes are corrected and depending on the received command the led is set on or off.

If the received destination address was the slaves home address and the received command was a data request the (simulated) measure data is read and then transmitted to the master.

Receive Subroutine

The receive subroutine is used to read a frame. It ignores all the RxD until the system address is received. When it is received for the second time, the next bytes of the frame are read and stored. To read the RxD this subroutine uses the read_bit subroutine which is described on Figure 36.

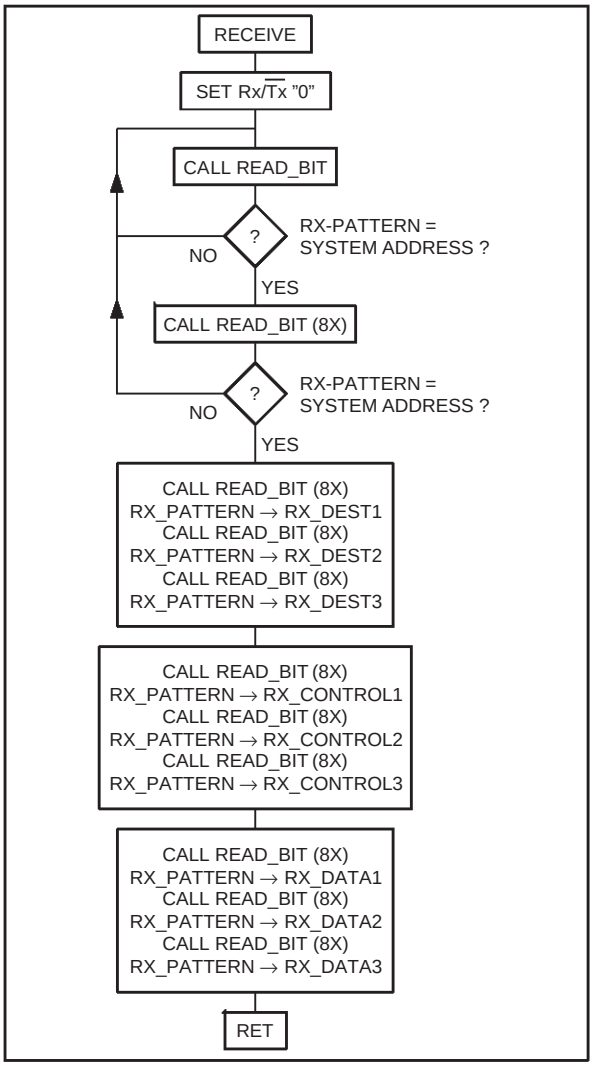
First of all the Rx/$\overline{Tx}$ line is reset. The ST7536 and the powerline interface will then be in receive mode. Then the read_bit subroutine is called, which will add the next received bit to the Rx_pattern. As long as the system address is not received, the programs continue read the RxD.

When the system address is received, the next 8 bits will be loaded using the read_bit subroutine, and after that the Rx_pattern should contain again the system address. If this is not the case this procedure starts again. Else the next bytes will be read and stored.

Flrst the 3 destlnatlon addresses. The read_bit subroutine is called 8 times and the Rx_pattern will then contain the next byte (Rx_dest1) which is stored. The next 2 bytes (Rx_dest2, Rx_dest3) are read in the same way.

When the destination addresses are received the control bytes and the data bytes are received and stored in the same way.

Figure 36

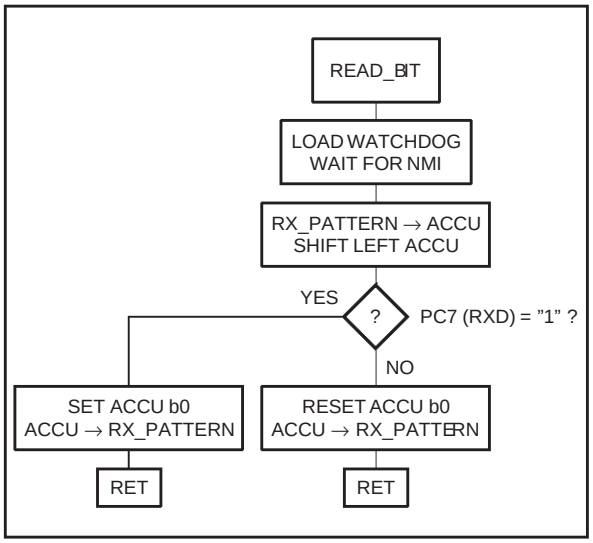


V - HEATING CONTROL APPLICATION (continued)

Read-bit Routine

This routine is used to read the RxD is presented on PC7 (for the master on PC5). The ST7536 delivers valid data on the positive edge of its clock. The inverted clock is used as the NMI input of the ST6. This NMI is falling edge sensitive - > an NMI will be generated on the positive edge of the ST7536 clock. This means that the RxD should be read immediately after a NMI interrupt. The received bit is then added to the (Rx_)pattern.

Figure 37



First of all the watchdog is reloaded.

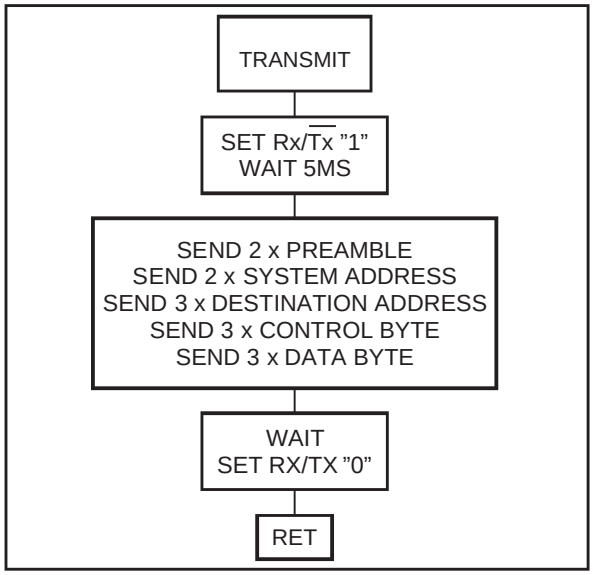
Then the ST6 will wait for the NMI (interrupt). The Rx_pattern is loaded into the accumulator and then shifted left. If the received data bit is a "1" the next bit (b0 in the accumulator) is set to "1". If the received bit is a "0", this bit will be set to "0".

At the end the new pattern is stored.

Transmit Subroutine

This subroutine uses the send 8-bit subroutine to send a 8-bit pattern. This subroutine is described on Figure 38.

Figure 38



In the transmit subroutine first off all the Rx/$\overline{Tx}$ line is set "1". The ST7536 and the powerline interface are then in transmit mode. Typical carrier stabilisation time of the ST7536 is 5ms. Therefore the program waits this time before sending all the bytes.

First the preamble (10101010) is send 2 times and then the system address. The destination address, the control byte and the data byte are send 3 time. This is done with the send 8-bit subroutine.

Send 8bit pattern subroutine

The ST7536 samples the TxD on the positive edge of the clock. The inverted clock is used as the NMI input of the ST6. On the positive edge of the clock (CLR/T) an NMI interrupt occurs. The software waits then 304 machine cycles before changing the TxD. When the TxD is changed it waits for the next NMI and again 304 cycles before storing the next TxD on PC5. Using these delays it is possible to present the ST7536 valid TxD on the positive edge of its clock. Both 600 (channel 1/2) and 1200 (channel 3/4) baud bitrates can be handled this way.

V - HEATING CONTROL APPLICATION (continued)

Figure 39

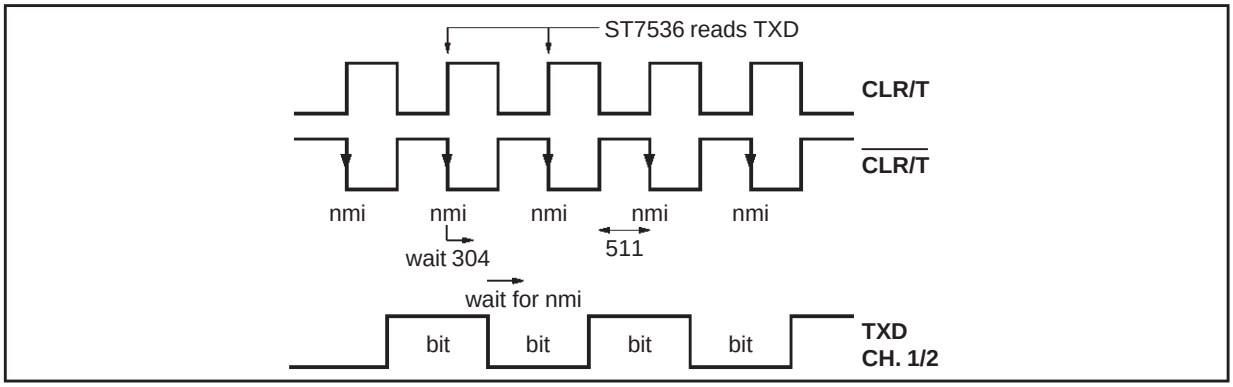


Figure 40

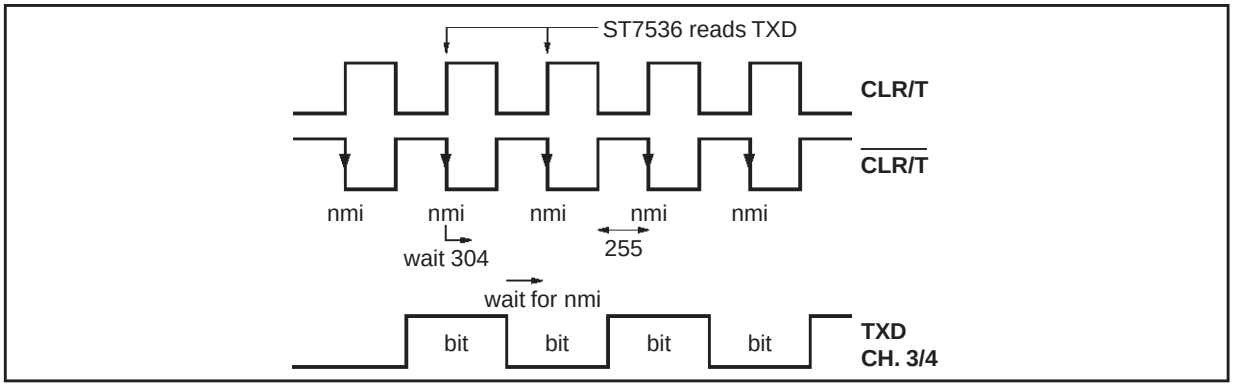
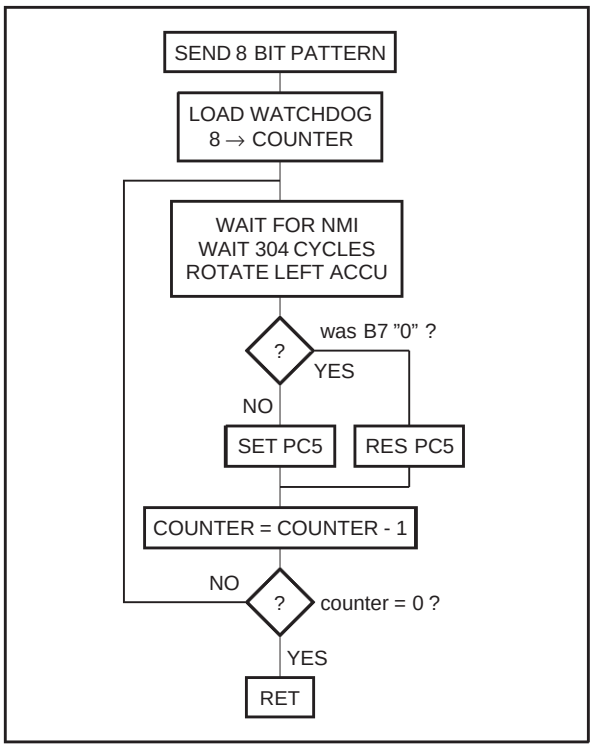


Figure 41



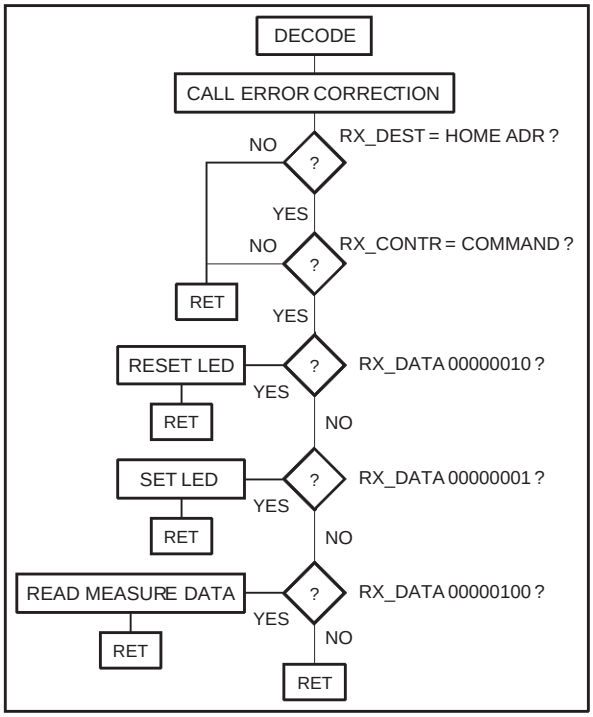
In the subroutine the watchdog is (re)loaded. Then the counter is set at 8. The ST6 waits for the NMI and then 304 cycles. The accumulator contains the pattern that has to be transmitted. This pattern is shift left; the carry bit will contain b7, b7 will contain b6 etc. If b7 was a "0" PC5 (the TxD output of the ST6) is reset, if it was a '1' PC5 is set. Bit7 is then transmitted. The counter is then decreased by 1, the software waits the same time, and the accumulator is shift left again. The carry bit will then contain b6 of the pattern that should be transmitted. The same as before, this bit is transferred to the TxD output.
This is also done with b5..b0. If b0 is transferred(transmitted) the counter will be 0. And then the ST6 will jump out of the subroutine.

Decode Subroutine

When a frame is received the main program jumps to this subroutine. In this subroutine first of all the error correction is called. After the correction, described below, the subroutine checks if the destination address of the frame was the home address of the slave. In this case, and then the control byte indicates a command in the data byte, the subroutine decodes the data byte. Then there is a jump out of the subroutine (see Figure 42).

V - HEATING CONTROL APPLICATION (continued)

Figure 42



Three commands are used in this program :

1: data = 0000 0001 → LED off.
2: data = 0000 0010 → LED on.
3: data = 0000 0100 → data request.

Depending on the received data byte the led will be set on or off, or in case of a data request, the ST6 reads the data on the system.

Error correction subroutine

In this subroutine the bits of the 3 received bytes are compared. The resulting should be set (”1”) if at least 2 out of 3 received bit are set. If 2 or more received bits are reset, the resulting bit should be reset (”0”). All the bits of the bytes are tested this way. This is done bit by bit (bit x), using the same procedure (see Figure 43).

V.8.1.2 - Master program

For the master one application program is set up. It presents the ST7536 in a central heating control. The receive, transmit and error correction subroutines are almost the same as described for the slave program. The master has a 2 bit command input (PC6/PC7).

After reading the command it is checked if it’s a new command or an old command. The program continues if a new command is read (from the switches).

Then this command is decoded :

PC6/7: 00 → heater off
PC6/7: 01 → heater on
PC6/7: 10 → not used
PC6/7: 11 → automatic control

The program will jump to the subroutine corresponding to the command that is decoded; the automatic, manual on or manual off subroutine (see Figure 44).

Figure 43

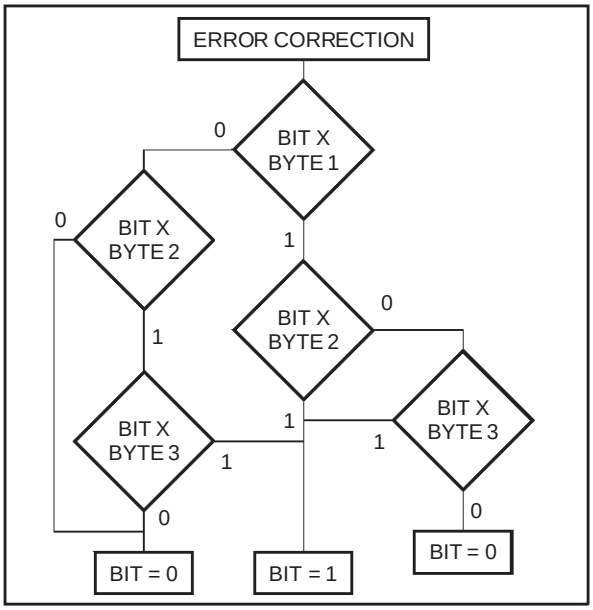
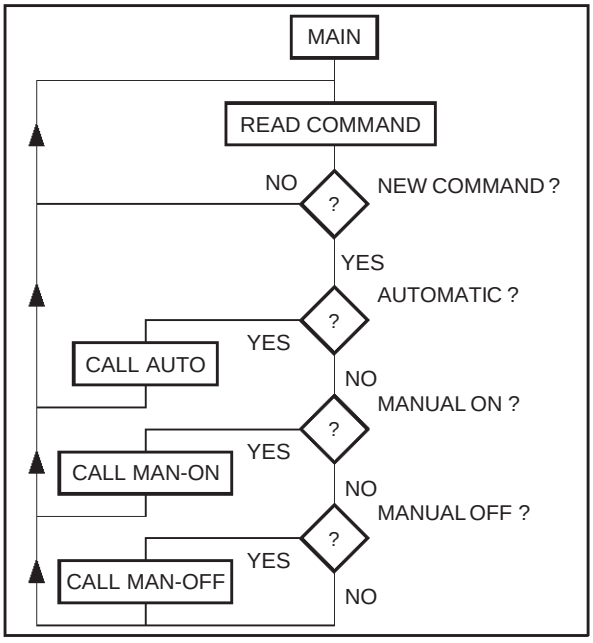


Figure 44



V - HEATING CONTROL APPLICATION (continued)

Automatic control subroutine

In this subroutine the master compares the receive data (temperature) from the slave to the reference value (00001 1 1 1). If the data < reference the heater is set on, else the heater is set off.

First the master sends a datarequest command to the slave. Then it goes in receive mode, to wait for the response of the slave. The received frame is then corrected, and the received destination address and control byte are checked. If the control byte indicates a response the received data is compared to the reference value (00001111). If the received data < the reference, a heater on command will be transmitted, else a heater off command. After that the command input is checked to be still an automatic control command. In this case, the master will continue with controlling the heater (see Figure 45).

Manual on/off subroutines

Although these routines are very simple, their functions are given in the flow charts below, to have a complete overview of the application program. The manual on subroutine sends a frame containing a heater on command, the manual off routine a frame containing a heater off command (see Figure 46).

V.8.1.3 - Evaluation of the software

The used protocol seems to be rather effective and functional. The system has been tested on very noise powerline networks, and no (software) problems occured. The ST6 programs have been written and tested step by step. When the programs were operating according to the protocol they have not been 're-written'. Therefore the programs might not be as well structured as possible. For final application software, it might be usefull to evaluate the programs, and then rewrite some subroutines. The program size may be decrease, and a 'clean up' will make the programs easier to understand.

Figure 45

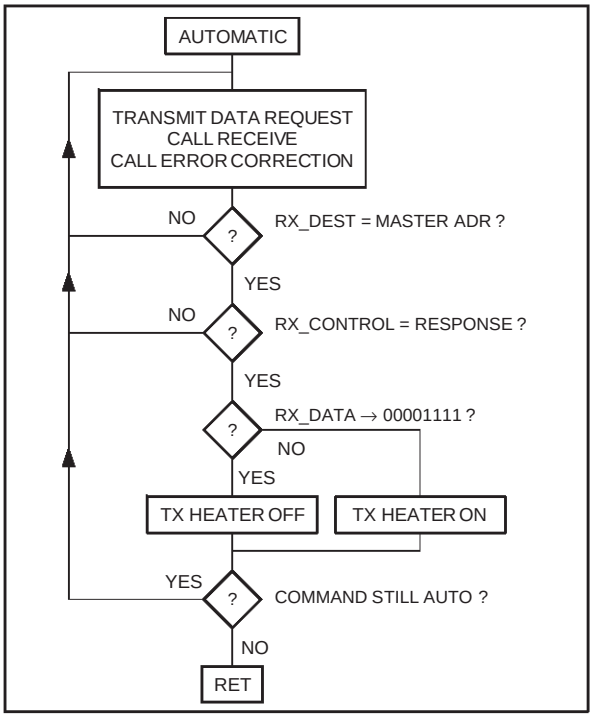
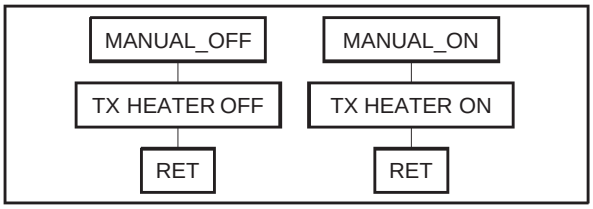


Figure 46



ANNEXE A

Figure 47 : B.E.R. ST7536 Application Board Comparison of channel 1/2/3/4 T = 25°C, Line Input = 1mV

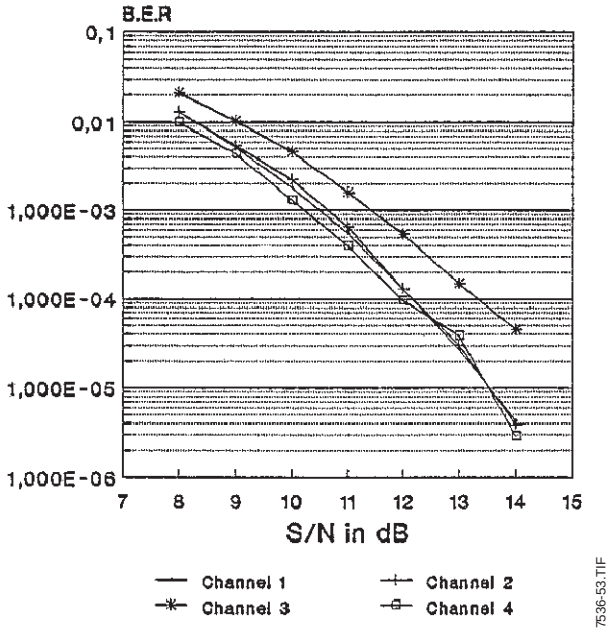


Figure 48 : B.E.R. Channel 3 (72kHz.) ST7536 board input 1mV & 5mV versus stand alone ST7536 RAI input 3mV

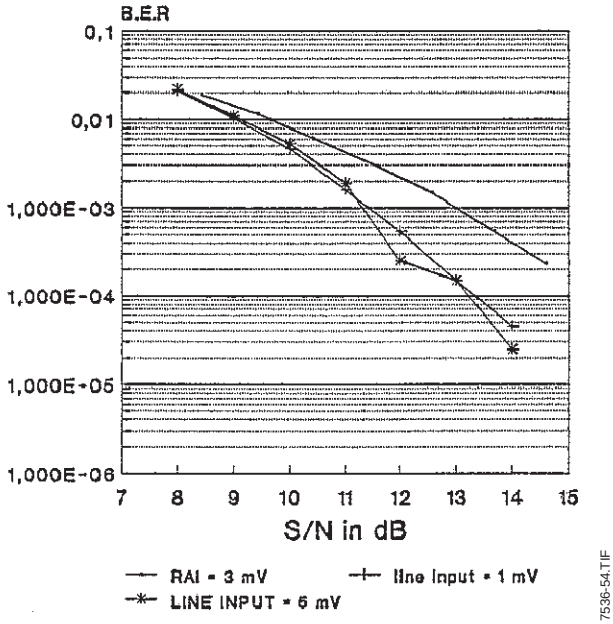


Figure 49 : B.E.R. comparison - ST7536 board versus stand alone ST7536 T = 25°C, Channel 1 (82kHz)

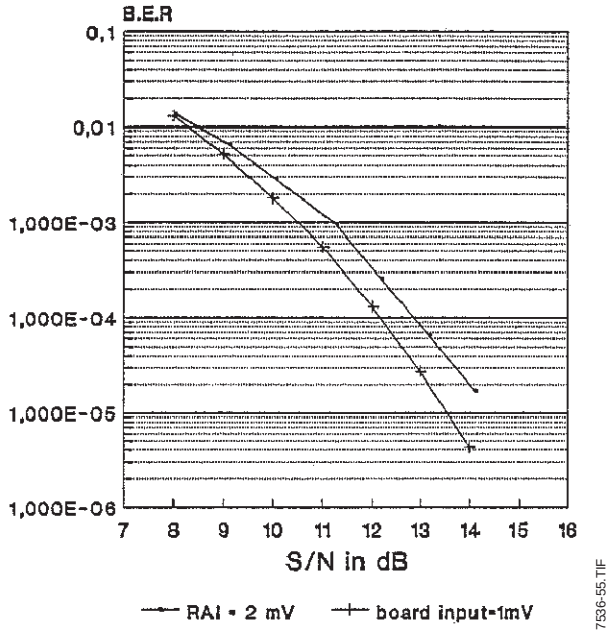


Figure 50 : B.E.R. comparison - ST7536 board versus stand alone ST7536 T = 25°C, Channel 2 (67kHz)

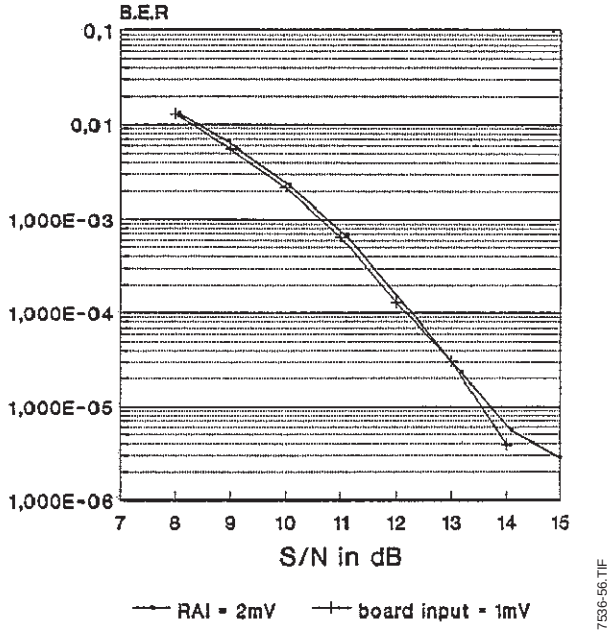


Figure 51 : B.E.R. comparison - ST7536 board versus stand alone ST7536
T = 25°C, Channel 3 (72kHz)

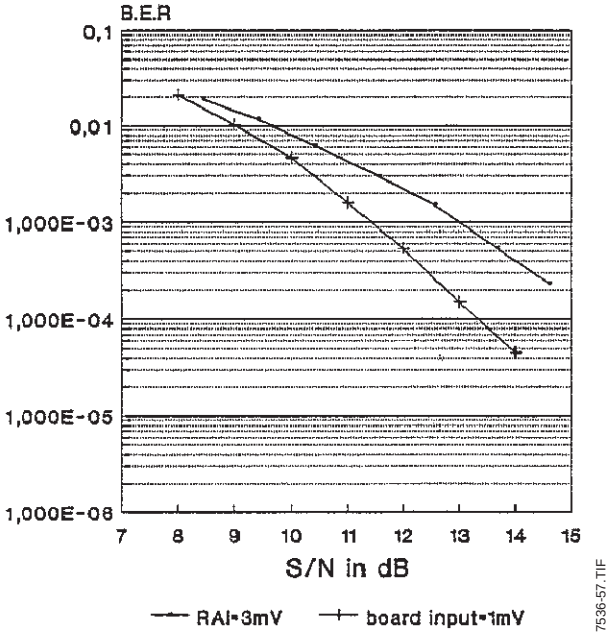
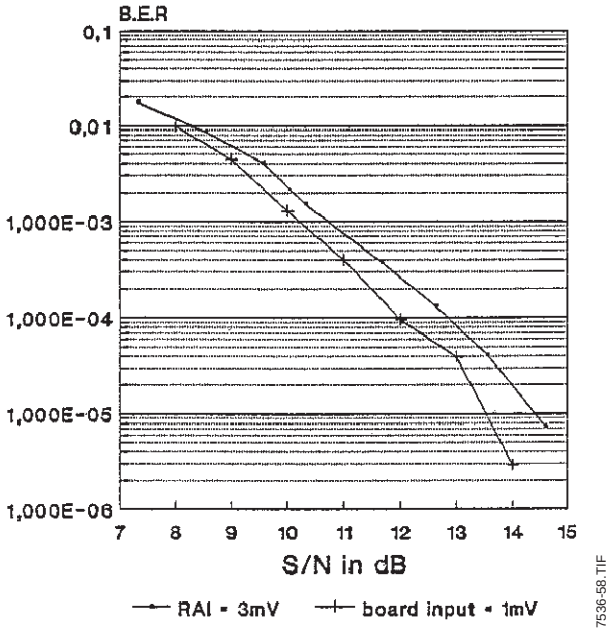
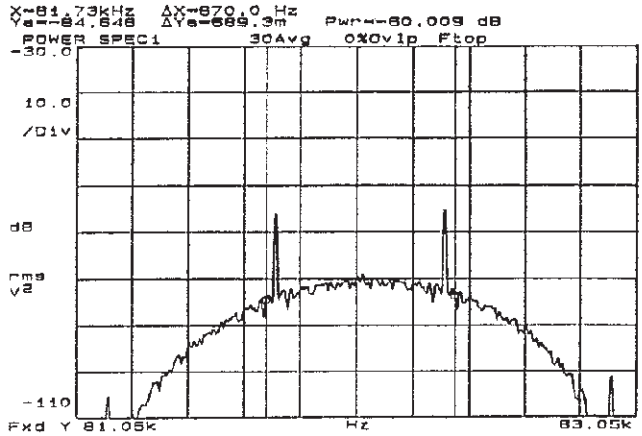


Figure 52 : B.E.R. comparison - ST7536 board versus stand alone ST7536
T = 25°C, Channel 4 (86kHz)



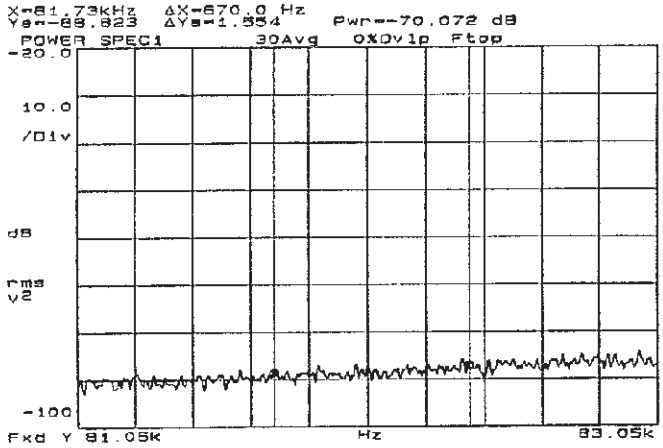
ANNEXE B : B.E.R. ST7536 APPLICATION BOARD (Signal/Noise frequency spectra)

Figure 53 : Channel 1 (82kHz) - S/N = -10dB, Input 1mV = -60dB
FSK (-60dB) - 1mV



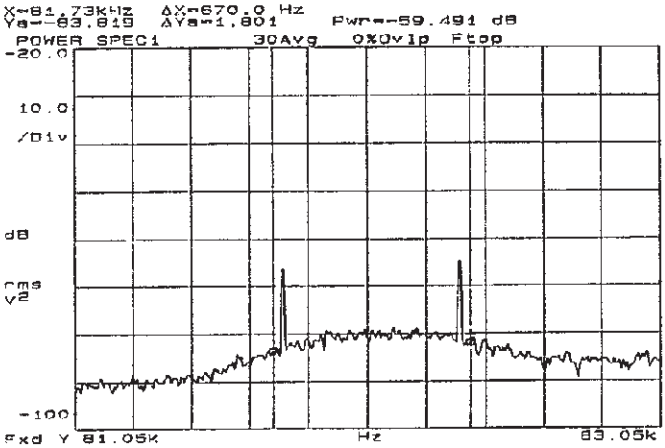
7536-59.TIF

Figure 54 : Channel 1 (82kHz) - S/N = -10dB, Input 1mV = -60dB
Noise (-70dB)



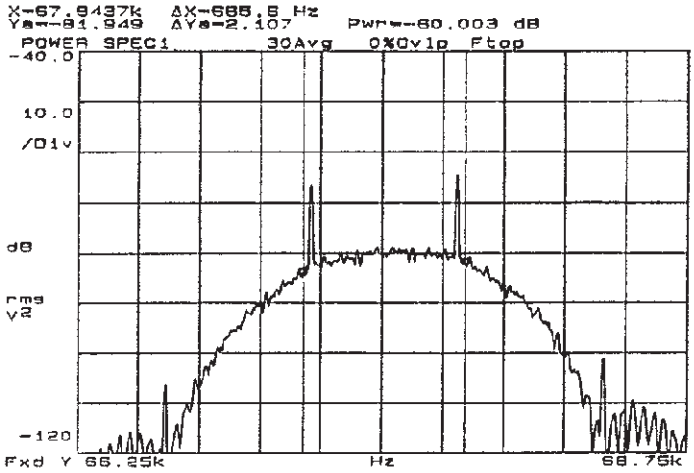
7536-60.TIF

Figure 55 : Channel 1 (82kHz) - S/N = -10dB, Input 1mV = -60dB
FSK + Noise



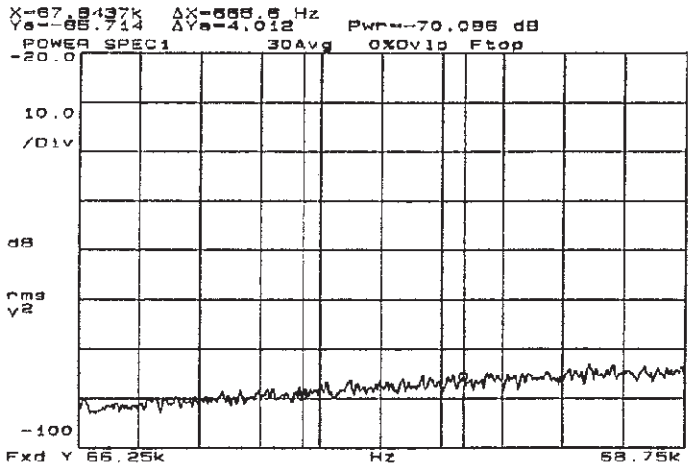
7536-61.TIF

Figure 56 : Channel 2 (67kHz) - S/N = -10dB, Input 1mV = -60dB
FSK (-60dB) - 1mV



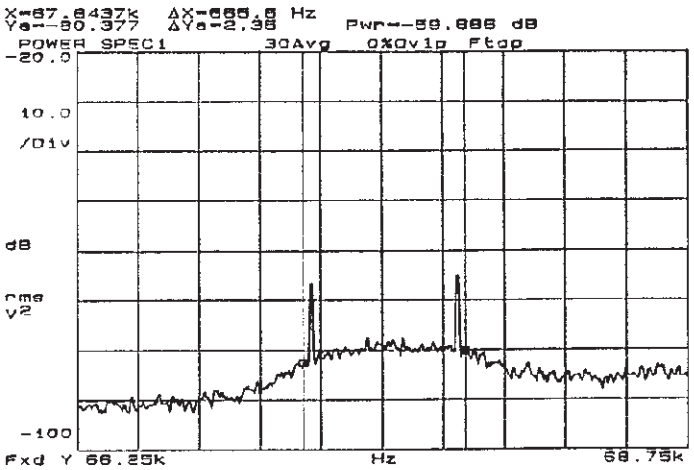
7536-62.TIF

Figure 57 : Channel 2 (67kHz) - S/N = -10dB, Input 1mV = -60dB
Noise (-70dB)



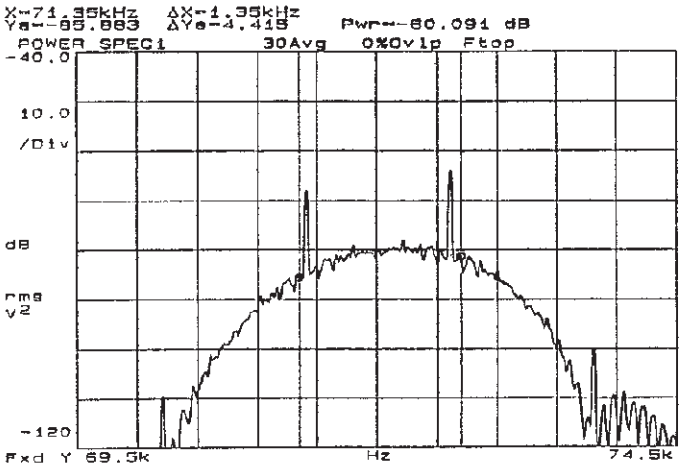
7536-63.TIF

Figure 58 : Channel 2 (67kHz) - S/N = -10dB, Input 1mV = -60dB
FSK + Noise



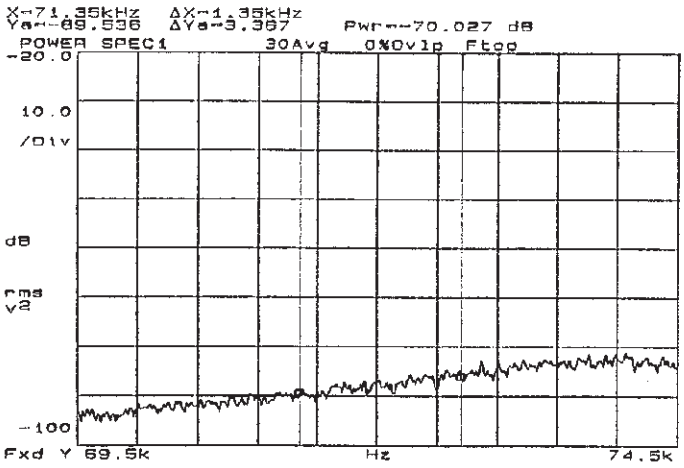
7536-64.TIF

Figure 59 : Channel 3 (72kHz) - S/N = -10dB, Input 1mV = -60dB
FSK (-60dB) - 1mV



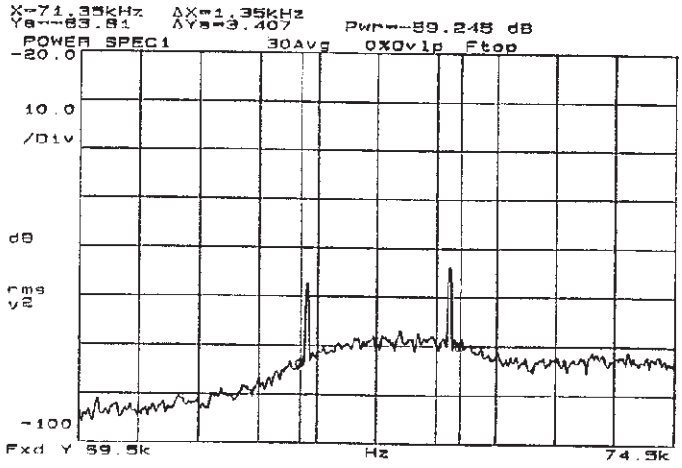
7536-65.TIF

Figure 60 : Channel 3 (72kHz) - S/N = -10dB, Input 1mV = -60dB
Noise (-70dB)



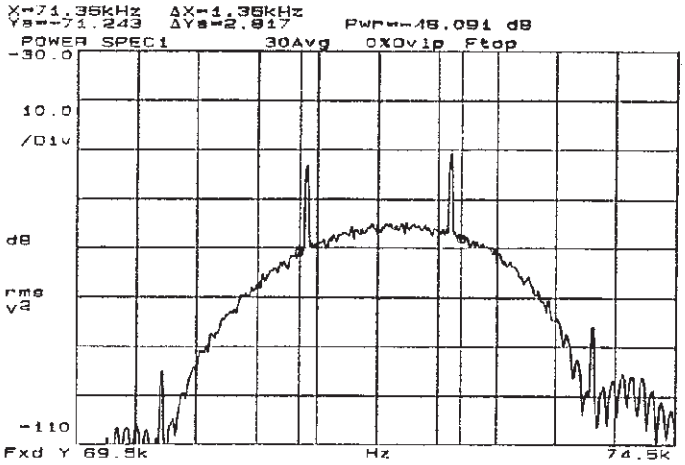
7536-66.TIF

Figure 61 : Channel 3 (72kHz) - S/N = -10dB, Input 1mV = -60dB
FSK + Noise



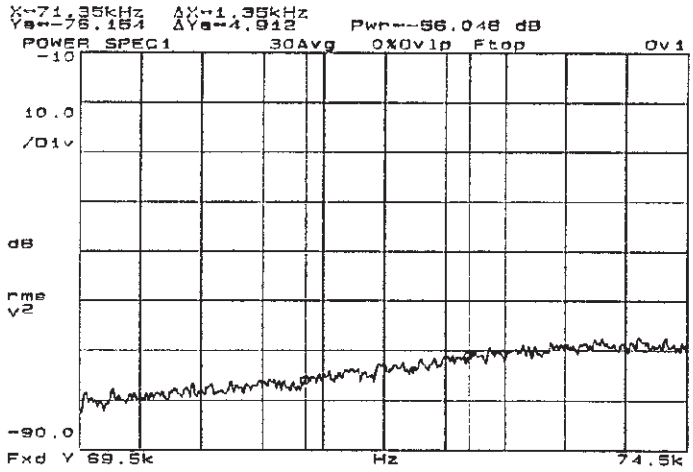
7536-67.TIF

Figure 62 : Channel 3 (72kHz) - S/N = -10dB, Input 5mV = -46dB
FSK (-46dB) - 5mV



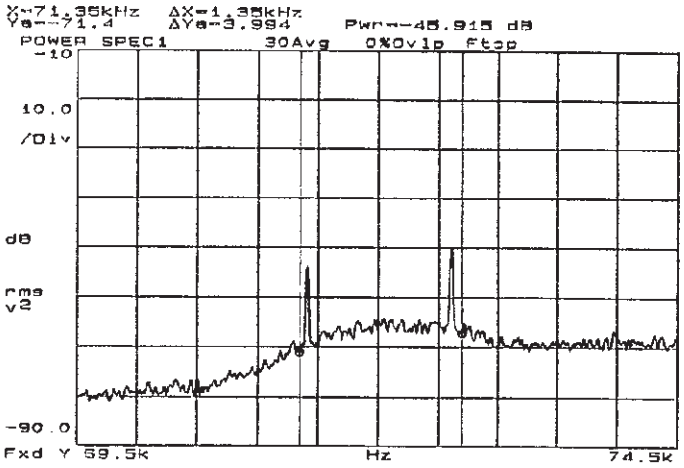
7536-68.TIF

Figure 63 : Channel 3 (72kHz) - S/N = -10dB, Input 5mV = -46dB
Noise (-56dB)



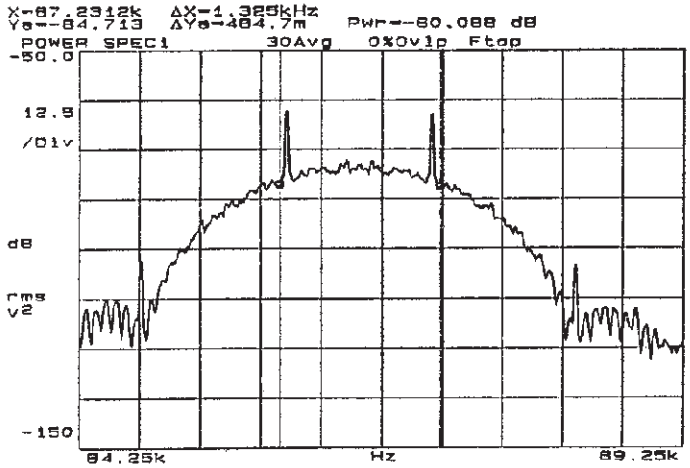
7536-69.TIF

Figure 64 : Channel 3 (72kHz) - S/N = -10dB, Input 5mV = -46dB
FSK + Noise



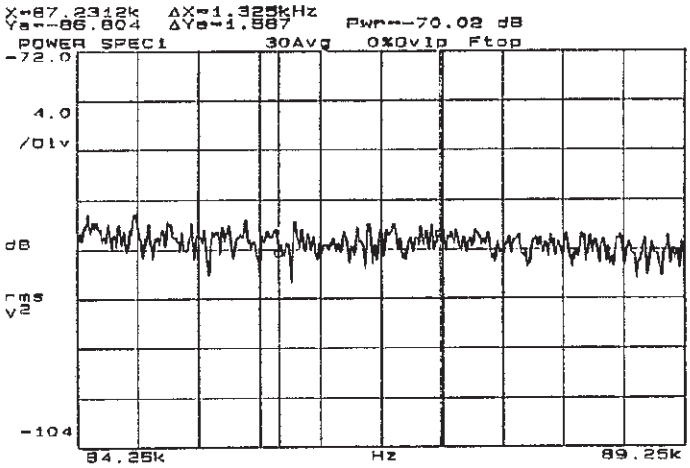
7536-70.TIF

Figure 65 : Channel 4 (86kHz) - S/N = -10dB, Input 1mV = -60dB
FSK (-60dB) - 1mV



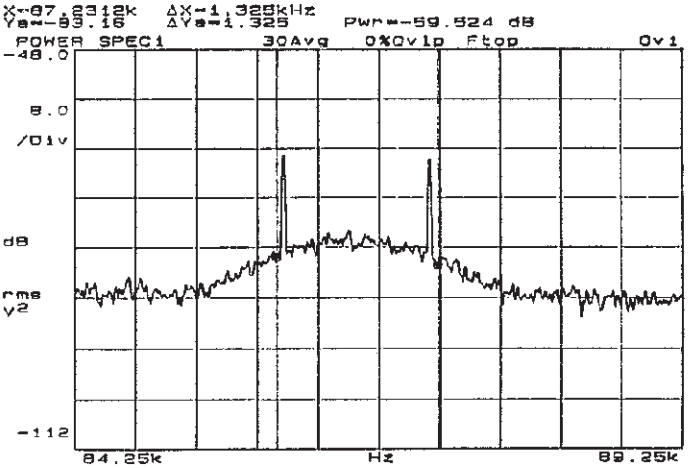
7536-71.TIF

Figure 66 : Channel 4 (86kHz) - S/N = -10dB, Input 1mV = -60dB
Noise (-70dB)



7536-72.TIF

Figure 67 : Channel 4 (86kHz) - S/N = -10dB, Input 1mV = -60dB
FSK + Noise



7536-73.TIF

ANNEXE C : BOARD SCHEMATICS

Figure 68 : ST7536 Master

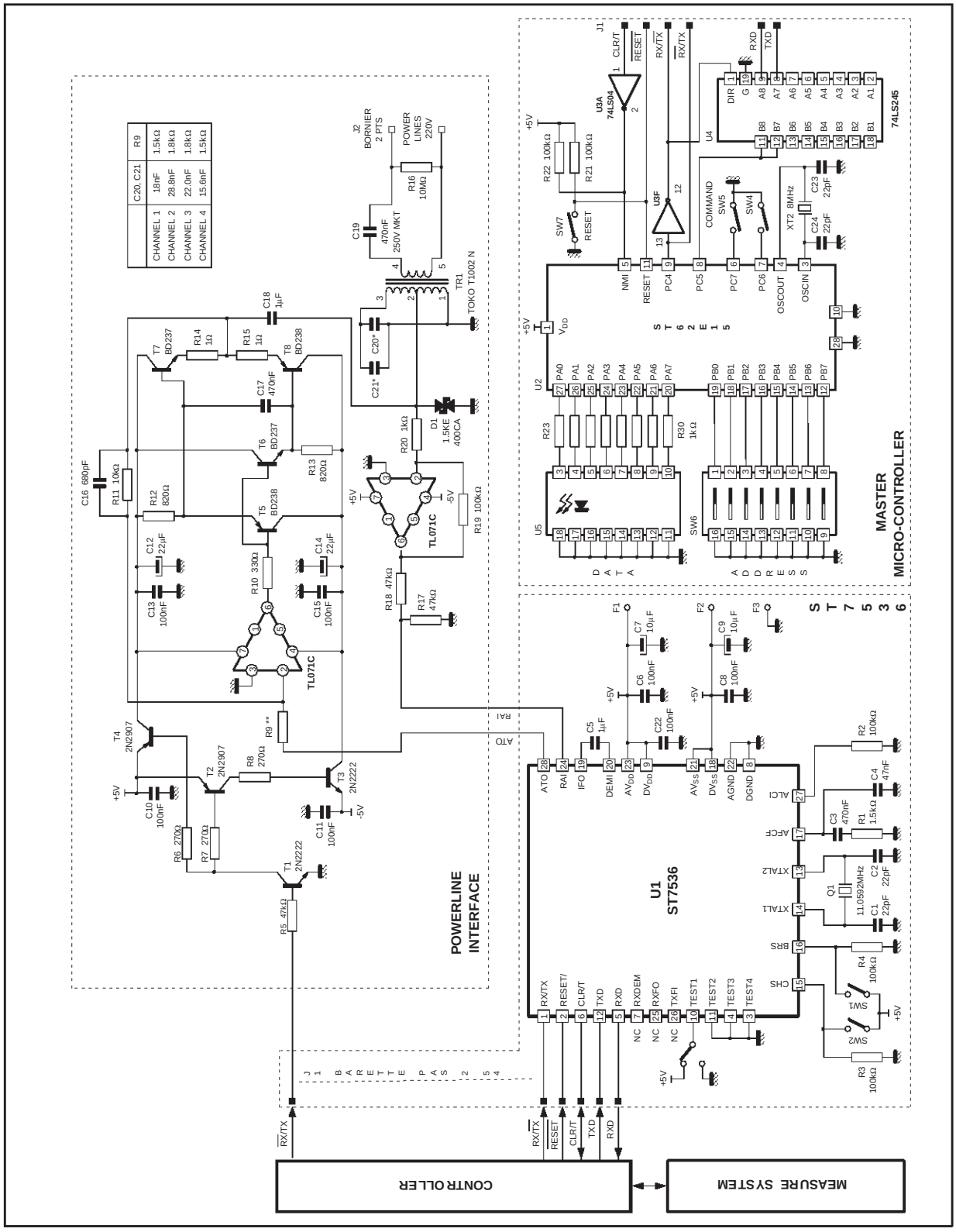


Figure 69 : ST7536 Slave