Austria Mikro Systeme International AG

AS5501 / AS5502
Multimode Powerline-Modem

Data Sheet
Rev A

Multimode Powerline-Modem

AS5501 / AS 5502

Key Features:

AS5501/02 is an FSK-modem device for **narrow-band FSK** communication via a Power-Line. The device is operated with a single supply voltage of 5V while the attached TX-driver stage is generating a 7Vpp (AS5501) or a 14Vpp (AS5502) FSK-signal with very low distortion which needs a supply of the external driver stage of 12V (AS5501) and 24V (AS5502) respectively. The high output-voltages which gets coupled to the power-line by using a transformer with proper ratios gives the advantage to lower the output impedance of the buffer while the buffer supply-current gets kept small.

Precise filtering gives an receiver performance with low BER-figures at <13dB of S/N white inband-noise and <-40dB S/N with monochromatic outband-noise and a sensitivity of 1.5mV

The carrier frequency is programmable in a range from 64kHz to 140kHz to support a big variety of communication-bands including home-automation applications.

Modulation depth and Baud-Rate are programmable to 600Hz/1200Hz and 600, 1200, 2400B/s.

There is a carrier-detect function included to support channels with protocoll.

In addition to the modem-function a reference voltage output is available as well as a supply-supervision.

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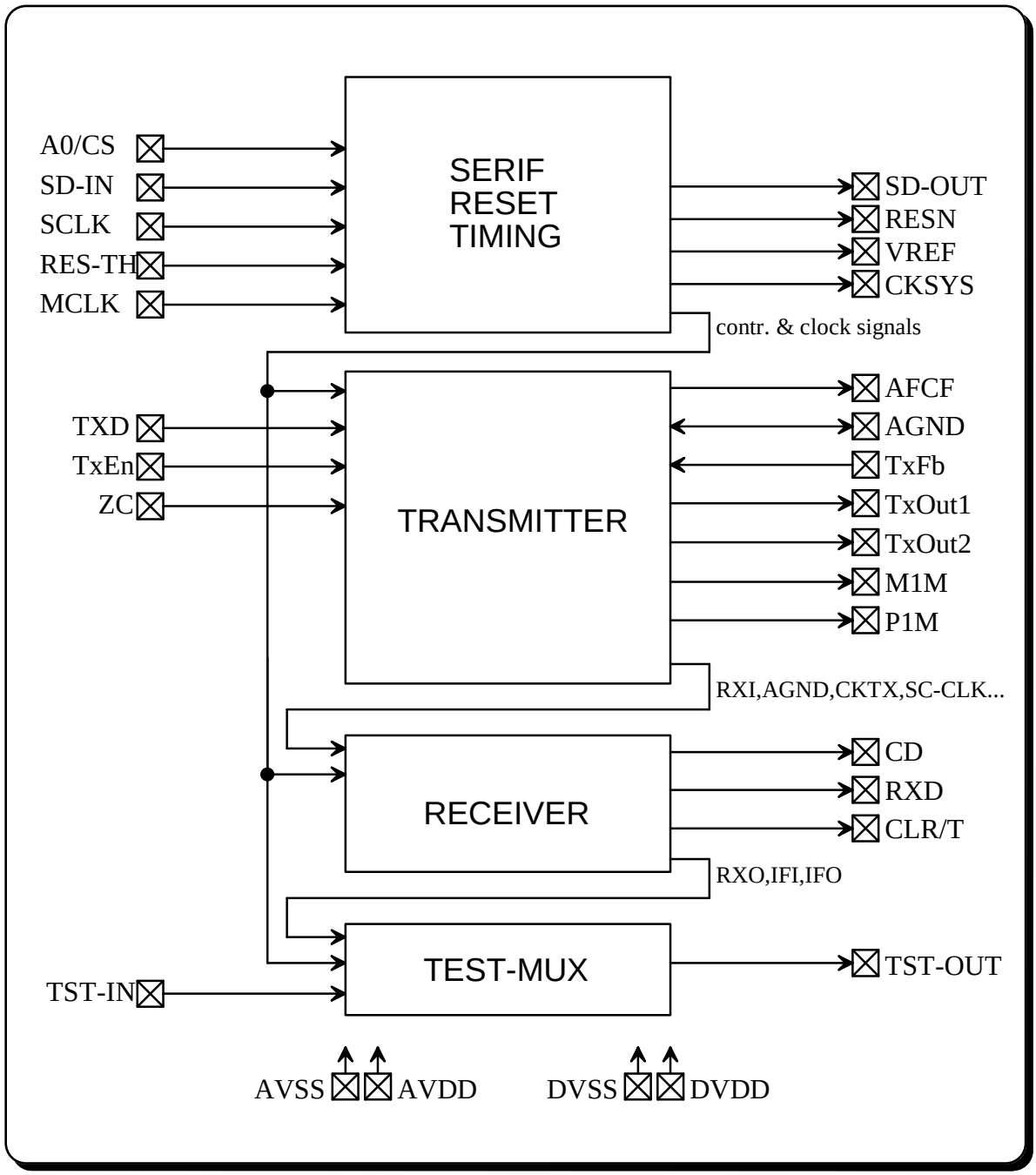
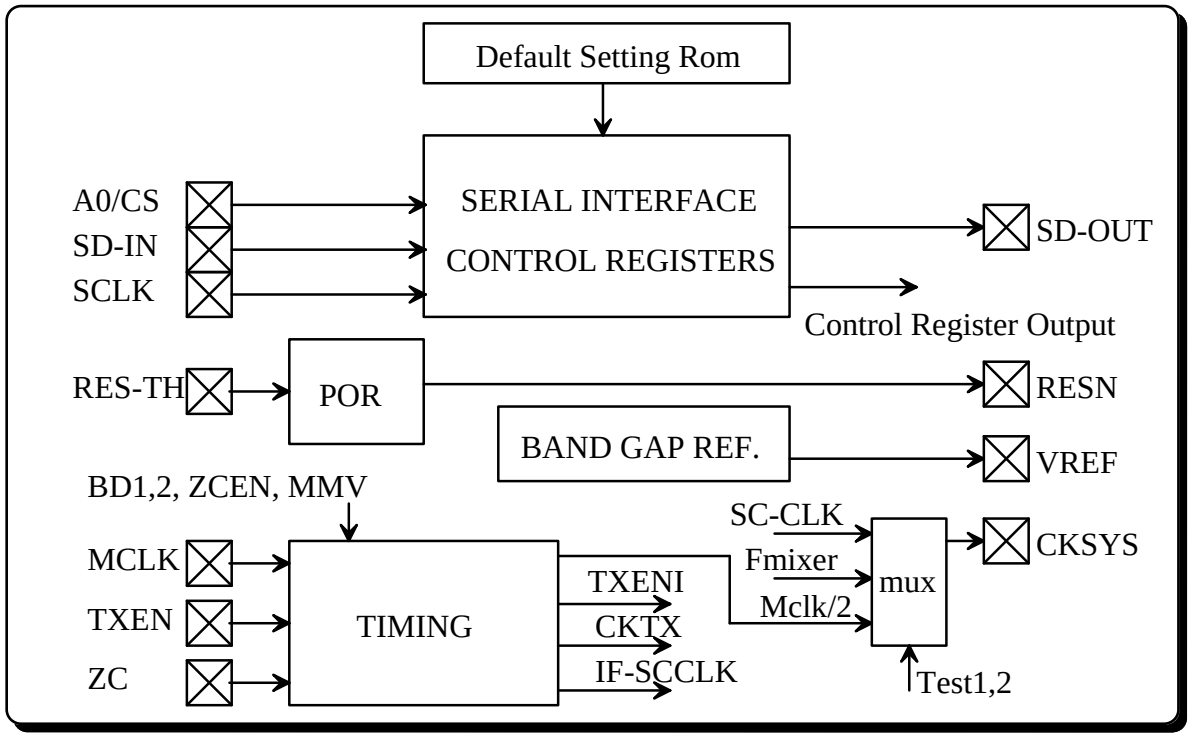
1. FUNCTIONAL DESCRIPTION

The AS5501/02 is a SYNCHRONOUS HALF DUPLEX FSK MODEM with programmable FSK-frequencies, Baud-Rate and ReceiverFilter-Characteristics working with a single +5V SUPPLY. The circuit is designed to be used with an external buffer-stage and transformer-coupling to transfer data over a POWER-LINE.

A mask-programmed default setting defines the state after power-up (reset) see chapter 1.1. With the serial interface the default setting can be overwritten.



1.1 SERIF, RESET, TIMING



1.1.1 SERIAL INTERFACE

There is a serial interface implemented for setting the control bits by a CPU.
Three bytes are available with following definitions and default contents (after reset).

Reg.-Name	addr	D1	D2	D3	D4	D5	D6	D7	D8
MRK-REG (def. value)	00H	MRK1 1	MRK2 0	MRK3 1	MRK4 0	MRK5 0	MRK6 0	MRK7 1	MRK8 1
GLOBAL (def. value)	01H	MRK9 1	BD1 1	BD2 1	RxBw1 1	RxBw2 0	ZCEN 1	MMV 0	PWD 0
TEST	02H	TEST1	TEST2	ASYN	AgcH	digMix	noTSTin	TxSyn	FCdOn

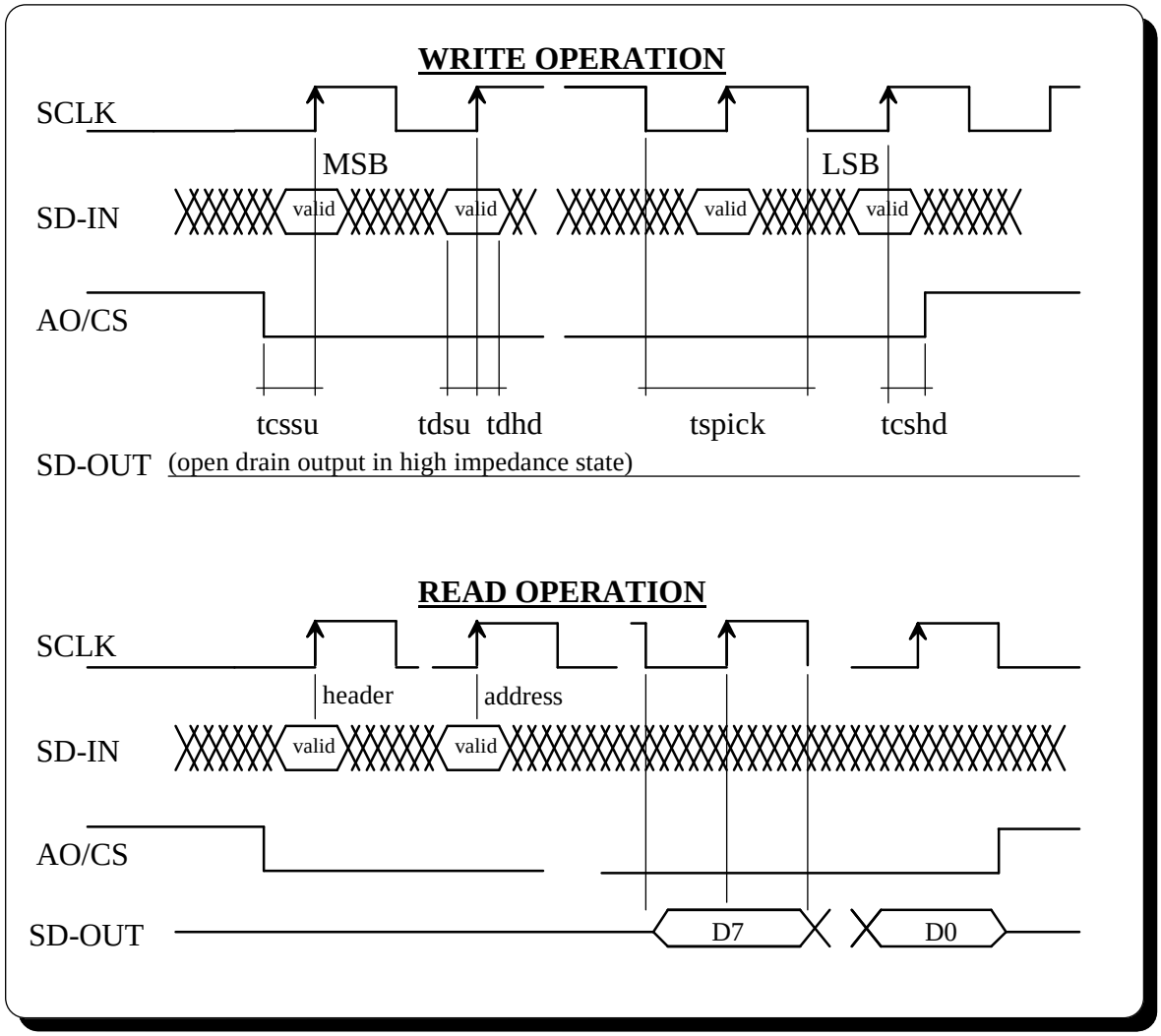
(The default setting of the register "TEST" is always 00h.)

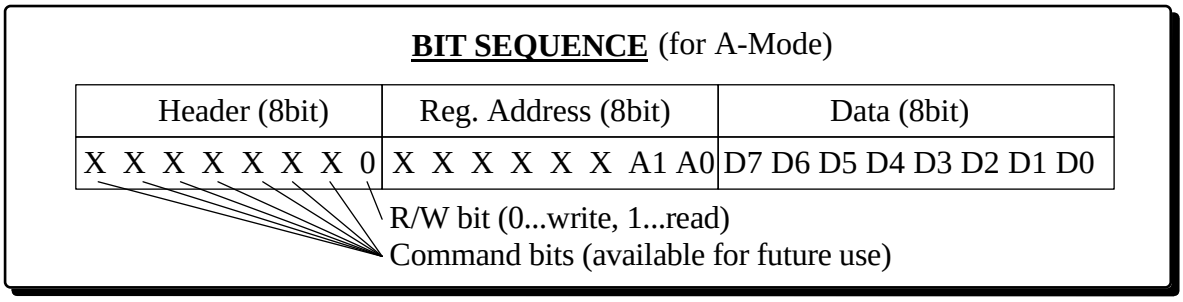
Bit-Name	Function	default val.	default function
MRK1-9	defines TX Mark Frequency (63.9k-140.55kHz)	453	131.85kHz
BD1,2	defines Baud-Rate and Modulation-Depth	1, 1	2400Hz/1200Hz
RXBW1,2	defines RX-BandPassFilter Bandwidth	1, 0	4.8kHz @132.45kHz
ZCEN	disable ZeroCrossing TX-Sync	1	ZC-disabled
MMV	disables transmit Timeout	0	TimeOut enabled
PWD	enables power down mode	0	powered up
TEST1,2	enables Test Mode 1-3	0, 0	normal mode
ASYN	disable synchronized receive data RXD	0	sync. RXD
AgcH	hold AGC counter-state	0	AGC-loop active
digMix	enables digital mixer; analog mixer enabled by def.	0	analog mixer
noTSTin	TST-out function only for receiver debugging	0	TSTin&out availab.
TxSyn	enables TXD sampling with CLR/T rising-edge	0	CLR/T gets synchronised by TXD-edges
FCdOn	enables faster CD-ON timing (5/Bdrate)	0	Tcdon=(10/Bdrate)

Default Setting: The default values shown in the table above, are related to the standard version of this device.
(Default setting of the registers can be changed by modification of the IC's metal2 layer. In this way special versions of this device can be defined and produced which are identified by different marking (see paragr. 2). A special version will however only be installed for annual deliveries not lower than 100000 devices and against upfront funding for the special tooling required.)

Serial Interface Operation:
The serial interface is built to work in two different modes. The mode of operation is defined by the logical state of the signal SCLK sampled (using the first rising edge of Fosc/512 signal) 46usec after a high going edge of the reset signal (RESN).

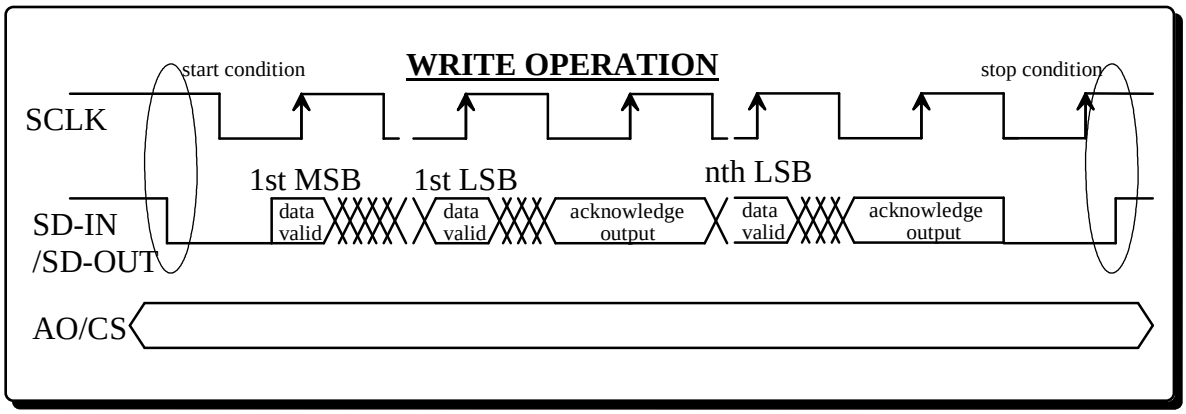
A-Mode (standard)
Features:
- 2 or 3 wire serial bus
- 8 bit data format
- data gets clocked on rising edge and shifted on falling edge of SCLK
- default polarity of signal SCLK is LOW (CPOL=0, CPMA=0)
- single and sequential read and write operations possible
- D7 is first bit

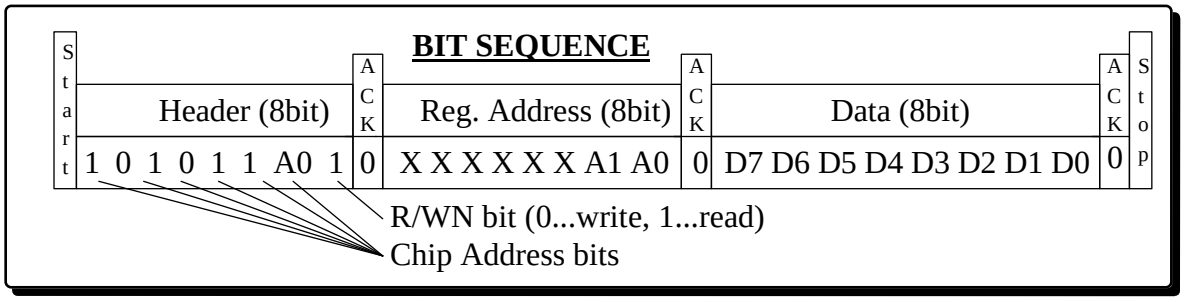




B-Mode

Features:
- 2 wire serial bus
- 9 bit data format
- data gets clocked on rising edge and shifted on falling edge
- single and sequential write operation possible
- default polarity of signal SCLK is HIGH
- acknowledge bit (9th bit) output (0 ... data acknowledged)
- D7 is the first bit
- A2 and A1 chip-address bits are internally set to 1

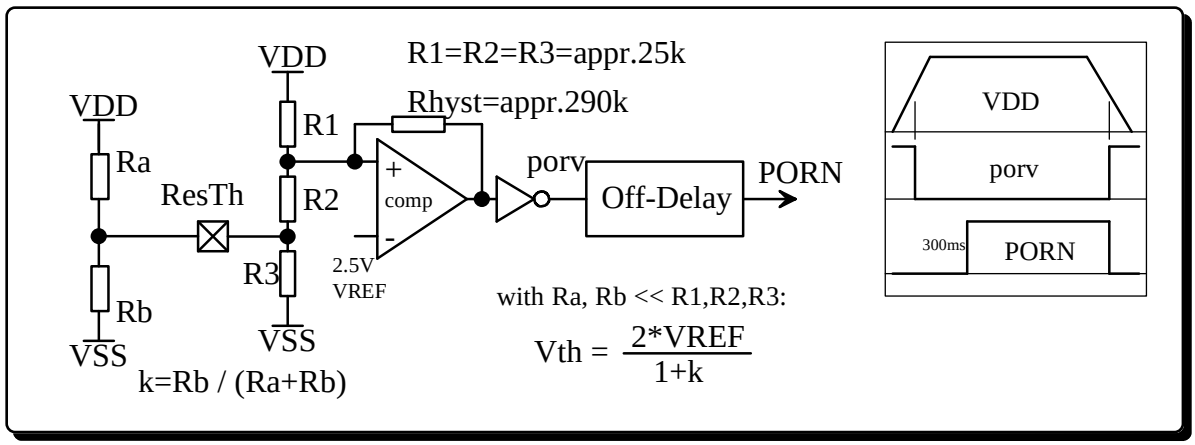




1.1.2 RESET

VREF: A Band Gap Reference block is included for generation of a reference-voltage VREF with nominal 2.5V needed for an external function (power-fail detection) and as reference for the power on reset.

POR: A power-on reset function with external adjustable threshold and fixed off-delay (300ms) defined by the master-clock is implemented. When pin RES-TH is floating the POR-OFF threshold is nominal 3.75V.There is a hysteresis of typ. 100mV implemented to V-ON. (In Test-Mode 2 and 3 the Por-delay is reduced to 1.17ms)



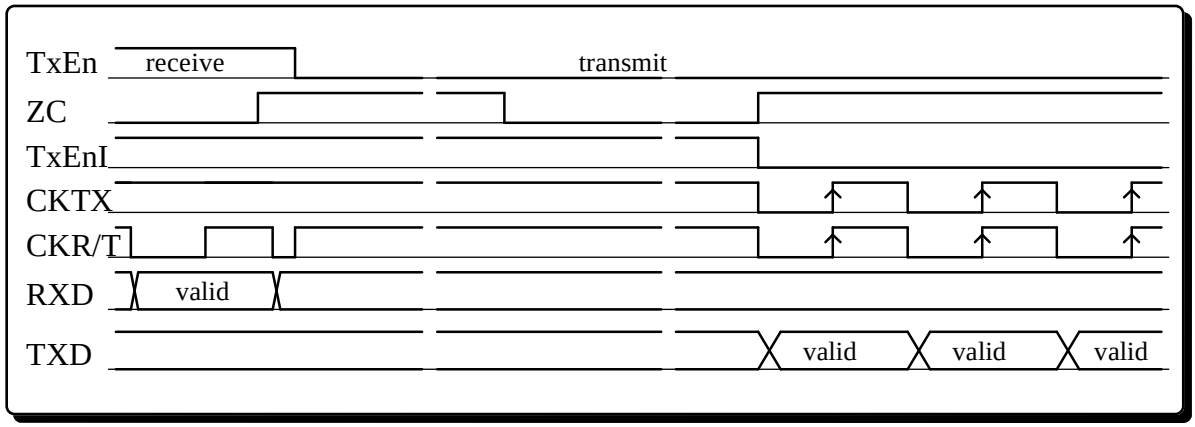
With V(ResTh) defined by external resistors much smaller than R1-3, the POR- threshold can be set in the range of 2.5V to 5.0V according to the given equation.

1.1.3 TIMING

MCLK: The circuit gets clocked by an 11.0592MHz MASTER CLOCK from external which is the frequency reference for all RX and TX functions. Since this circuit is working as a narrow band FSK-modem, the precision of this clock is very critical.

CKSYS: The master-clock divided by 2 is presented at the output CKSYS. In test-mode1 this pin is used to measure the FSK_ZC signal. In test-mode 2 this pin is used to measure the PLL-output SC-CLK. In test-mode 3 this pin is used to measure the PLL-output Fmixer.

TxEnI: Transmission gets initialized by setting the input signal TxEn to low. When ZCEN (zero-crossing TX-sync) is disabled, the internal signal TxEnI is following and setting the TX-driver active immediately. When ZCEN is enabled, the signal TxEnI is set to low after the high-going edge of ZC-input after TxEn was forced low.



TXD-input gets strobed by CKR/T in TxSyn-mode which can be entered with setting D7 of the TST-Reg. to H. In default mode (asynchr. TXD) the CKR/T gets synchronised by TXD-edges with a clock 64 times the baud-rate.

TX-TIMEOUT: There is a timeout-function implemented which sets the device back to receive-mode (TxEnI=H) after 3 seconds of transmission. This timeout-function can be disabled by setting the contol-bit MMV by the serial interface. In test-mode 2 and 3 the 3sec timeout is divided by 256 to 11.7ms to reduce test-time.

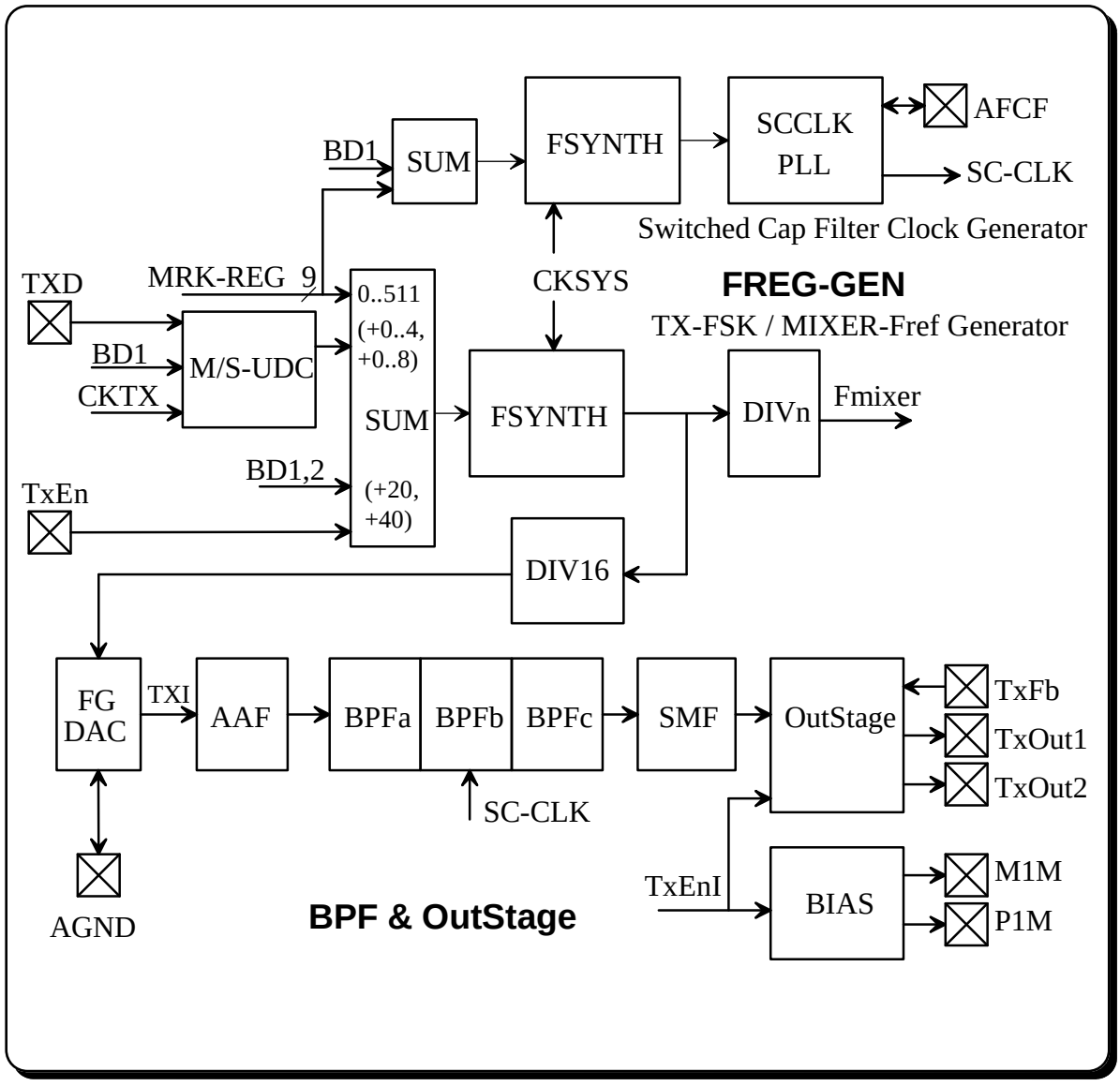
CKTX: The transmit clock is dependent on the Baud-Rate setting BD1,2.

BD1	BD2	division factor fom CKSYS	Baud-Rate (CKTX)
0	0	9216_{dec}	600Hz
1	0	4608_{dec}	1200Hz
0	1	4608_{dec}	1200Hz
1	1	2304_{dec}	2400Hz

IF-SCCLK: The intermediate frequency SC-filter is settable to two different modes, one for dF=600Hz and the other for dF=1200Hz (dF=Fspace-Fmark). These modes are defined by the SC-clock frequency which is generated in the timing block.

BD1	BD2	IFcenter	IFbandw	division factor fom CKSYS	IF-SC-CLK
0	X	2700Hz	1200Hz	96_{dec}	57.6kHz
1	X	5400Hz	2400Hz	48_{dec}	115.2kHz

1.2 TRANSMITTER



There is one FREQUENCY-SYNTHESISER used to generate the FSK-signal.
With the input signal TXD strobed with the high going edge of CKTX the control input of the synthesiser gets modified which results in frequency shift corresponding to the data-input.

In receive-mode, the same synthesiser is used to generate the Mixer reference-clock.
The Mixer-Frequency Fmixer is set to a value to fold down the FSK-signal to one of two possible IF-frequencies (2.7kHz / 5.4kHz).

The SCCLK-PLL is used to filter the phase jitter of the second frequency-synthesiser generating the reference-clock for the SC-Filter. There is an external capacitor needed as low-pass filtercomponent of the PLL-loop.

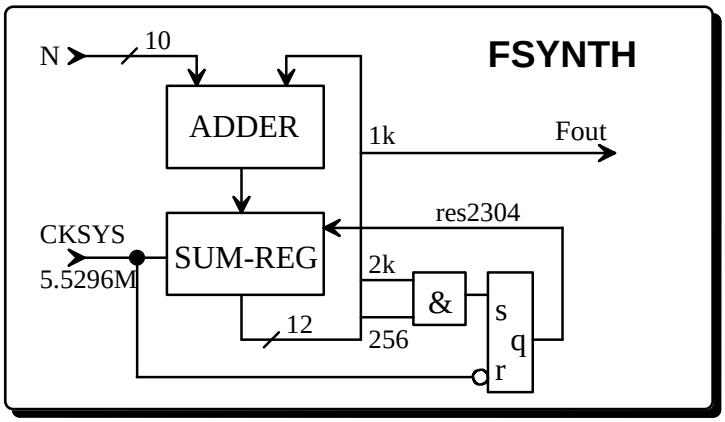
The BANDPASS Filter is used to limit the output-spectrum properly for power-line modem applications.

The OUTPUT-STAGE is designed to be connected to an external buffer arrangement for minimising the output-impedance and increasing the output-swing. The interface to the external circuit is done with special I/O-pins allowed to operate with voltages up to +24V.

With two bias pins M1M and P1M the external buffer-stage gets biased (activated). When these two pins are inactive, the buffer is in a high impedance-mode.

1.2.1 FREQ-GEN

Since the FSK-signal shall be programmable in steps of 150Hz, and the CKSYS clock-frequency is 5.5296MHz the following structure is used for frequency generation:



The SC-CLK is defined to be 16 times the center-frequency of the bandpass filters.
For generating the FSK or MIXER-frequency, Fsynth gets divided by 16 for generation of proper DAC input signals.
This means for both synthesisers the frequency steps are 2400Hz.

To get a resolution of 2400Hz a division by 2304 has to be done by subtraction of 2304 whenever the contents of the SUM-REG exceeds 2303.

SUBSTR = 5529.6kHz / 2.4kHz = 2304 (=> res 2048+256)

To generate mark-frequencies in the range of 63.9 ... 140.55kHz, the adder factor Nmark has to be: Nmark = 16*Fmark / 2.4kHz

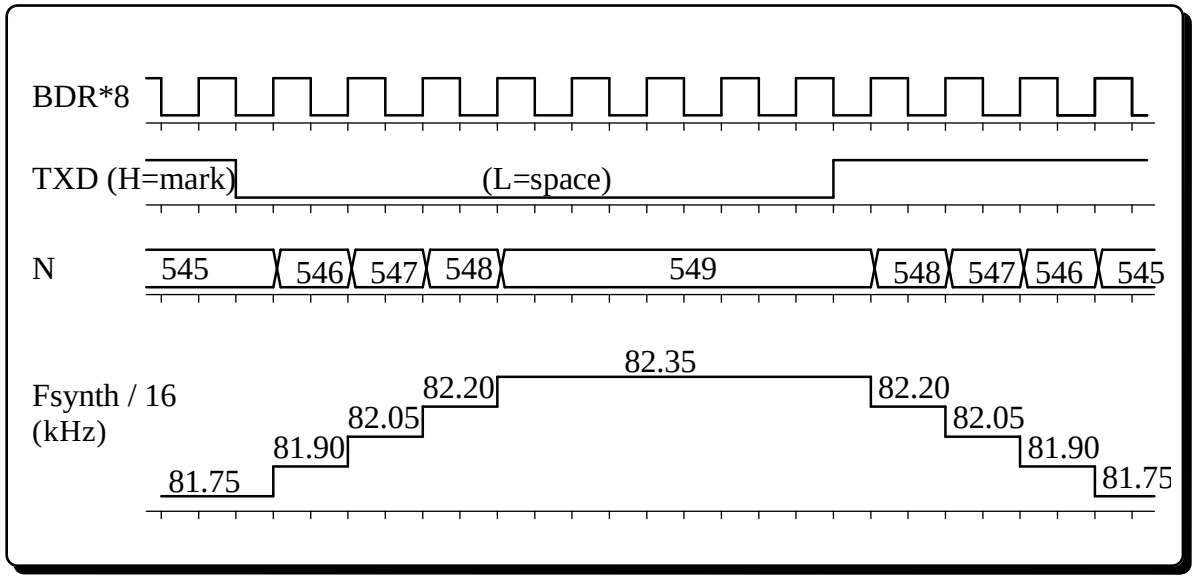
To cover the wanted frequency-range with a 9 bit word, a fixed number of 426 is added.

	MRK-REG	Nmark = MRK-REG+426	Fout	Fmark
min	0	426	1022.4kHz	63.9kHz
max	511	937	2248.8kHz	140.55kHz

To establish the frequency modulation, the output of the mark/space up/down-counter gets added to Nmark. There has to be a smooth frequency-change from mark to space and from space to mark within half the bit-time with 3 intermediate frequencies.

BD1	BD2	Fspace-Fmark	Baud-Rate (CKTX)	M/S-UDC	BDclk (UDC-CLK)
0	0	600Hz	600Hz	0,1,2,3,4	4800Hz
1	0	1200Hz	1200Hz	0,2,4,6,8	9600Hz
0	1	600Hz	1200Hz	0,1,2,3,4	9600Hz
1	1	1200Hz	2400Hz	0,2,4,6,8	19200Hz

Example with MRK-REG=8 => Fmark=81.75kHz; BD1,2=0 => dF=BRate=600Hz:



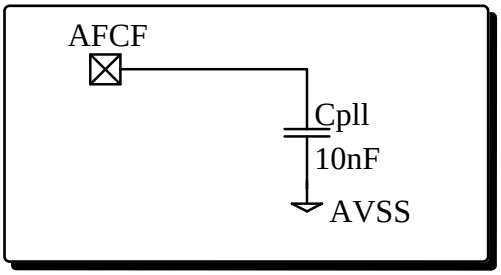
In receive-mode(TxEn=1), a constant number Nmix defined by BD1 gets added to Nmark instead of the output of the M/S-UDC. This gives a constant frequency which is used as Mixer-frequency to fold the FSK-signal down to 2.7kHz or 5.4kHz. According to the mixer-frequency the IF-SC-CLK is defined by the timing-block (see 1.1.3).

BD1	BD2	IFcenter	IFbandw	IF-SC-CLK	Nmix	BDclk (UDC-CLK)
0	X	2700Hz	1200Hz	57.6kHz	20	4800Hz
1	X	5400Hz	2400Hz	115.2kHz	40	9600Hz

The second frequency-synthesiser which is a similar structure as described for generating the FSK-frequencies, is generating the target-frequency for the SCCLK-PLL. To get no disturbing components, the phase-jitter of the synthesiser has to be reduced by the PLL. There is a capacitor needed as external low-pass filter, to define the frequency response of the PLL-loop. To generate the right target-frequency, one half of modulation-depth which is a factor of 2 or 4 dependent on BD1 has to be added to Nmark. Since the center-frequency is a very critical parameter, there is a possibility implemented for adjustment by wafersort-trim.

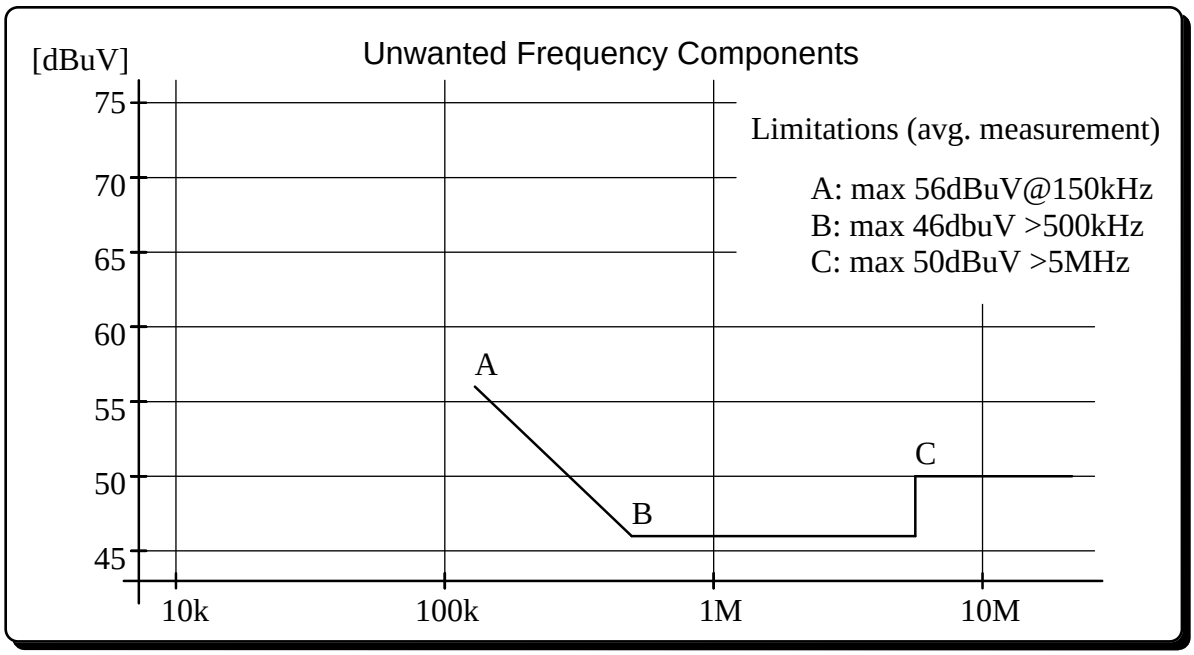
BD1	BD2	Fspace-Fmark	(Fcenter-Fmark)/150Hz	Npll
0	X	600Hz	2	MRK_REG + 426 + Itrim + 2
1	X	1200Hz	4	MRK_REG + 426 + Itrim + 4

(Itrim=0 ... 3 defined at wafer-sort)



1.2.2 TX-BPF

The staircase waveform generated by the FG-DAC in combination with the divider by 16 has to be filtered by an anti-aliasing filter because the SC-Filter clock is not synchronous to the FSK-signal. There is a 6th order bandpass filter, which is also used as receive-filter in receive-mode, implemented to reduce the FSK-spectrum. The filter-clock gets canceled by a smoothing filter at the end of this filter-chain.
Both, AAF and SMF will be designed in a way to move their corner-frequencies according to the frequency-band programmation. With the help of the resonator built with the transformer and attached capacitor, the unwanted frequencies (SC-clk, harmonics) are attenuated so that the signal spectrum at the transformer-output passes the following specification



1.2.3 Output-Stage

AS5502: The output stage is designed to amplify the FSK-signal by a factor of 7 with the help of an external buffer-stage to 14Vpp. The transfer from the 5V circuitry (asic) to the 24V buffer-structure is done by current-source outputs. The on-chip resistor-network is done in a way to shift the DC-operating point from 2.5V (on chip) to 12V (ext. buffer). With this output-voltage a transformer with a ratio of 2.5:1 can be used (VLmax=2Vrms). The buffer gives a very low impedance which is needed to modulate the power-line (Line-impedance: 5 .. 150ohm).

AS5501 is available for 12V buffer-supply

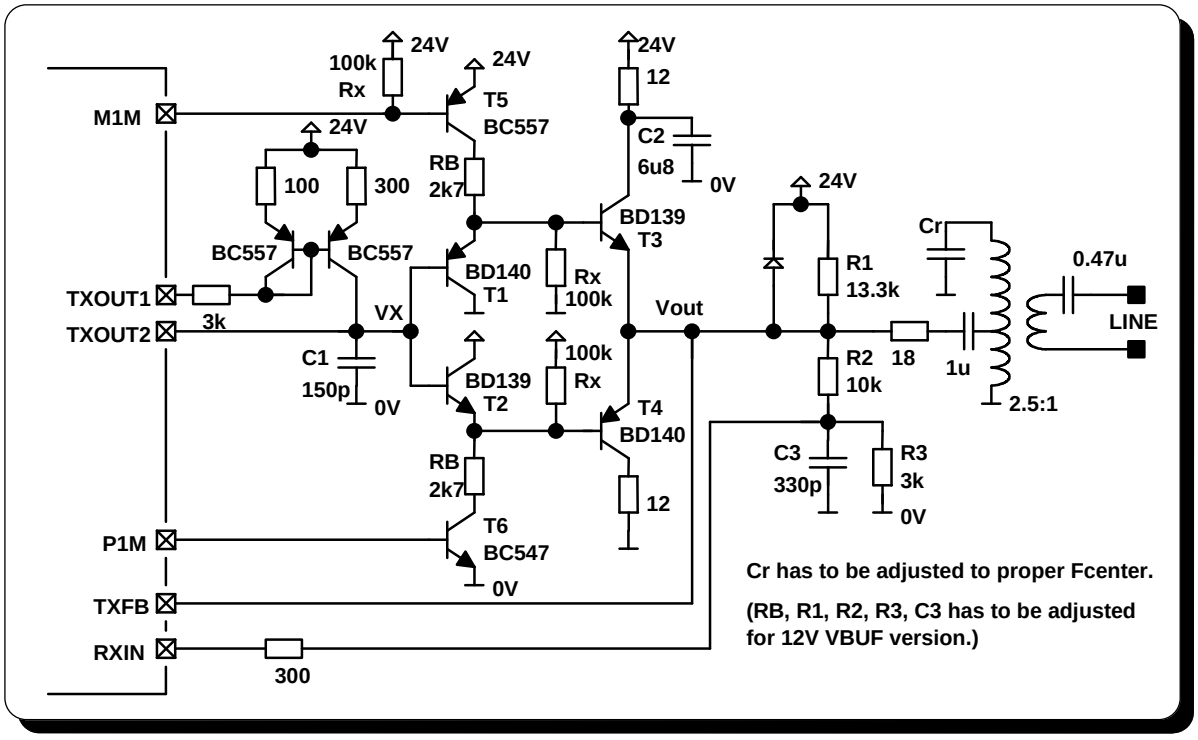
- amplification-factor: 3.5 instead of 7.0
- buffer DC-operating point: 6V instead of 12V

With the bias-current outputs M1M and P1M the transistors T5 and T6 get switched on and the driver stage is activated. The TxOut1,2 output-currents are in the range of 3mA with complementary AC-components. For stability-reasons it is needed to place a capacitor of 150pF from node VX to VSS.

The circuit with T1-T4 is a unity gain buffer structure. The transformer with attached capacitor Cr gives a resonator for the used frequency-band.

With the shown test-circuit, the harmonic distortion has to be within the following limits with a power-line load of (5ohms+50uH) // 50ohms:

	ratio to the fundamental
2nd Harm.	min. 70dB
3rd Harm.	min. 75dB
higher Harm.	min. 80dB



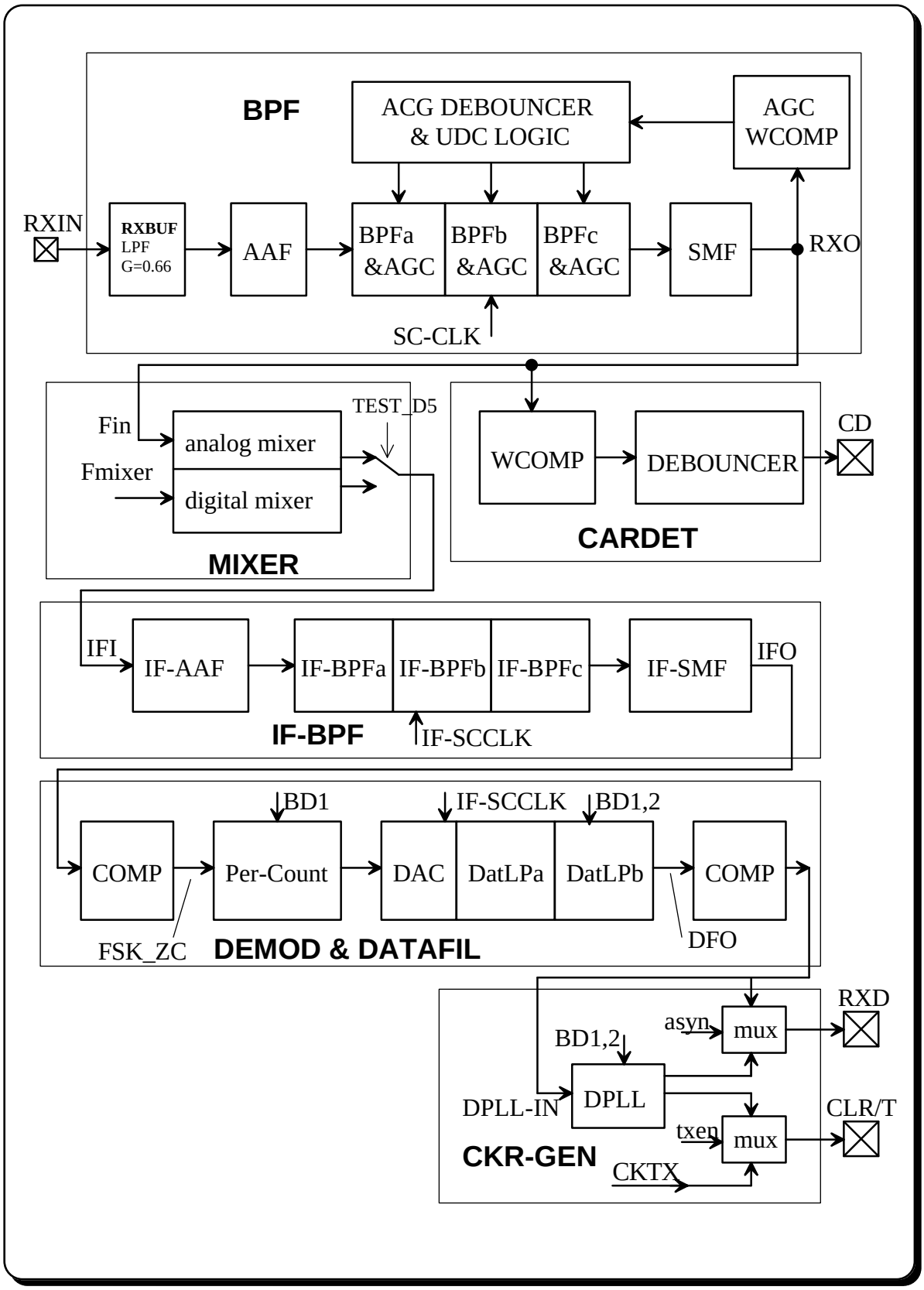
In receive-mode, when the bias-currents are turned off, the base of the two output-transistors are forced by resistors of 100k (Rx) to 0V and Vbuf respectively to guarantee high impedance of the buffer. The current of the pins TxOut1,2 is 0 (VX is floating). Since the receiver-AGC is reacting on signal levels at the RXBPF-filter output, high outband noise-components could give clipping in the first stages of the receiver path. To avoid this, aa attenuation of 16dB with R2, R3, C3 is realized.

(Monochromatic Noise Measurement: Outband-noise with 0dBV @ line w. 80% AM (1kHz)
=> 12.8Vpp after transformer;
=> 2.0Vpp at pin RXIN;)

The resistors R1, R2, R3 are calculated to have a DC-voltages of Vbuf/2 at node Vout and 2.5V at node RXIN. An external diode for protection against high positive voltages is needed at Vout (Pin TXFB).

1.3 RECEIVER

The receiver consists of the following blocks:
BPF(RX,TX common), MIXER, CARDET, IF-BPF, DEMOD, DATAFIL and CKR-GEN



The received signal gets filtered by the BANDPASS filter. An AGC-function is implemented in this filter, to have improved performance over a wide range of input signal amplitude. The filtered signal gets transferred to a low frequency band by the use of an MIXER-CIRCUIT so that the frequency-band can be further reduced by an additional IF_BANDPASS. The IF-filter output-signal gets DEMODULATED, FILTERED and SYNCHRONIZED to a receive-clock. In receive mode the CLOCK-RECOVERY circuit is generating the receive-clock locked to the RX-data edges. The input signal gets compared with a fixed CARRIER DETECT threshold to get valid RX-data to be further processed by the connected CPU only.

1.3.1 RXBPF

The bandpass-filter eliminates the frequency components which are not of interest. The Bandwidth is programmable in 3 steps with the control-bits RXBW1 and RXBW2.

RXBW1	RXBW2	BW/Fcenter	BW @ 72.00kHz	BW @ 82.05kHz	BW @ 132.45kHz
0	0	+/-4.2%	**6.0kHz**	(6.8kHz)	(11.0kHz)
1	0	+/-1.8%	(2.6kHz)	**3.0kHz**	**4.8kHz**
0	1	+/-2.3%	(3.3kHz)	(3.7kHz)	(6.0kHz)

The center-frequency of the filter is defined by the SC-Clock-Frequency (MRK-REG and the bits BD1,2) in steps of 150Hz. (See paragraph 1.2.1 FREG_GEN).
Frequency-Response with RXBW1=1, RXBW2=0:

Fin / Fcenter	typ. rel. Gain
0.67	-45dB
0.98	-3dB
0.99	0.0dB
1	reference
1.01	0.0db
1.02	-3dB
1.5	-45dB

As already mentioned in the transmitter description, the AAF and SMF of the bandpass-filter are tuned according to the SC-Clock and therefore to the BPF-centerfrequency.
An additional attenuation of the mains-frequency (50Hz ..) is not needed because of the external coupling which is already a very good filter for that.

The input-voltage range which has to be handled is 1.5mV ... 1.5Vrms. The signal of the input-pin RXIN gets buffered and lowpass-filtered by the RXBUF with a fixed gain of 0.66. (Max. input level 14Vpp@transformer =>2.2Vpp@Rxin =>1.5Vpp@FilterInput)
The gain of the SC-BPF is controlled by the AGC loop to keep the filter-output RXO constant at 1.0Vp for a wide range of input-dynamic. In total there is a variable gain from -3.6 to +41.4dB in steps of 1dB.

	V(Line)	V(Vout)	V(RxIn)	V(RXO)
min	-56.5dBV = 1.5mVrms	3.75mVrms = 10.6mVpp	1.7mVpp	0.20Vpp
max	+6dBV = 2.0Vrms	5.0Vrms = 14.0Vpp	2.2Vpp	1.45Vpp

The window-comparator threshold for the AGC-control is set to 1.02V+/-12%. The AGC-UDC will be clocked by 8*Fbaud which gives a max. settling time of 9.4ms at 600bps.

1.3.2 CARDET

The carrier detect circuit is comparing the RXBPF-output against a constant threshold. The carrier detect has to go active when the RXIN input-voltage exceeds 5mVp.

V(Line)	V(Vout)	V(RxIn)	V(RXO)
8.9mVrms	31.5mVp	5.0mVp	593mVp

The carrier detect ON-time can be choosen by D8 of the TST-Reg. The OFF-time is defined by the AGC-stage settling-time of max. 45/(8*Fbaud) plus 12 cycles of Fbaud*64.

	Fbaud=600	Fbaud=1200	Fbaud=2400
T (CD-ON) with TST.D8=L	16.7ms	8.33ms	4.17ms
T (CD-ON) with TST.D8=H	8.33ms	4.17ms	2.08ms
T (CD-OFF)	0.3 ... 9.7ms	0.15 ... 4.9ms	0.07 ...2.5ms

1.3.3 MIXER

There are two mixer stages implemented. The analog mixer (default) consists of an unity-gain amplifier-stage which is switched to inverting or non-inverting mode by the mixer-reference clock. The digital mixer, enabled with bit TEST_D5=H, consist of a comparator-stage with hysteresis of appr. 50mV with which the BPF-output gets transferred to digital. This signal gets combined with the mixer reference clock by an EXOR-gate.
For the two different modulation-depths, different intermediate frequencies are generated by proper generation of the reference-frequency. (see paragr.: 1.2.1 FREG-GEN)

BD1	Fspace-Fmark	IF
0	600Hz	2700Hz
1	1200Hz	5400Hz

1.3.4 IF-BPF

The mixer-output is fed to the input of the intermediate-frequency filter. According to the two different IF defined by BD1, this BPF is programmed to these frequencies by the IF-SC-CLOCK generator.

BD1	Fcenter	Band Width
0	2700Hz	1200Hz
1	5400Hz	2400Hz

The corner-frequencies of the AAF and the SMF are controlled accordingly.
The SC-filter is a 6th order filter with the following characteristics:

Fin / Fcenter	Fc=2.7k	Fc=5.4k	typ. rel. Gain
0.45	1200Hz	2400Hz	-45dB
0.78	2100Hz	4200Hz	-3dB
1.22	3300Hz	6600Hz	-3dB
2.14	5800Hz	11600Hz	-45dB

1.3.5 DEMOD & DATAFIL

The output of the IF-BPF gets transferred to digital by an comparator with pos. AC-feedback Vhyst~10mV. The periode-time is then measured by a counter which gets set to a proper starting point, so that at the end of a measurement-periode the frequency-delta is represented by a 4 bit word. This digital information is transformed again into analog by an DAC which is included to the input-stage of the SC-Datafilter. No AAF is needed because the DAC is synchronised with the filter. The unity-gain datafilter can be programmed to three different corner-frequencies according to the Baudrates of 600,1200 and 2400Hz.

Fin/Fbaud	typ. Gain
0.75	-3.0dB
1.3	-25dB

A comparator with hysteresis of appr. 200mV and adjustable (bias-distortion wafer-sort-trim) absolute reference is converting the DataFilter-output to RXDA (asynchronous receive data).

1.3.6 Bit Error Rate

The system specification of BER is the following:

	Parameter	Condition	min	typ	max
BER1	Bit Error Rate with Minimum Input Level	White Noise with S/N=13dB RXL = 1.5mVrms		$5*10^{-5}$	10^{-3}
BER3	Bit Error Rate with Maximum Input Level	White Noise with S/N=25dB RXL = 1.5Vrms		10^{-7}	10^{-3}
BER4	Bit Error Rate with Medium Input Level	White Noise with S/N=13dB RXL = 600mVrms		10^{-6}	10^{-3}
BER5	Bit Error Rate with Impulsive Noise	Noise: 5Vpp rect., 100Hz, DC=10%, Trise/fall=10us; RXL=90mVrms			10^{-3}
BER6	Bit Error Rate with Modulated Sinusoidal Noise	Noise: sine carrier w. 80% AM; Fmod=1kHz, special S/N-Mask RXL=1.5Vrms			10^{-3}

1.3.7 CKR-GEN

There is a digital pll for receive-clock reconstruction. The signal RXDA (async. RXD) gets synchronised by this clock which then gives the synchronous receive data signal RXD.
A multiplexer is used to select RXDA or RXD to be transferred to the pin RXD by the use of a control bit "ASYN". The signal RXDA is used to verify the Mixer and DataFil-structure.
A second multiplexer selects CKRX or CKTX to be transferred to pin CLKR/T by the use of control signal "TxEn". In synchronouse-mode RXD is valid at the high going edge of CKR/T.

1.4 TEST-MUX

A test-input pin, a test-output pin with attached buffer and multiplexers are used to have access to some internal nodes for testing. To have access to internal nodes of the receiver in normal receive operation, the bit TEST_D6 can be set to H for avoiding TST_IN function.
The asic is forced to one of these test-modes by setting the control-bits TEST1 and TEST2.

Test1	Test2	Mux-State	TST-IN	TST-OUT	CKSYS	Reset-Delay	TX-Timeout
0	0	0	bypass timer	VREF	MCLK/2	300ms	3sec
1	0	1	IFI	IFO	FSK_ZC	300ms	3sec
0	1	2	TXI	RXO	SC-CLK	1.17ms	11.7ms
1	1	3	DPLL-IN	DFO	Fmixer	1.17ms	11.7ms

Mux-State 0 (Normal Operation): In normal operation the test-muxes are in position 0. In this configuration, the reference voltage VREF (2.5V) is present at pin TST-OUT.
In this mode the reset and TX-timeout counter are bypassed with TST-IN set to H.

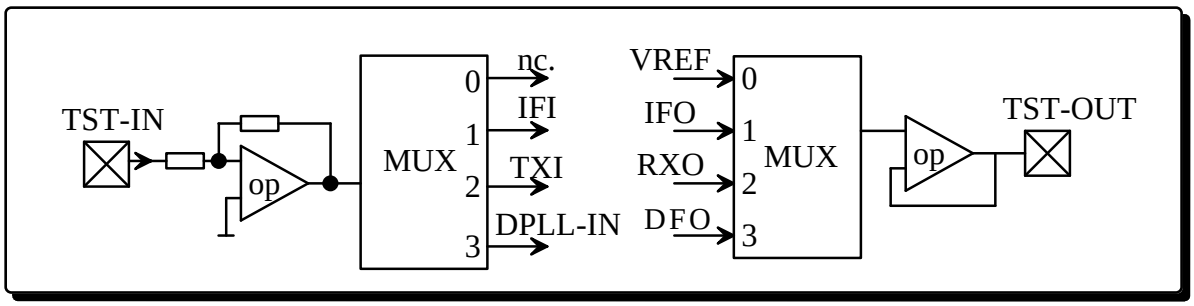
Mux-State 1(IF-Test):
In this mode the IFBPF can be measured by forcing the IFI via pin TST-IN and measuring IFO via pin TST-OUT. With pin CKSYS the FSK-ZC signal can be measured.

Mux-State 2 (TXPATH / RXO):
In this mode the TXPATH can be measured by forcing TXI via pin TST-IN and measuring the TX-Output-Stage output. The SC-CLK can be measured via pin CKSYS. The receiver bandpass filter can be measured by forcing RXIN and measuring TST-OUT (RXO).

Mux-State 3 (DPLL / DATAFIL):
In this mode the input of the RX-DPLL can be forced by TST-IN for digital verification of this block. Further the output of the data LP-filter can be measured at TST-OUT. The MIXER- PLL output can be measured via pin CKSYS.

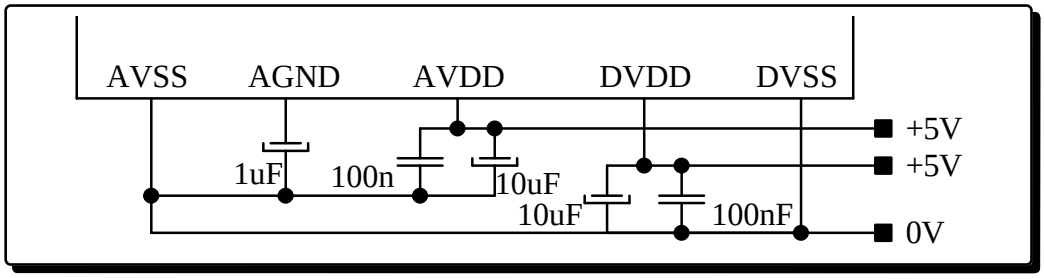
TX Timeout / RES-Delay Test-Mode: With bit "Test2" set to 1 the TX-timeout (3sec) and the RES-Delay (300ms) gets reduced by a factor of 256 for production test.

ASYN Test-Mode: The contol-bit "ASYN" is used for global verification of the receiver-block and especially for verification of the MIXER and the DataFilter by measuring the RXDA-jitter (isochronous-distortion).

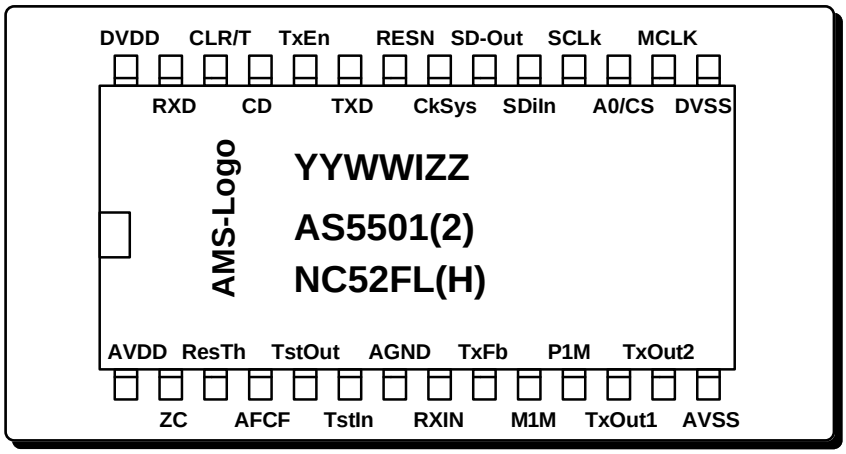


1.5 Supply and Analog Ground

There are two different pairs of supply pins, one for analog (AVSS,AVDD) and one for digital (DVSS, DVDD). The two VSS-pins have to be at the same level to avoid substrate-current. The two VDD-pins should not differ more than 0.25V. The reason for splitting the supply lines is to avoid noise from the digital circuit injected to the analog section.
The analog-ground is generated by resistive division of the supply-voltage to AVDD/2. Since the SC-clock is working in the range of >1MHz, an external capacitor of 1uF is needed to decouple the AGND to AVSS.
There has to be sufficient decoupling from AVDD to AVSS and from DVDD to DVSS separately. Usually a combination of a 10uF tantal and 100nF ceramic-capacitor is used dependent on the supply structure.



2. Package and Marking



Package: SOIC28

Marking:	YYWWIZZ	YYWWIZZ	(date code)
	AS5501	AS5502	(AS-number dependent on version)
	NC52FL	NC52FH	(coded default setup)

The default setup coded in the following way, gets printed as 3rt marking line:

Bonding option:
1st character ... "N" for not locked; "L" for locked version (pad LOCK bonded to VSS)
(Option "Not Locked": All control registers are accessable via SERIF)
(Option "Locked": Only contr. register TEST is accessable via SERIF)
6th character ... "H" for 24V buffer supply (standard version); " L" for 12V buffer supply;

Mask options:

Character	hex. rep. of reg.-bits	standard version bits	Char
2nd	MRK8-5	’1100’	C
3rd	MRK4-1	’0101’	5
4th	PWD, MMV, ZCEN, RXBW2	’0010’	2
5th	RXBW1, BD2, BD1, MRK9	’1111’	F

3. Pinlist

PIN#	Name	Type	Function
1	AVDD	supply	+5V supply pin for analog section
2	ZC	inp. w. pd	mains zero-cross input for transmission synchronisation
3	RES-TH	ana. inp.	reset threshold adjust input
4	AFCF	ana. i/o	compensation pin for PLL-loop
5	TST-OUT	ana. outp.	test function output pin (VREF in normal mode)
6	TST-IN	ana. inp.	test function input pin
7	AGND	ana. I/O	analog ground pin for external decoupling capacitor
8	RXIN	ana. inp.	receiver input pin
9	TxFb	ana. inp.	transmission feedback / receive input
10	M1M	ana. outp.	minus 1mA bias current for TX-buffer stage

11	P1M	ana. outp.	plus 1mA bias current for TX-buffer stage
12	TxOut1	ana. outp.	TX output 1
13	TxOut2	ana. outp.	TX output 2
14	AVSS	supply	0V supply pin for analog section
15	DVSS	supply	0V supply pin for digital section
16	MCLK	dig. inp.	master clock input (11.0592 MHz)
17	A0/CS	dig. inp.	serial bus control signal with pull up
18	SCLK	dig. inp.	serial bus clock with pull up
19	SD-IN	dig. inp.	serial bus data input with pull up
20	SD-OUT	dig. outp.	serial bus data open drain output with pull up
21	CKSYS	dig. outp.	system clock output (5.5296MHz)
22	RESN	dig. odo.	reset open drain output active at low supply
23	TXD	dig. inp.	transmit data input
24	TxEn	dig. inp.	transmit-mode txen=0 / receive-mode txen=1
25	CD	dig. outp.	carrier detect output
26	CLR/T	dig. outp.	receive / transmit clock output
27	RXD	dig. outp.	receive data output
28	DVDD	supply	+5V supply for digital section

4. ABSOLUTE MAXIMUM RATINGS

Max. Supply Voltage	-0.5V ... +7.0V
Max. Input Voltage	VSS-0.5V ... VDD+0.5V
Max. Current forced to any input or output except pin "P1M"	-100mA ... +100mA
Max. Current forced to pin "P1M"	-100mA ... +25mA
Max. Power Dissipation	700mW
Storage Temperature Range	-55 deg C ... 150 deg C
Humidity Noncondensating	5% ... 95%
ESD general limit (R=1.5kOhm, C=100pF, 3 pulses each pol.)	+/- 1kV
Lead Temperature (max. 10sec)	max 300 deg C

5. OPERATING CONDITIONS

Parameter	min	typ	max	unit
Operating Supply Voltage	4.7	5	5.3	V
Operating Temperature Range	-25	25	70	deg C

6. TEST SPECIFICATION

6.1 Test Conditions

Temperature: -25, 25, 70 deg C.

Signals:	Clock:	11.0592MHz forced to pin MCLK;
Modes:	"default":	condition after power-up/reset (see paragr. 1.1)
	"M72":	MRK= 50, BD1=H, BD2=L, RxBw1=L, RxBw2=L
	"M82":	MRK=119, BD1=L, BD2=L, RxBw1=H, RxBw2=L
	"M132":	MRK=453, BD1=H, BD2=H, RxBw1=H, RxBw2=L
	"RxMode":	TxEn = H;
	"TxMode":	MMV=H, TxEn=L (disable timeout)
	"norm. transm. seq.":	TxMode, M82, TXD: 010101..(with Ft=600Hz);

6.2 Power Consumption Test

VDD=5.3V	min	typ	max	conditions
I1(DVDD)	-	-	3mA	normal transmission sequ.
I2(AVDD)	-	-	36mA	normal transmission sequ.
I3(AVDD)	-	-	32mA	RxMode, M82, (receive)
I4(AVDD)	-	-	1mA	PWD=H

6.3 Input Characteristics

ZC (Schmitt-Trigger with pull down)	min	typ	max	Condition
IIL (vin=0V)	-10uA	0	10uA	-
IIH (vin=VDD)	80uA	150uA	250uA	-
VIL	-	-	1.1V	VDD=5.0V
VIH	3.9V	-	-	VDD=5.0V
Vhyst (not tested at production test)	1.2V	-	2.5V	VDD=5.0V

RES-TH (see paragr. 1.1)	min	typ	max	Condition
IIL (vin=0V)	-15uA	-23uA	-33uA	VDD=5.0V
IIH (vin=VDD)	30uA	45uA	65uA	VDD=5.0V

TST-IN (anal. buffer input)	min	typ	max	Condition
RIN (vin=0.5V ... VDD-0.5V)	20k	36k	60k	TM1, TM2
I pull-down (vin=vdd)	80uA	150uA	250uA	nor. Mode, TM3

TxFb (resistive divider)	min	typ	max	Condition
RIN (vin=0V ... VDD)	45k	82k	148k	RxMode, V24
RIN (vin=0V ... VDD)	25k	46k	83k	RxMode, V12

RXIN (receive input buffer)	min	typ	max	Condition
RIN (vin=0V ... VDD)	38k	68k	122k	RxMode

MCLK, A0/CS, SPI_CK, SPI-IN, TXD, TxEn (dig. std. input)	min	typ	max	Condition
I pull-up (vin=0V)	80uA	150uA	250uA	A0/CS, SPICK, SPI-IN
Ileak (vin=0..vdd)	-1uA	-	1uA	MCLK, TXD, TXEN
VIL	-	-	0.3*Vdd	-
VIH	0.7*Vdd	-	-	-

LOCK, V12N	min	typ	max	Condition
I pull-up (vin=0V)	10uA	20uA	35uA	at wafer-sort only

6.4 Output Characteristics

AFCF (PLL compensation)	typ. Load	min	typ	max	Condition
IOUT (Vafcf=0..5V, Vdd=5V)	1uF(no res)	-200uA	-	200uA	(not tested at product. test)
TST-OUT (ana. buffer output)	max. Load	min	typ	max	Condition
IOUT (Vtstout=0V)	10k//50pF	400uA	820uA	1.6mA	Vdd=5V
VREF (in normal mode) (Iout= +/-250uA)	10k//50pF	2,45	2,5	2,55	Vdd= 3.3...5.3V
AGND (resistive divider)	typ. Load	min	typ	max	Condition
VOUT	1uF(no res)	2.4	2.5	2.6	VDD=5.0V
M1M (current sink to VSS)	Load	min	typ	max	Condition
IOL (Vm=12V, 24V)	(see 1.2.3)	-0.5mA	-0.75mA	-1mA	TxMode
Ileak (Vm=0...24V)		-	-	10uA	RxMode
P1M (current source)	Load	min	typ	max	Condition
IOH (Vm=1V)	(see 1.2.3)	0.5mA	0.75mA	1mA	TxMode
VOL (Iout=1mA)		-	-	0.5V	RxMode
TxOut1, TxOut2 (current sink to VSS)	Load	min	typ	max	Condition
IOL (dc-component)	(see 1.2.3)	-1.9mA	-3.2mA	-5.2mA	TxMode
Ileak (Vin=0...24V)		-	-	10uA	RxMode

CKSYS, CLR/T, CD, RXD (dig. std. output)	min	typ	max	Condition
VOL (Iout=4mA)	-	0.25V	0.5V	-
VOH (Iout=-4mA)	VDD-0.5V	VDD-0.25V	-	-

SPI-OUT, RES (dig. open drain output)	min	typ	max	Condition
VOL (Iout = 4mA)	-	0.25V	0.5V	-
ILeak (Vout = 0...VDD)	-10uA	-	10uA	RES-pin
I pull-up (V=0V)	80uA	150uA	250uA	SPI-OUT pin

6.5 Reset -Test

	min	typ	max	Condition
Vpor_off_1 (res-th=VDD)	2.4V	2.5V	2.6V	TSTIN=VDD
Vpor_off_2 (res-th=floating)	3.65V	3.75V	3.90V	TSTIN=VDD
Vpor_hyst (res-th=floating)	50mV	100mV	150mV	TSTIN=VDD
Vpor_on_pwd (res-th=floating)	3.50V	3.65V	3.85V	TSTIN=VDD, PWD=H
Vpor_off_3 (res-th=VSS)	4.8V	5.0V	5.2V	TSTIN=VDD
Reset off-delay	1.1ms	0.3/256s	1.2ms	TestMode3 (pattern test)

6.6 CKTX -Test (pattern test)

ZC-Trigger Test included !	min	typ	max	Condition
Freq1(CLR/T)	-	600Hz	-	TxMode, BD1=L, BD2=L
Freq2(CLR/T)	-	1200Hz	-	TxMode, BD1=H, BD2=L
Freq3(CLR/T)	-	1200Hz	-	TxMode, BD1=L, BD2=H
Freq4(CLR/T)	-	2400Hz	-	TxMode, default

6.7 TX-Timeout Test

TestMode3: 3sec timeout divided by 256	min	typ	max	Condition
TxEn H=>L ... M1M/P1M-bias off	11.5ms	3/256sec	12.0ms	TestMode3 (pattern test)

6.8 PLL -Test (SCCLK)

Cafcf = 10nF Tsettle=5ms	min	typ	max	Condition
Freq1(CKSYS)	-0.8%	1.032MHz	+0.8%	TestMode2, MRK1-9=0, BD1=L
Freq2(CKSYS)	-0.8%	2.263MHz	+0.8%	TestMode2, MRK1-9=511, BD1=H
Freq3(CKSYS)	-0.8%	1.850MHz	+0.8%	TestMode2, MRK1-9=341, BD1=L
Freq4(CKSYS)	-0.8%	1.445MHz	+0.8%	TestMode2, MRK1-9=170, BD1=H
Phase Jitter	-	-	+/-50ns	TestMode2, M82

6.9 FSYNTH -Test (FMIXER)

	min	typ	max	Condition
Freq1(CKSYS)	-0.5%	66.9kHz	+0.5%	TestMode3, MRK1-9=0, BD1=L
Freq2(CKSYS)	-0.5%	146.55kHz	+0.5%	TestMode3, MRK1-9=511, BD1=H
Freq3(CKSYS)	-0.5%	118.05kHz	+0.5%	TestMode3, MRK1-9=341, BD1=L
Freq4(CKSYS)	-0.5%	95.4kHz	+0.5%	TestMode3, MRK1-9=170, BD1=H
Phase Jitter	-	-	+/-100ns	TestMode3, M82

6.10 TXOUT -Test

Testcircuit: (similar to the circuit shown on page 12)

VDD=5.0V	min	typ	max	Condition
Freq1(Vout)	-0.05%	81.75kHz	+0.05%	TxMode, M82, TXD=H
Freq2(Vout)	-0.05%	82.35kHz	+0.05%	TxMode, M82, TXD=L
Freq3(Vout)	-0.05%	82.95kHz	+0.05%	TxMode, M82,TXD=L,BD1=H
Freq4(Vout)	-0.05%	63.90kHz	+0.05%	TxMode, MRK1-9=0, TXD=H
Freq5(Vout)	-0.05%	140.55kHz	+0.05%	TxMode, MRK1-9=511, TXD=H
Freq6(Vout)	-0.05%	115.05kHz	+0.05%	TxMode, MRK1-9=341, TXD=H
Freq7(Vout)	-0.05%	89.40kHz	+0.05%	TxMode, MRK1-9=170, TXD=H
VppV24(Vout)	12Vpp	13.0Vpp	14Vpp	TxMode, M82,BD1=H,TXD=L/H
VppV12(Vout)	6.0Vpp	6.5Vpp	7.0Vpp	TxMode, M82,BD1=H,TXD=L/H

HD2(Vout)	-	-	-70dB	TxMode, M82, TXD=L
HD3(Vout)	-	-	-70dB	TxMode, M82, TXD=L
PSRR1(Vout)	15dB	-	-	TxMode, M82, VDD=200mVpp, 50Hz not tested, guaranteed by design
PSRR2(Vout)	35dB	-	-	TxMode,M82, VBUF=200mVpp, 50Hz not tested, guaranteed by design

6.11 RX AGC and FILTER Test

VDD = 5.0V, TxEn=H, TestMode2 input pin: RXIN, measured pin: TST-OUT	min	typ	max	Condition
Industrial Mode 72kHz dF=1.2kHz Bd=1.2k BW=6kHz				
abs. Gain @ 72kHz, 1.0Vrms	0.86Vp	1.0Vp	1.30Vp	M72
abs. Gain @ 72kHz, 100mVrms	0.86Vp	1.0Vp	1.15Vp	M72
abs. Gain @ 72kHz, 10mVrms	0.86Vp	1.0Vp	1.15Vp	M72
abs. Gain @ 72kHz, 3mVrms	380mVp	500mVp	660mVp	M72
rel. Gain @ 71.4kHz	-0.5dB	0.0dB	+0.5dB	M72
rel. Gain @ 72.6kHz	-0.5dB	0.0dB	+0.5dB	M72
rel. Gain @ 69kHz	-4dB	-3.0dB	-2dB	M72
rel. Gain @ 75kHz	-4dB	-3.0dB	-2dB	M72
rel. Gain @ 42kHz	-	-	-45dB	M72
rel. Gain @ 124kHz	-	-	-45dB	M72
Domestic Mode 82.05kHz dF=600Hz Bd=600 BW=3k				
abs. Gain @ 82.05kHz, 1.0Vrms	0.86Vp	1.0Vp	1.15Vp	M82
rel. Gain @ 81.75kHz	-0.5dB	0.0dB	+0.5dB	M82
rel. Gain @ 82.35kHz	-0.5dB	0.0dB	+0.5dB	M82
rel. Gain @ 80.55kHz	-4dB	-3.0dB	-2dB	M82
rel. Gain @ 83.55kHz	-4dB	-3.0dB	-2dB	M82
rel. Gain @ 55kHz	-	-	-45dB	M82
rel. Gain @ 123kHz	-	-	-45dB	M82
Home Automation 132.45kHz dF=1.2kHz Bd=2.4k BW=4.8kHz				
abs. Gain @ 132.45kHz, 1.0Vrms	0.86Vp	1.0Vp	1.15Vp	M132
rel. Gain @ 131.85kHz	-0.5dB	0.0dB	+0.5dB	M132
rel. Gain @ 133.05kHz	-0.6dB	0.0dB	+0.5dB	M132
rel. Gain @ 130.05kHz	-4dB	-3.0dB	-2dB	M132
rel. Gain @ 134.85kHz	-4.5dB	-3.0dB	-2dB	M132
rel. Gain @ 88kHz	-	-	-45dB	M132
rel. Gain @ 198kHz	-	-	-45dB	M132

6.12 IF-FILTER Test

VDD=5.0V input: TST_IN, output: TST_OUT	min	typ	max	Condition
abs. Gain @ 2.7kHz Vin: tbd	-1.0dB	0.0dB	+1.0dB	BD1=L, TestMode1
rel. Gain @ 1.2kHz	-	-	-45dB	BD1=L, TestMode1
rel. Gain @ 2.1kHz	-4dB	-3.0dB	-2dB	BD1=L, TestMode1
rel. Gain @ 3.3kHz	-4dB	-3.0dB	-2dB	BD1=L, TestMode1
rel. Gain @ 5.8kHz	-	-	-45dB	BD1=L, TestMode1
abs. Gain @ 5.4kHz Vin: tbd	-1.0dB	0.0dB	+1.0dB	BD1=H, TestMode1
rel. Gain @ 2.4kHz	-	-	-45dB	BD1=H, TestMode1
rel. Gain @ 4.2kHz	-4dB	-3.0dB	-2dB	BD1=H, TestMode1
rel. Gain @ 6.6kHz	-4dB	-3.0dB	-2dB	BD1=H, TestMode1
rel. Gain @ 11.6kHz	-	-	-45dB	BD1=H, TestMode1

6.13 RXD-Distortion Test

A fsk-signal with a bit-stream of 010101... will be forced to the TxFb-Pin. The asynchronous RXD-signal (ASYN=H) will be measured. This test will indirectly cover the Bit Error Rate requirements.

VDD=5.0V, ASYN=H 72kHz, dF=1200Hz, 1200baud input: RXIN, output: RXD	**min**	**typ**	**max**	**Condition**
Bias Distortion @ Vin=1.5Vrms	-	-	8%	M72
Isochr. Distortion @ Vin=1.5Vrms	-	-	12%	M72
Bias Distortion @ Vin=3.0mVrms	-	-	8%	M72
Isochr. Distortion @ Vin=3.0mVrms	-	-	18%	M72
82.05kHz, dF=600Hz, 600baud input: RXIN, output: RXD				
Bias Distortion @ Vin=1.5Vrms	-	-	8%	M82
Isochr. Distortion @ Vin=1.5Vrms	-	-	14%	M82
Bias Distortion @ Vin=3.0mVrms	-	-	10%	M82
Isochr. Distortion @ Vin=3.0mVrms	-	-	25%	M82
132.45kHz, dF=1200Hz, 2400baud input: RXIN, output: RXD				
Bias Distortion @ Vin=1.5Vrms	-	-	12%	M132
Isochr. Distortion @ Vin=1.5Vrms	-	-	22%	M132
Bias Distortion @ Vin=3.0mVrms	-	-	14%	M132
Isochr. Distortion @ Vin=3.0mVrms	-	-	30%	M132

Isochr. Distortion @ Vin=3.0mVrms will not be tested at low temperature !

6.14 Carrier Detect - Test

VDD=5.0V, input: RXIN, output: CD	min	typ	max	Condition
VIN_on (CD=H, Fin=82.05kHz)	-	-	4.9mVeff	M82
VIN_off (CD=L, Fin=82.05kHz)	2.9mVeff	-	-	M82
Tattack1 (CD=>H @ Vin=4.9mVrms, 82.05kHz)	8.0ms	8.33ms	9.0ms	M82, FCDON=H
Tattack2 (CD=>H @ Vin=4.9mVrms,132.45kHz)	4.0ms	4.17ms	4.5ms	M132, FCDON=L
Tattack3 (CD=>H @ Vin=4.9mVrms,132.45kHz)	1.9ms	2.08ms	2.5ms	M132, FCDON=H
Trelease1 (CD =>L @ Vin=1.5Vrms, 82.05kHz)	8.0ms	-	9.0ms	M82
Trelease2 (CD=>H @ Vin=1.5Vrms, 82.05kHz)	4.0ms	-	5.0ms	M82, BD1,2=H,L
Trelease3 (CD=>H @ Vin=1.5Vrms, 82.05kHz)	1.9ms	-	2.5ms	M82, BD1,2=H,H

6.15 CKRX - Test (pattern test)

The DPLL of the Rx-clock recovery circuit will be tested by a digital pattern defined during design-phase. In Test-Mode 3 a certain DPLL-input will be supplied by the pin TST-IN. The CLR/T has to recover a minimum of 20% jitter and a frequency tolerance of +/-1.5%.

6.16 Serial Interface - Test (pattern test)

The serial interface will be tested by a digital pattern defined during design-phase.

	min	typ	max	Condition
Tspick	1us	-	-	-
Tcssu, Tcshd	200ns	-	-	-
Tdsu, Tdhd	100ns	-	-	-