# *TOPSwitch*®*-FX* Flyback Design Methodology

## Application Note AN-25

This application note introduces a simple methodology for the design of off-line flyback power supplies using the *TOPSwitch-FX* family. It is fundamentally the same as AN-16, "*TOPSwitch* Flyback Design Methodology", which was intended for *TOPSwitch* and *TOPSwitch-II* families. Several modifications reflect the features of *TOPSwitch-FX*. In addition to addressing basic design issues specific to *TOPSwitch-FX*, many other general enhancements over AN-16 were also implemented. A brief summary of the major differences between this document and AN-16 is provided in Appendix B as a quick reference for readers already familiar with AN-16.

## Introduction

The design of a switching power supply, by nature, is an iterative process with many variables that have to be adjusted to optimize the design. The design method described in this document consists of two major sections: The design flow chart and the step-by-step design procedure. The flow chart shows design sequence at conceptual level for *TOPSwitch-FX* flyback power supply design. The step-by-step procedure gives details within each step of the design flow chart including rules of thumb and look up tables. All key equations and guidelines are provided wherever possible to assist the readers in better understanding and/or further optimization.

### Basic Circuit Configuration

Because of the high level integration of *TOPSwitch-FX*, many power supply design issues are resolved in the chip. Far fewer issues are left to be addressed externally, resulting in one common circuit configuration for all applications. Different output power levels may require different values of some circuit components, but the circuit configuration stays unchanged. *TOPSwitch-FX* is a feature rich product family. Advanced features like Under-Voltage, Over-Voltage, External $I_{LIMIT}$, Line Feed Forward, Remote ON/OFF are easily implemented with a minimal number of external components, but do require additional design considerations. Please refer to the *TOPSwitch-FX* data sheet for details. Other application specific issues such as constant current, constant power outputs, etc. are beyond the scope of this application note. However, such requirements may be satisfied by adding additional circuitry to the basic converter configuration. The only part of the circuit configuration that may change from application to application is the feedback circuitry. Depending on the power supply output requirement, one of the two feedback circuits, shown in Figures 3 and 4, will be chosen for the application.

The basic circuit configuration used in *TOPSwitch-FX* flyback power supplies is shown in Figure 1, which also serves as the

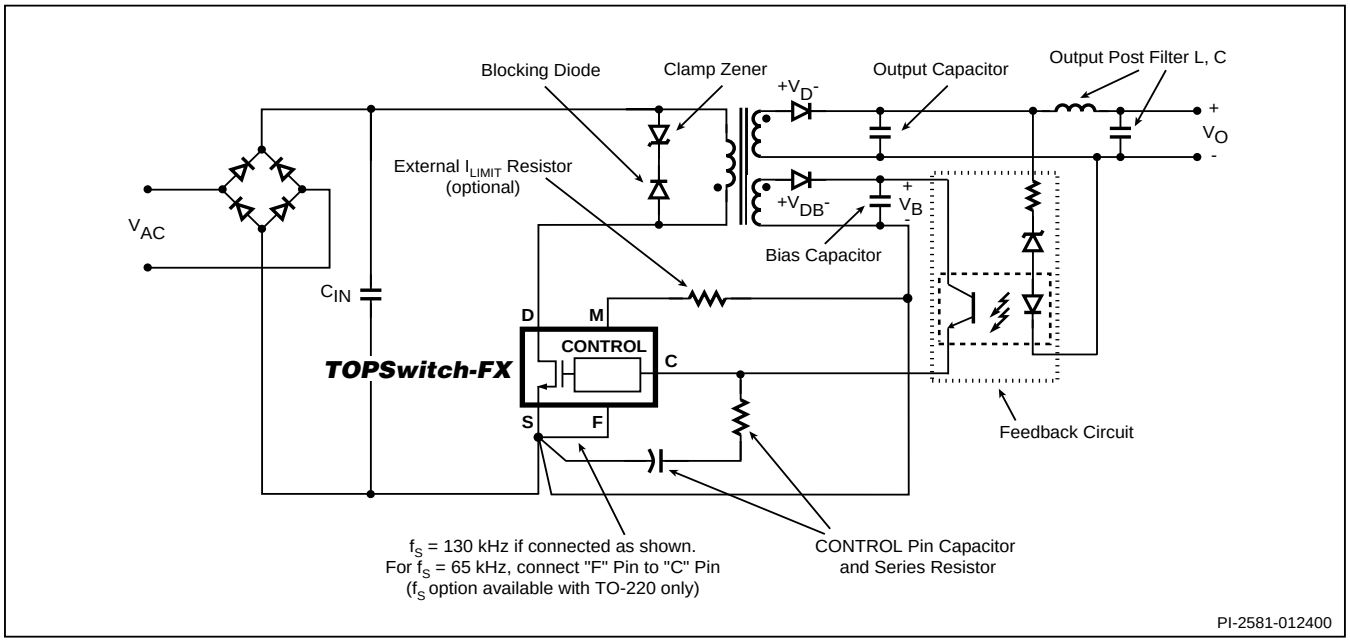


*Figure 1. Typical TOPSwitch-FX Flyback Power Supply.*

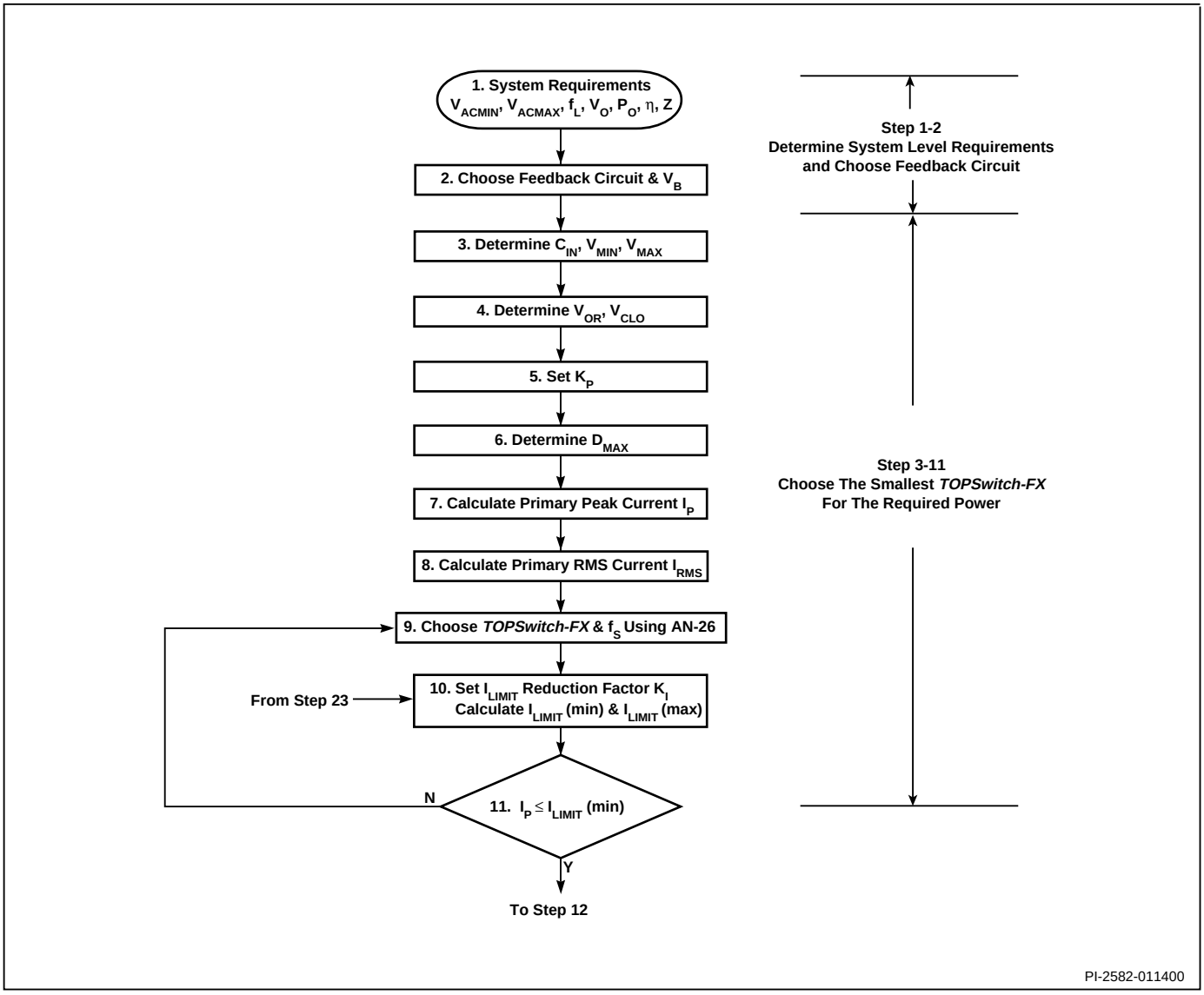


*Figure 2A. TOPSwitch-FX Design Flow Chart. Step 1 to 11.*

reference circuit for component identifications used in the description through out this application note.

## Design Flow

Figures 2A, 2B and 2C present a design flow chart showing the complete design procedure in 37 steps. With the basic circuit configuration shown in Figure 1 as its foundation, the logic behind this design approach can be summarized as following:

1. Determine system requirements and decide on feedback circuit accordingly.
2. Choose the smallest *TOPSwitch-FX* capable for the required output power.
3. Design the smallest transformer for the *TOPSwitch-FX* chosen.
4. Select all other components in Figure 1 to complete the design.

The overriding objective of this procedure is “design for cost effectiveness”. Using smaller components usually leads to a less expensive power supply. However, for applications with stringent size or weight limitations, the designer may need to strike a compromise between cost and specific design requirements in order to achieve the optimum cost effectiveness for the end product.

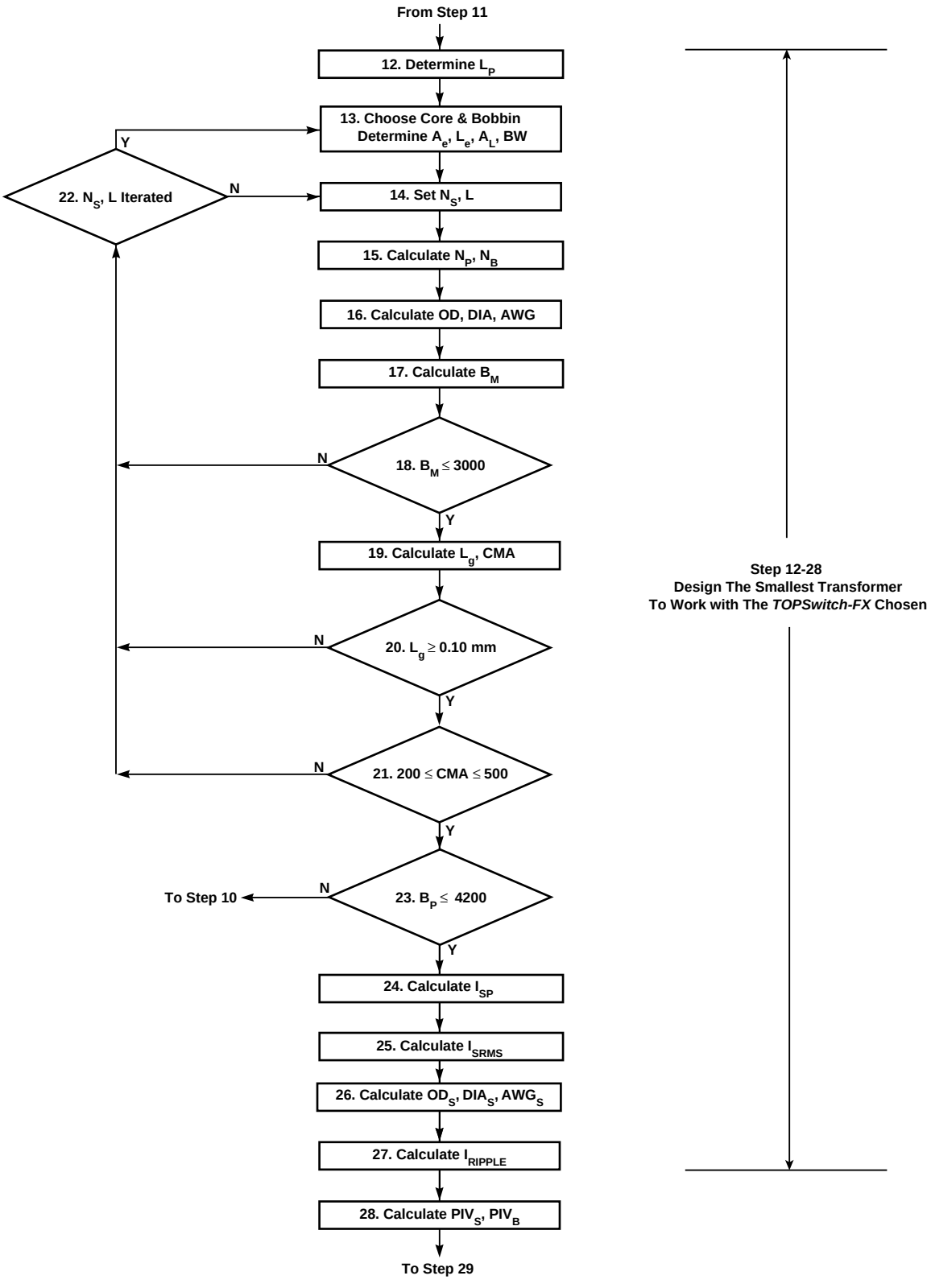


*Figure 2B. TOPSwitch-FX Design Flow Chart. Step 12 to 28.*

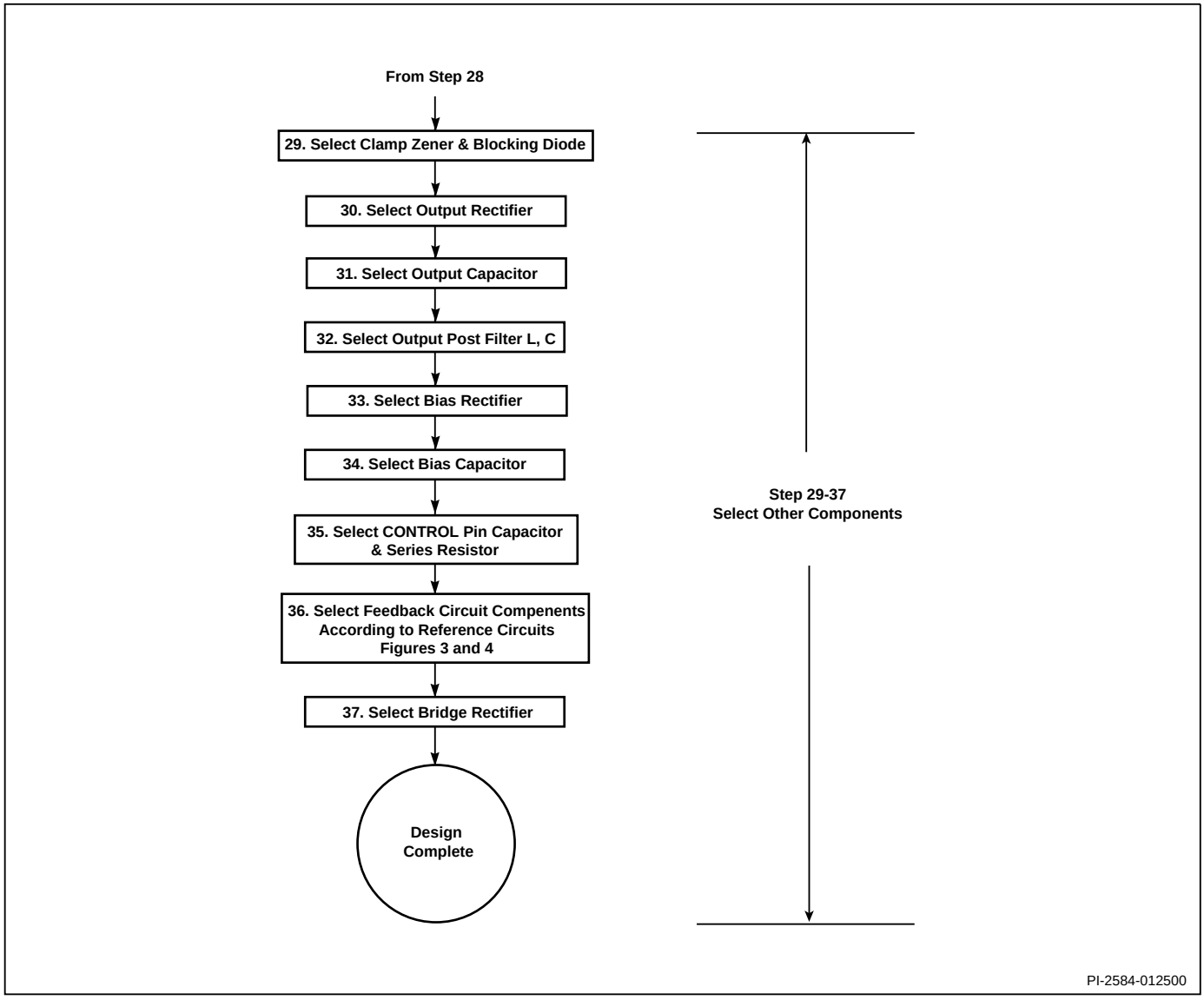


*Figure 2C. TOPSwitch-FX Design Flow Chart. Step 29 to 37.*

## Step by Step Design Procedure

This design procedure uses the *TOPSwitch-FX* continuous/discontinuous flyback design spreadsheet (available from Power Integrations) which contains all the important equations required for a *TOPSwitch-FX* flyback power supply design, and automates most calculations. Designers are, therefore, relieved from the tedious calculations involved in the complicated and highly iterative design process. Note that all user provided inputs are in column B and all spreadsheet calculated results are in column D. Column C is reserved for intermediate variables needed in some complicated calculations. Look up tables and rules of thumb are provided where appropriate to facilitate the design task.

**Step 1. Determine system requirements: $V_{ACMAX}$, $V_{ACMIN}$, $f_L$, $V_O$, $P_O$, $\eta$, Z**

- Minimum AC input voltage, $V_{ACMIN}$: in Volts.
- Maximum AC input voltage, $V_{ACMAX}$: in Volts.
- Recommended AC input ranges:

| Input (VAC) | $V_{ACMIN}$ (VAC) | $V_{ACMAX}$ (VAC) |
|---|---|---|
| Universal | 85 | 265 |
| 230 or 115 with doubler | 195 | 265 |

*Table 1*

- Line frequency, $f_L$: 50 Hz or 60 Hz.
- Output voltage, $V_O$: in Volts.
- Output power: $P_O$: in Watts.
- Power supply efficiency, $\eta$: 0.8 if no better reference data available. (Refer to AN-26)
- Loss allocation factor, Z: If Z = 1, all losses are on the secondary side. If Z = 0, all losses are on the primary side. Set Z = 0.5 if no better reference data available.

**Step 2. Choose feedback circuit and bias voltage $V_B$ based on output requirements**

| Feedback Circuit | $V_B$ (V) | Output Accuracy | Load* Reg. | Line Reg. | Ref. Circuit |
|---|---|---|---|---|---|
| Opto/Zener | 15 | ± 5% | ± 1% | ± 0.5% | Figure 3 |
| Opto/TL431 | 15 | ± 1% | ± 0.2% | ± 0.2% | Figure 4 |

**Over 10% to 100% Load Range.*
*Table 2*

- Use Opto/Zener for lower cost.
- Use Opto/TL431 for better performance.
- Although not included in Table 2, primary feedback may also be used with *TOPSwitch-FX* design.
- Bias voltage $V_B$: 15 V recommended. May be set to different value if needed.

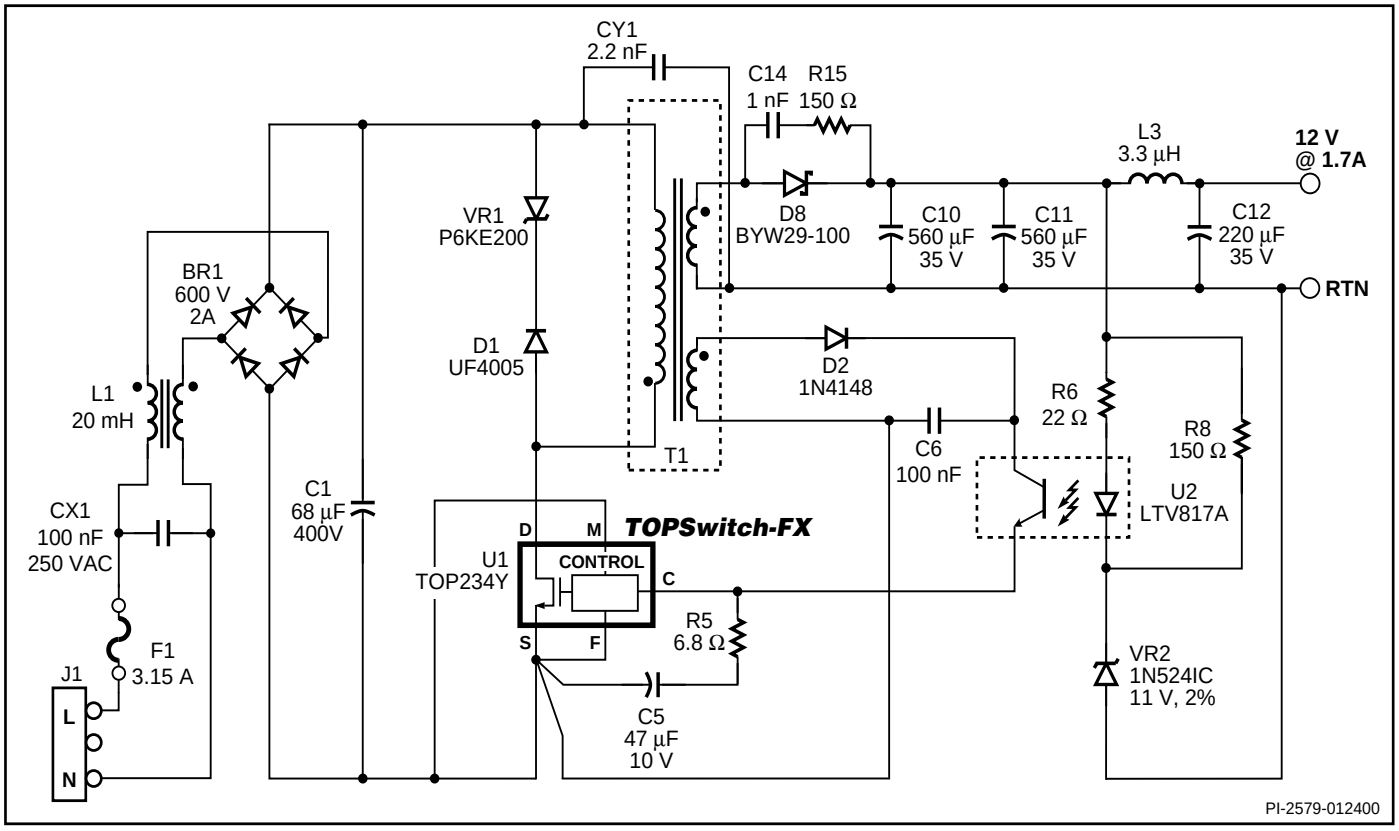


*Figure 3. Opto/Zener Feedback Reference Circuit.*

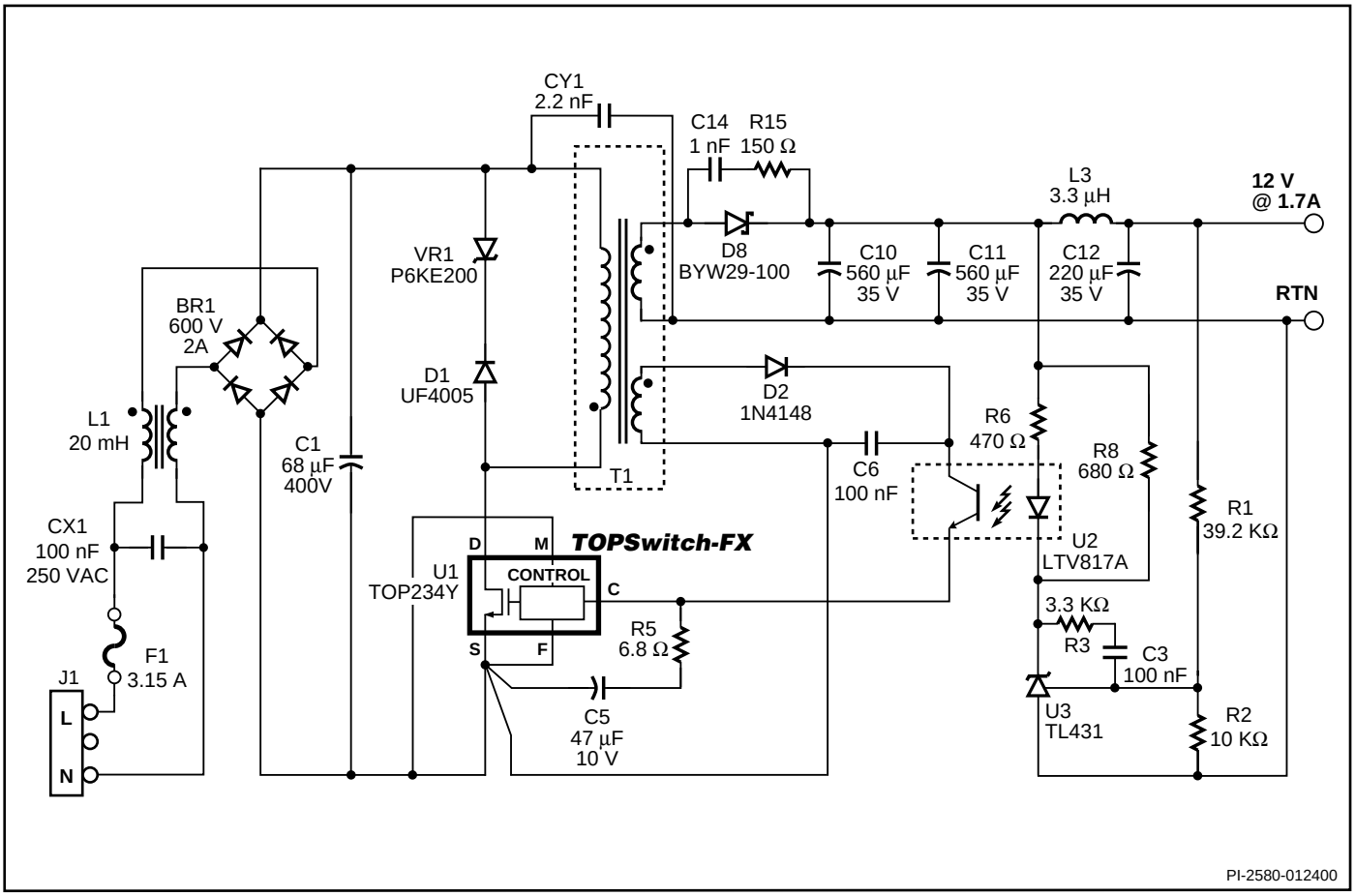


*Figure 4. Opto/TL431 Feedback Reference Circuit.*

**Step 3. Determine minimum and maximum DC input voltages $V_{MIN}$, $V_{MAX}$ and input storage capacitance $C_{IN}$ based on AC input voltage and $P_O$ (Figure 5)**

- Choose input storage capacitor, $C_{IN}$ per Table 3.

| Input (VAC) | $C_{IN}$ (µF/Watt of $P_O$) | $V_{MIN}$ (V) |
|---|---|---|
| Universal | 2 ~ 3 | ≥ 90 |
| 230 or 115 with doubler | 1 | ≥ 240 |

*Table 3*

- Set bridge rectifier conduction time, $t_C$ = 3 ms.
- Derive minimum DC input voltage $V_{MIN}$

$$V_{MIN}=\sqrt{(2\times V_{ACMIN}{}^2)-\frac{2\times P_O\times\left(\frac{1}{2\times f_L}-t_C\right)}{\eta\times C_{IN}}}$$

where units are volts, watts, Hz, seconds and farads

- Calculate maximum DC input voltage $V_{MAX}$:

$$V_{MAX}=\sqrt{2}\times V_{ACMAX}$$

**Step 4. Determine reflected output voltage $V_{OR}$ and clamp Zener voltage $V_{CLO}$ based on input voltage (Figure 6)**

- Set reflected output voltage, $V_{OR}$ = 135 V.
- Use 200 V clamp Zener, $V_{CLO}$ = 200 V.
- RCD (Resistor/Capacitor/Diode) clamp may be used with *TOPSwitch-FX* for increased $V_{OR}$ and wider $D_{MAX}$ when and only when current limit is set externally with current limit reduction as a function of line voltage. Compared to Zener clamp, designs using RCD clamp usually have slightly lower efficiency at light load. In addition, great care must be taken in RCD clamp design. Because of its inherent variation in clamp voltage over load range, if not designed properly, RCD clamp may fail to protect *TOPSwitch-FX*, especially under startup or output overload conditions.

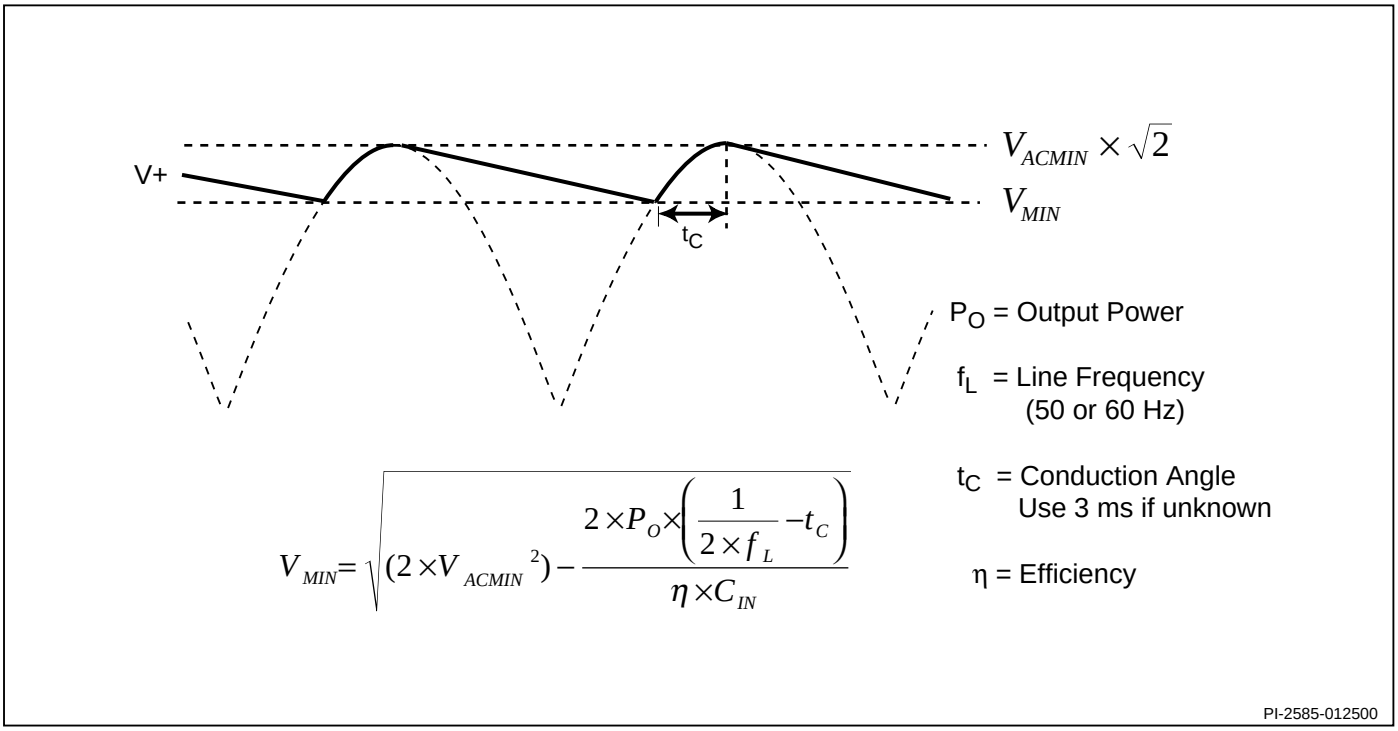


*Figure 5. Input Voltage Waveform.*

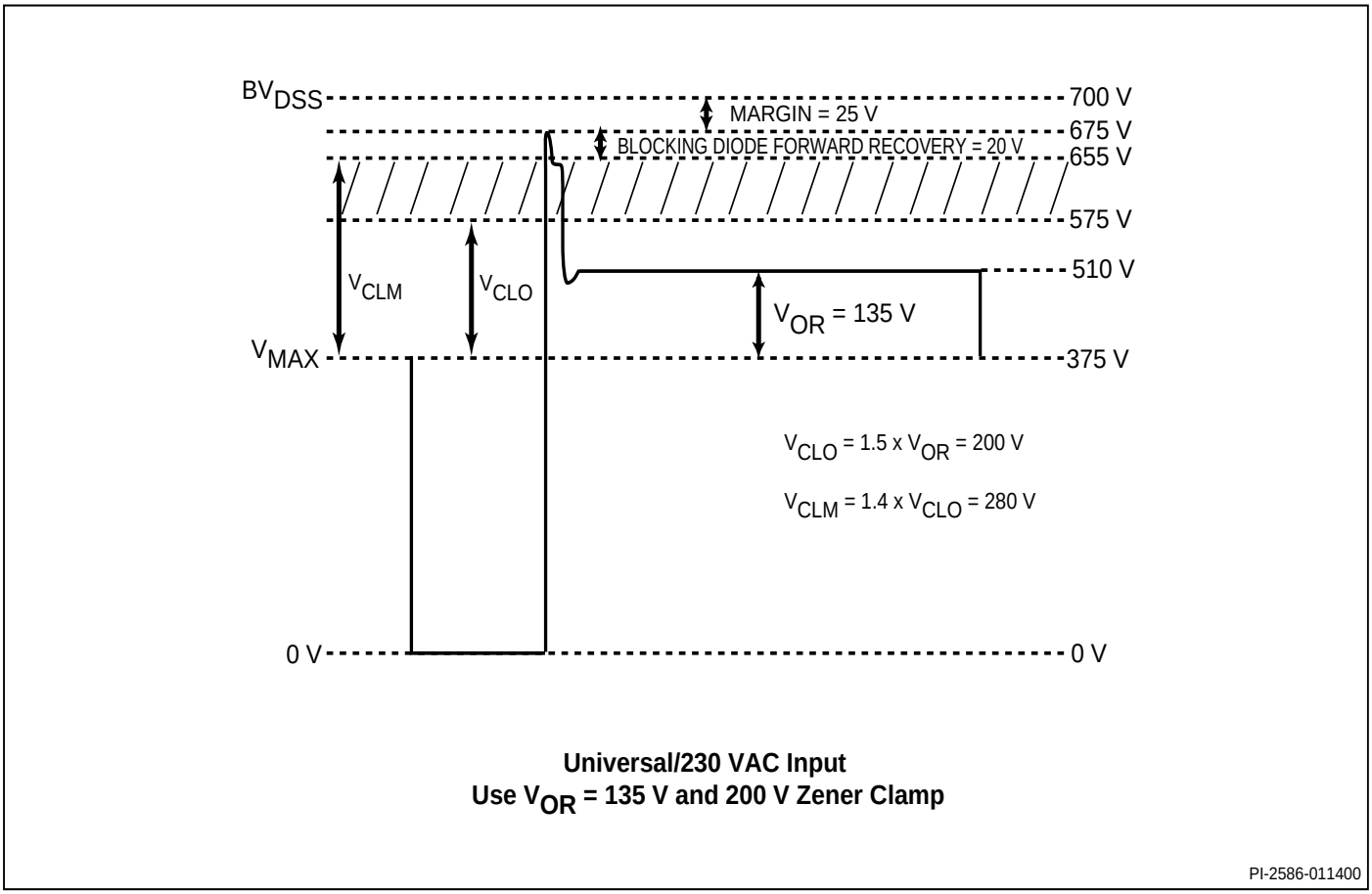


*Figure 6. Reflected Voltage $V_{OR}$ and Clamp Zener Voltage $V_{CLO}$.*

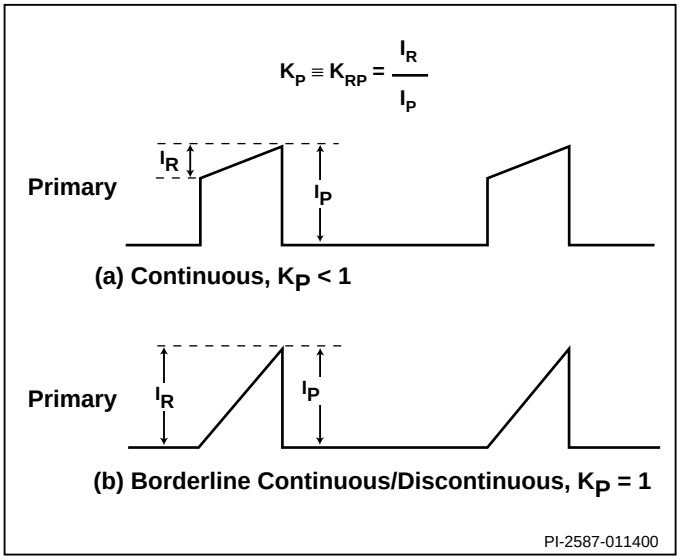


*Figure 7. Continuous Mode Current Waveform, $K_P \leq 1$.*

**Step 5. Set primary current waveform parameter $K_P$ for desired mode of operation and current waveform: $K_P \equiv K_{RP}$ for $K_P \leq 1.0$ and $K_P \equiv K_{DP}$ for $K_P \geq 1.0$ (Figures 7 & 8)**

- For $K_p \leq 1.0$, $K_p \equiv K_{RP}$, continuous mode (see Figure 7)

$$K_P \equiv K_{RP} = \frac{I_R}{I_P}$$ where $I_R$ is primary ripple current and $I_p$ is primary peak current.

- For $K_p \geq 1.0$, $K_p \equiv K_{DP}$, discontinuous mode (see Figure 8)

$$K_P \equiv K_{DP} = \frac{V_{OR} \times (1 - D_{MAX})}{(V_{MIN} - V_{DS}) \times D_{MAX}}$$

- For continuous mode design, set
  $K_p$ = 0.4 for universal input
  0.6 for 230 VAC or 115 VAC with doubler.
- For discontinuous mode design, set $K_p$ = 1.0.
- $K_p$ must be kept within the range specified in Table 4.

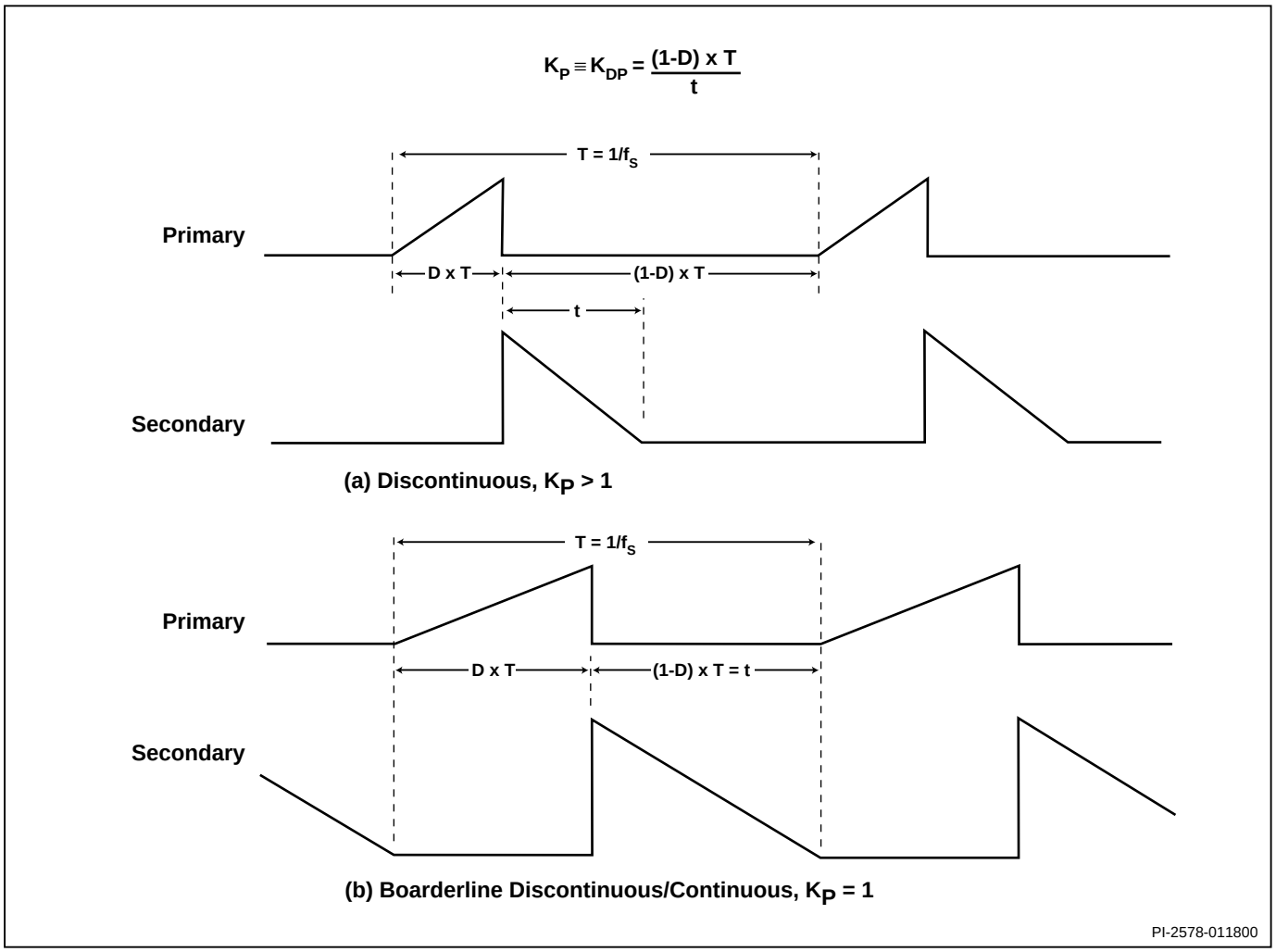


*Figure 8. Discontinuous Mode Current Waveform, $K_P \geq 1$.*

| Input (VAC) | $K_P$ | |
|---|---|---|
| | Continuous Mode | Discontinuous Mode |
| Universal | 0.4~1.0 | ≥1.0 |
| 230 | 0.6~1.0 | ≥1.0 |

*Table 4*

**Step 6. Determine $D_{MAX}$ based on $V_{MIN}$ and $V_{OR}$**

- Continuous mode

$$D_{MAX}=\frac{V_{OR}}{(V_{MIN}-V_{DS})+V_{OR}}$$

- Discontinuous mode

$$D_{MAX}=\frac{V_{OR}}{K_P\times(V_{MIN}-V_{DS})+V_{OR}}$$

- Set *TOPSwitch-FX* Drain to Source voltage, $V_{DS}$ = 10 V.

**Step 7. Calculate primary peak current $I_P$**

- Continuous mode ($K_P \le 1.0$)

$$I_P=\frac{I_{AVG}}{\left(1-\frac{K_P}{2}\right)\times D_{MAX}}$$

- Discontinuous mode ($K_P \ge 1.0$)

$$I_P=\frac{2\times I_{AVG}}{D_{MAX}}$$

- Input average current $I_{AVG}=\frac{P_O}{\eta\times V_{MIN}}$

**Step 8. Calculate primary RMS current $I_{RMS}$**

- Continuous mode

$$I_{RMS}=I_P\times\sqrt{D_{MAX}\times\left(\frac{K_P^{\,2}}{3}-K_P+1\right)}$$

- Discontinuous mode

$$I_{RMS}=\sqrt{D_{MAX}\times\frac{I_P^{\,2}}{3}}$$

**Step 9. Choose *TOPSwitch-FX* based on AC input voltage, $P_O$ and η using AN-26 selection curves**

- Choose the smallest *TOPSwitch-FX* using *TOPSwitch-FX* Selection Curves in AN-26.
- Identify appropriate selection curves according to AC input voltage.
- Continuous mode: Use selection curves as is.
- Discontinuous mode: Use selection curves with the output power derated by 33%. This effectively makes a 10 W discontinuous design equivalent to a 15 W continuous design in *TOPSwitch-FX* selection.
- Switching Frequency $f_S$: For DIP and SMP packages, set $f_S$ = 130 kHz. For TO-220 package, choose between 65 kHz and 130 kHz.

**Step 10. Set $I_{LIMIT}$ reduction factor $K_I$ for External $I_{LIMIT}$**

- $K_I=\frac{external\ I_{LIMIT}}{default\ I_{LIMIT}}$ where $0.4 \le K_I \le 1.0$
- $K_I$ is set by the value of the resistor connected between M pin and SOURCE pin (Refer to *TOPSwitch-FX* data sheet).
- For applications demanding very high efficiency, a *TOPSwitch-FX* bigger than necessary may be used by lowering $I_{LIMIT}$ externally to take advantage of the lower $R_{DS(ON)}$.
- If no special requirement, set $K_I$ = 1.0.
- Calculate $I_{LIMIT}$(min) and $I_{LIMIT}$(max)

$$I_{LIMIT}(\min)=default\ I_{LIMIT}(\min)\times K_I$$

$$I_{LIMIT}(\max)=default\ I_{LIMIT}(\max)\times K_I$$

**Step 11. Validate *TOPSwitch-FX* selection by checking $I_P$ against $I_{LIMIT}$(min)**

- For $K_I$ = 1.0, check $I_P \le 0.96$ x $I_{LIMIT}$(min).
- For $K_I$ < 1.0, check $I_P \le 0.94$ x $I_{LIMIT}$(min).
- Choose larger *TOPSwitch-FX* if necessary.

**Step 12. Calculate primary inductance $L_P$**

- Continuous mode

$$L_P=\frac{10^6\times P_O}{I_P^{\,2}\times K_P\times\left(1-\frac{K_P}{2}\right)\times f_S(\min)}\times\frac{Z\times(1-\eta)+\eta}{\eta}$$

where units are μH, watts, amps and Hz

• Discontinuous mode.

$$L_P = \frac{10^6 \times P_O}{I_P{}^2 \times \frac{1}{2} \times f_S(\min)} \times \frac{Z \times (1-\eta) + \eta}{\eta}$$

where units are μH, watts, amps and Hz

• Z is loss allocation factor and η is efficiency from Step 1.

**Step 13. Choose core and bobbin based on $f_S$ and $P_O$ using Table 5 and determine $A_e$, $L_e$, $A_L$ and BW from core and bobbin catalog**

• Core effective cross sectional area, $A_e$: in $cm^2$.
• Core effective path length, $L_e$: in cm.
• Core ungapped effective inductance, $A_L$: in $nH/turn^2$.
• Bobbin width, BW: in mm.
• Choose core and bobbin based on $f_S$, $P_O$ and construction type.

| Output Power | 65 kHz | | 130 kHz | |
|---|---|---|---|---|
| | Triple Insulated Wire | Margin Wound | Triple Insulated Wire | Margin Wound |
| 0-10 W | EFD15<br>EF16<br>EE16<br>EE22<br>EFD20<br>EE19 | EEL16<br>EF20<br>EEL19 | EFD15<br>EF16<br>EE16 | EEL16 |
| 10-20 W | EF20<br>EI25<br>E24/25<br>EI30 | EFD25<br>EF25<br>EFD30<br>EF20 | EE22<br>EFD20<br>EE19 | EF20<br>EEL19 |
| 20-30 W | EF25<br>EI28 | EER28<br>EF30 | EI25<br>E24/25 | EFD25<br>EF25 |
| 30-50 W | EI30<br>EF30<br>EER28<br>ETD29<br>EER28L | ETD29<br>EER28L<br>ETD34 | EF25<br>EI28 | EFD30<br>EI30<br>EER28<br>EF30 |
| 50-70 W | EI35<br>ETD34 | EI40<br>EER35<br>EER28 | EI30<br>EF30 | ETD29<br>EER28L |
| 70-100 W | EI40<br>EER35 | ETD39<br>EER40<br>EI35<br>ETD34<br>EI40<br>EER35 | ETD29<br>EER28L<br>EER35<br>ETD39<br>EER40 | ETD34<br>EI40 |

*Table 5.*

**Step 14. Set value for number of primary layers L and number of secondary turns $N_S$ (may need iteration)**

• Starting with L = 2 (Keep 1.0 ≤ L ≤ 2.0 through out iteration).
• Starting with $N_S$ = 0.6 turn/volt.
• Both L and $N_S$ may need iteration.

**Step 15. Calculate number of primary turns $N_P$ and number of bias turns $N_B$**

• Diode forward voltages: 1.0 V for fast P/N diode, 0.7 V for ultra fast P/N diode and 0.5 V for Schottky diode.
• Set output rectifier forward voltage, $V_D$.
• Set bias rectifier forward voltage, $V_{DB}$.
• Calculate number of primary turns.

$$N_P = N_S \times \frac{V_{OR}}{V_O + V_D}$$

• Calculate number of bias turns $N_B$.

$$N_B = N_S \times \frac{V_B + V_{DB}}{V_O + V_D}$$

**Step 16. Determine primary winding wire parameters OD, DIA, AWG**

• Primary wire outside diameter in mm.

$$OD = \frac{L \times (BW - 2 \times M)}{N_P}$$

where L is number of primary layers,
BW is bobbin width in mm,
M is safety margin in mm.

• Determine primary wire bare conductor diameter DIA and primary wire gauge AWG.

**Step 17 to Step 22. Check $B_M$, CMA and $L_g$. Iterate if necessary by changing L, $N_S$ or core/bobbin until within specified range**

• Set safety margin, M. Use 3 mm (118 mils) for margin wound and zero for triple insulated secondary.
• Maximum flux density: 3000 ≥ $B_M$ ≥ 2000; in gauss.

$$B_M = \frac{100 \times I_P \times L_P}{N_P \times A_e}$$

where units are gauss, amps, μH and $cm^2$

• Gap length in mm: $L_g \geq 0.1$

$$L_g = 40 \times \pi \times A_e \times \left( \frac{N_P{}^2}{1000 \times L_P} - \frac{1}{A_L} \right)$$

where $L_g$ in mm, $A_e$ in cm$^2$, $A_L$ in nH/turn$^2$ and $L_P$ in µH

• Primary winding current capacity in circular mils per amp: $500 \geq CMA \geq 200$

$$CMA = \frac{1.27 \times DIA^2 \times \frac{\pi}{4}}{I_{RMS}} \times \left( \frac{1000}{25.4} \right)^2$$

where DIA is the bare conductor diameter in mm

• Iterate by changing L, $N_S$, core/bobbin according to Table 6.

| | | $B_M$ | $L_g$ | CMA |
|---|---|---|---|---|
| L | ↑ | - | - | ↑ |
| $N_S$ | ↑ | ↓ | ↑ | ↓ |
| core size | ↑ | ↓ | ↑ | ↑ |

*Table 6*

**Step 23. Check $B_P \leq 4200$ . If necessary, reduce current limit by lowering $I_{LIMIT}$ reduction factor $K_I$**

• $B_P = \frac{I_{LIMIT}(\max)}{I_P} \times B_M$

• Check $B_P \leq 4200$ gauss to avoid transformer saturation at startup and output over load.

• Decrease $K_I$ if necessary until $B_P \leq 4200$.

**Step 24. Calculate secondary peak current $I_{SP}$**

• $I_{SP} = I_P \times \frac{N_P}{N_S}$

**Step 25. Calculate secondary RMS current $I_{SRMS}$**

• Continuous mode

$$I_{SRMS} = I_{SP} \times \sqrt{(1 - D_{MAX}) \times \left( \frac{K_P{}^2}{3} - K_P + 1 \right)}$$

• Discontinuous mode

$$I_{SRMS} = I_{SP} \times \sqrt{\frac{1 - D_{MAX}}{3 \times K_P}}$$

**Step 26. Determine secondary winding wire parameters $OD_S$, $DIA_S$, $AWG_S$**

• Secondary wire outside diameter in mm

$$OD_S = \frac{BW - (2 \times M)}{N_S}$$

• Secondary wire bare conductor diameter in mm

$$DIA_S = \sqrt{\frac{4 \times CMA_S \times I_{SRMS}}{1.27 \times \pi}} \times \frac{25.4}{1000}$$

where $CMA_S$ is secondary winding current capacity in circular mils per amp. Minimum wire diameter is calculated by using a $CMA_S$ of 200.

• Determine secondary winding wire gauge $AWG_S$ based on $DIA_S$. If the bare conductor diameter of the wire is larger than that of the 27 AWG for 130 kHz or 25 AWG for 65 kHz, a parallel winding using multiple strands of thinner wire should be used to minimize skin effect.

**Step 27. Determine output capacitor ripple current $I_{RIPPLE}$**

• Output capacitor ripple current

$$I_{RIPPLE} = \sqrt{I_{SRMS}{}^2 - I_O{}^2}$$

where $I_O$ is the output DC current

**Step 28. Determine maximum peak inverse voltages $PIV_S$, $PIV_B$ for secondary and bias windings**

• Secondary winding maximum peak inverse voltage.

$$PIV_S = V_O + (V_{MAX} \times \frac{N_S}{N_P})$$

• Bias winding maximum peak inverse voltage.

$$PIV_B = V_B + (V_{MAX} \times \frac{N_B}{N_P})$$

**Step 29. Select clamp Zener and blocking diode for primary clamping based on input voltage and $V_{CLO}$**

• Use 200 V Zener such as Motorola P6KE200 for the clamp.

• Use ultra fast diode such as General Instruments UF4005 for the blocking diode.

**Step 30. Select output rectifier**

• $V_R \geq 1.25$ x $PIV_S$; where $PIV_S$ is from Step 28 and $V_R$ is the rated reverse voltage of the rectifier diode.

• $I_D \geq 3$ x $I_O$; where $I_D$ is the diode rated DC current and $I_O = P_O/V_O$.

**Step 31. Select output capacitor**

- Ripple current specification at 105 ˚C, 100 kHz: Must be equal to or larger than $I_{RIPPLE,}$ where $I_{RIPPLE}$ is from Step 27.
- ESR specification: Use low ESR, electrolytic capacitor. Output switching ripple voltage is $I_{SP}$ x ESR , where $I_{SP}$ is from Step 24.

**Step 32. Select output post filter L, C**

- Inductor L: 2.2 to 4.7 uH. Use bead for low current (≤ 1A) output and standard off-the-shelf choke for higher current output. Increase choke current rating or wire size if necessary to avoid significant DC voltage drop.
- Capacitor C: 120 uF, 35 V, low ESR, electrolytic capacitor.

**Step 33. Select bias rectifier**

- $V_R \geq 1.25$ x $PIV_B$; where $PIV_B$ is from Step 28 and $V_R$ is the rated reverse voltage of the rectifier diode.

**Step 34. Select bias capacitor**

- Use 0.1 uF, 50 V, ceramic.

**Step 35. Select CONTROL pin capacitor and series resistor**

- CONTROL pin capacitor: 47 uF, 10 V, low cost electrolytic (Do not use low ESR capacitor).
- Series resistor: 6.2 ohm, 1/4 W (Not needed if $K_P \geq 1$, i.e. discontinuous mode).

**Step 36. Select feedback circuit components according to applicable reference circuits shown in Figures 3 and 4**

- Applicable reference circuit: Identified in Step 2.

**Step 37. Select input bridge rectifier**

- $V_R \geq 1.25$ x $\sqrt{2}$ x $V_{ACMAX}$; where $V_{ACMAX}$ is from Step 1.
- $I_{ACRMS} \geq 2$ x $I_D$; where $I_D$ is the bridge rectifier rated RMS current and $I_{ACRMS}$ is the input RMS current.

  Note: $I_{ACRMS} = \frac{P_O}{\eta \times V_{ACMIN} \times PF}$ ;where $V_{ACMIN}$ is from Step 1 and PF is the power factor of the power supply which is typically between 0.5 and 0.7. If no better reference information available, use PF = 0.5.

# Appendix A

## Multiple Output Flyback Power Supply Design

The only difference between a multiple output flyback power supply and a single output flyback power supply of the same total output power is in the secondary side design. Instead of delivering all power to one output as in single output case, a multiple output flyback distributes its output power among several outputs. Therefore, the design procedure for the primary side stays the same while that for the secondary side demands further considerations.

**Design with lumped output power**

One simple way of doing multiple output flyback design is described in detail in AN-22, "Designing Multiple Output Flyback Power Supplies with *TOPSwitch*". The design method starts with a single output equivalent by lumping output power of all outputs to one main output. Secondary peak current $I_{SP}$ and RMS current $I_{SRMS}$ are derived. Output average current $I_O$ corresponding to the lumped power is also calculated.

**Assumption for simplification**

The current waveforms in the individual output windings are determined by the impedance in each circuit, which is a function of leakage inductance, rectifier characteristics and capacitor value. Although this current waveform may not be exactly the same from output to output, it is reasonable to assume that, to the first order, all output currents have the same shape as for the single output equivalent of lumped power.

**Output RMS current vs. average current**

The output average current is always equal to the DC load current, while the RMS value is determined by current wave shape. Since the current wave shapes are assumed to be the same for all outputs, their ratio of RMS to average currents must also be identical. Therefore, with the output average current known, the RMS current for each output winding can be calculated as

$$I_{SRMS}(n) = I_O(n) \times \frac{I_{SRMS}}{I_O}$$

where $I_{SRMS}(n)$ and $I_O(n)$ are the secondary RMS current and output average current of the $n^{th}$ output and $I_{SRMS}$ and $I_O$ are the secondary RMS current and output average current for the lumped single output equivalent design.

**Customization of secondary designs for each output**

The turns for each secondary winding are calculated based on the respective output voltage $V_O(n)$:

$$N_S(n) = N_S \times \frac{V_O(n) + V_D(n)}{V_O + V_D}$$

Output rectifier maximum inverse voltage is

$$PIV_S(n) = V_{MAX} \times \frac{N_S(n)}{N_P} + V_O(n)$$

With output RMS current $I_{SRMS}(n)$, secondary number of turns $N_S(n)$ and output rectifier maximum inverse voltage $PIV_S(n)$ known, the secondary side design for each output can now be carried out exactly the same way as for the single output design.

**Secondary winding wire size**

*TOPSwitch-FX* design spreadsheet assumes a CMA of 200 when calculating secondary winding wire diameters. This gives the minimum wire sizes required for the RMS currents of each output using seperate windings. Designers may wish to use larger size wire for better thermal performance. Other considerations such as skin effect and bobbin coverage may suggest the use of a smaller wire by using multiple strands wound in parallel. In addition, practical considerations in transformer manufacturing may also dictate the wire size.

# Appendix B

## AN-25 and AN-16 Comparison Table

| Design Methodologies | AN-16 | AN-25 |
|---|---|---|
| Applicable products | *TOPSwitch*<br>*TOPSwitch-II* | *TOPSwitch-FX* |
| Product selection basis | $I_{LIMIT}(min) \geq I_P$ | AN-26 selection curves |
| Product selection validation | power dissipation | $I_{LIMIT}(min) \geq I_P$ |
| Mode of operation | continuous | continuous and discontinuous |
| Switching frequency $f_S$ | 100 kHz | 130 kHz or 65 kHz |
| Maximum duty cycle $D_{MAX}$ | 64% | 75% |
| $I_{LIMIT}$ reduction factor $K_I$ | N/A | $1.0 \geq K_I \geq 0.4$ |
| Core selection table | 100 kHz | 130 kHz & 65 kHz |
| Flux density limitation | design for $B_M \leq 3000$ & $B_P \leq 4200$ | design for $B_M \leq 3000$ & adjust $I_{LIMIT}$ to meet $B_P \leq 4200$ |
| Minimum gap size | $L_g \geq 0.05$ mm | $L_g \geq 0.1$ mm |
| Secondary winding wire size | calculated based on primary CMA | calculated based on CMA of 200 for minimum wire size |
| Secondary side design for multiple outputs | N/A | yes |

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