TOPSwitch® Tips, Techniques, and Troubleshooting Guide

Application Note AN-14

Answers to All Common *TOPSwitch* Technical Questions can be found in this application note, the *TOPSwitch* Data Sheets, the *TOPSwitch* Design Notes, and the *TOPSwitch* reference design/evaluation board documentation. The fastest path to *TOPSwitch* success is to **read the *TOPSwitch* data sheets, AN-16 and this document carefully and completely before beginning the design**. Detailed information on specific application circuits can be found in the Application Notes, Design Notes and Reference Design/Evaluation Board documentation listed below. **Purchasing a Reference Design/ Evaluation Board is strongly recommended and will dramatically reduce design, breadboarding, and debugging time**. For information on specific subjects including PC design, Drain Voltage Clamping, and Recommended Transformer Inductance, find the appropriate section in the table of contents on the next page. For problems encountered in working power supplies, refer directly to the Troubleshooting Guide. For technical questions not covered by any *TOPSwitch* literature, fill out a copy of the TOPFAX form given at the end of this application note and FAX to Power Integrations, Inc.

Other Design/Application Notes

AN-15: *TOPSwitch* Power Supply Design Techniques for EMI and Safety

AN-16: *TOPSwitch* Flyback Design Methodology

AN-17: Flyback Transformer Design for *TOPSwitch* Power Supplies

AN-18: *TOPSwitch* Flyback Transformer Construction Guide

AN-19: *TOPSwitch* Flyback Power Supply Efficiency

AN-20: Transient Suppression Techniques for *TOPSwitch* Power Supplies

DN-7: Power Factor Correction Using *TOPSwitch*

DN-8: Simple Bias Supplies Using the TOP200

DN-11: A Low-Cost, Low Part Count *TOPSwitch* Supply

DN-12: Non-isolated Flyback Supplies Using *TOPSwitch*

DN-14: Constant Current/Constant Power Regulation Circuits for *TOPSwitch*

DN-15: *TOPSwitch* Power Supply for Echelon PLT-21 Power Line Transceiver

DN-16: DC to DC Converters Using *TOPSwitch* for Telecom and Cablecom Applications

Reference Design/Evaluation Board Documentation

ST200: TOP200 Reference Design Board
95 to 370 Volt DC Input; 5V, 5W Output
(Replaced by RD1)

ST202A: TOP202 Reference Design Board
Universal AC Input; 7.5V, 15W Output

ST204A: TOP204 Reference Design Board
Universal AC Input; 15V, 30W Output

RD-1: TOP210 Reference Design Board
104 to 370 VDC Input, 4W Output

RD-2: TOP210 Reference Design Board
85 to 132 VAC or 170 to 265 VAC
input; 8W Output

Table of Contents

1. Troubleshooting Guide

GENERAL		
SYMPTOM	**CAUSE**	**WHAT TO DO**
Power supply does not start	Switching currents trigger shutdown latch	• Use Kelvin (single point ground) connection for all capacitors connected to Source pin (Section 4.1) • Minimize length of Source Pin • Improve PC layout (Section 4.2, 4.3) • Electrically isolate heat sink from circuit
	Transformer primary Zener clamp voltage too low	• Increase clamp Zener voltage rating to 1.5 times reflected output voltage V_{OR}
	Secondary winding connected backwards	• Reverse connection on winding to match schematic dot polarity
	Failed output rectifier or clamp circuit	• Replace output rectifier, clamp Zener, or clamp diode
	High optocoupler current during start up triggers shutdown latch	• Increase value of optical coupler LED series resistor • Use optical coupler with CTR between 50% and 200% • Add resistor (270 Ω to 620 Ω) in series with optocoupler emitter
	R3 exceeds 15 Ω (Figure 3)	• Add 0.1µF bypass capacitor across Control and Source pin (Section 12.1)
TOPSwitch blows up at turn on or overload	Insufficient clamping or high leakage inductance causes excessive Drain-Source voltage	• Use Zener diode/blocking diode clamp circuit across transformer primary (Section 3) • Make sure Zener voltage clamps Drain voltage below breakdown (Section 3) • Reduce transformer leakage inductance or V_{OR}
Low Efficiency	Transformer primary clamp Zener voltage too low causing high loss in clamp Zener	• Increase clamp Zener voltage rating to 1.5 times reflected output voltage V_{OR}
	Clamp circuit blocking diode is too slow or has low breakdown voltage rating	• Use ultra fast recovery rectifier with at least 400 Volt breakdown for TOP100 series and 600 Volt breakdown for TOP200 series (section 3)
	Output rectifier recovery too slow	• Use ultra fast recovery output rectifier
	Output rectifier breakdown voltage too low	• Increase breakdown voltage of output rectifier
	Transformer primary inductance too low causing high RMS currents	• Increase the transformer primary inductance • Increase the transformer turns ratio and primary inductance for higher duty cycle and lower peak current
	TOPSwitch current or power rating too low	• Use higher power *TOPSwitch* • Add or increase *TOPSwitch* heatsink

GENERAL		
SYMPTOM	**CAUSE**	**WHAT TO DO**
TOPSwitch appears to operate at 50 KHz (or lower subharmonic of 100 KHz switching frequency)	Turn-on Drain current spike duration exceeds leading edge blanking due to:	
	• Excessive clamp circuit capacitance	• Use Zener clamp circuit across transformer primary (Section 3)
	• Excessive RC damper capacitance	• Remove or reduce RC damping on primary or secondaries
	• Slow recovery rectifiers on output windings	• Use ultra fast recovery output rectifiers • Add heat sink to output rectifier
	• Excessive transformer primary capacitance	• Rewind transformer primary adding additional insulation between layers of primary winding to reduce capacitance (See AN-18) • Reduce number of turns on primary
Drain clamp Zener diode is too hot	Reflected output voltage exceeds Zener diode voltage rating	• Increase clamp Zener voltage rating to 1.5 times reflected output voltage V_{OR}
	Poor heat transfer	• Reduce Zener diode lead length • Increase PC trace width
	Slow recovery rectifiers on output windings	• Use ultra fast recovery output rectifiers
	Clamp dissipation exceeds Zener diode power rating	• Use higher power rating Zener • Place a 0.01 µF, 200V capacitor in parallel with Zener diode • Rewind transformer for lower leakage inductance
TOPSwitch too hot	High switching loss due to slow recovery clamp diode.	• Use ultra fast recovery rectifier with at least 400 Volt breakdown for TOP100 series and 600 Volt breakdown for TOP200 series (Section 3)
	High switching loss due to slow recovery output rectifier	• Use ultra fast recovery output rectifier
	Transformer primary inductance too low, causing high RMS currents	• Increase the transformer primary inductance • Increase the transformer turns ratio and primary inductance for higher duty cycle and lower peak current
	Poor heat transfer	• Add or increase size of heat sink
	Current or power rating too low	• Use *TOPSwitch* with higher current or output power rating
Power supply output voltage increases at high input voltage and light load	Minimum duty cycle delivers more energy than light load can consume	• Increase primary bias voltage (up to 30 Volts) • Add minimum load resistor (Section 11)

POWER SUPPLIES REGULATED WITH OPTICAL COUPLED FEEDBACK

SYMPTOM	CAUSE	WHAT TO DO
Power Supply Oscillates	Insufficient gain/phase margin due to:	
	• Output has (π-filter) filter adding additional phase shift to control loop.	• Connect optical coupler to the rectifier side of π section (Section 12.1)
	• Improper compensation	• Increase resistor in series with optocoupler LED (Section 12.1) • Increase size of auto-restart/compensation capacitor across Control and Source pins • Increase or add resistor in series with auto-restart/ compensation capacitor (Section 12.1)
	• Optocoupler current transfer ratio (CTR) too high	• Use optical coupler with CTR between 50% and 200% (Section 16)
Output voltage turns on too fast or overshoots	Control loop is too slow	• Increase control loop bandwidth • Add soft start capacitor (between 4.7 µF and 47 µF) across error amplifier output or Zener diode (Section 14)
Output voltage line frequency ripple too large	Control loop bandwidth too low	• Increase control loop bandwidth
	Input capacitor too small	• Increase input capacitor

POWER SUPPLIES REGULATED WITH BIAS WINDING FEEDBACK

SYMPTOM	CAUSE	WHAT TO DO
Power Supply Oscillates	Insufficient gain/phase margins	• Increase output capacitance • Increase size of auto-restart/compensation capacitor • Add or increase resistor R3 in series with auto-restart/ compensation capacitor (Section 12.1)
Output voltage turns on too fast or overshoots	Control loop is too slow	• Increase control loop bandwidth • Add RC soft start network (Section 14)
Poor load regulation	Leakage inductance spike on bias winding	• Add resistor in series with bias winding to filter leakage inductance spike (See DN-8) • Change transformer winding order so that primary is first and bias winding is last • On bias winding, use parallel, oversized diameter wire so bias winding completely covers width of bobbin
	Discontinuous mode operation	• Redesign transformer for continuous mode operation

POWER FACTOR CORRECTION CIRCUITS		
SYMPTOM	**CAUSE**	**WHAT TO DO**
PFC stage does not start	Drain voltage rings below Source potential	• Add fast recovery blocking diode in series with Drain (Section 19.1)
Total Harmonic Distortion (THD) is greater than 10%	Precompensation resistor value is not correct	• Adjust precompensation resistor until optimum THD has been obtained (See DN-7)
	Precompensation current waveform is being filtered	• Reduce bypass capacitance on Control pin to less than 4.7 µF • Add resistor (75 to 200 Ω) between Control pin bypass capacitor and auto-restart/compensation capacitor (R2 in Figure 19)
	Output voltage ripple modulates duty cycle	• Increase auto-restart/compensation capacitor to reject output voltage ripple
	Inductor value is too large and enters continuous mode at peak of rectified AC input voltage	• Decrease inductor value (See DN-7)
	Inductor value is too small and *TOPSwitch* current limit reduces duty cycle	• Increase inductor value (See DN-7) • Use *TOPSwitch* with higher current limit
PFC stage turns off with short interruption in AC power	Precompensation resistor current disables auto-restart	• Add 2.7 kΩ to 6.8 kΩ resistor across C3 (Figure 19) to shunt precompensation current from control pin (See DN-7)

2. Example Power Supply Circuits

The following three isolated power supplies will be used as examples in the text that follows. The ST200 (Figure 1) is a simple, absolute minimum part count 5V, 5W isolated bias supply using the TOP200 that operates from a high voltage DC bus. The ST202A (Figure 2) is a universal AC input, 7.5V, 15 Watt power supply using the TOP202 and demonstrates low cost, optically coupled feedback control. The ST204A (Figure 3) is a universal AC input, 15V, 30 Watt power supply using the TOP204 and features improved output voltage accuracy and regulation with optically coupled feedback control.

2.1 ST200 General Circuit Description

The ST200 is a low-cost, DC input, isolated Buck-Boost or flyback switching power supply using the TOP200 integrated circuit. The circuit shown in Figure 1 produces a 5 V, 5 W power supply that operates from 95 to 370 VDC input voltage. The 5 V output is indirectly sensed by the primary bias winding. The output voltage is determined by the *TOPSwitch* control pin voltage (typically 5.7V), the voltage drops of rectifiers D2 and D3, and the turns ratio between the bias winding and output winding of T1. Other output voltages are also possible by adjusting the transformer turns ratios.

The high voltage DC bus is applied to the primary winding of T1. The other side of the transformer primary is driven by the integrated high-voltage MOSFET within the TOP200. D1 and VR1 clamp the voltage spike caused by transformer leakage inductance to a safe value and reduce ringing at the Drain of U1. The power secondary winding is rectified and filtered by D2, C2, L1, and C3 to create the 5V output voltage. The bias winding is rectified and filtered by D3, R1 and C5 to create a bias voltage to the TOP200. C5 also filters internal MOSFET gate drive charge current spikes on the Control pin, determines the auto-restart frequency, and together with R1, compensates the control loop.

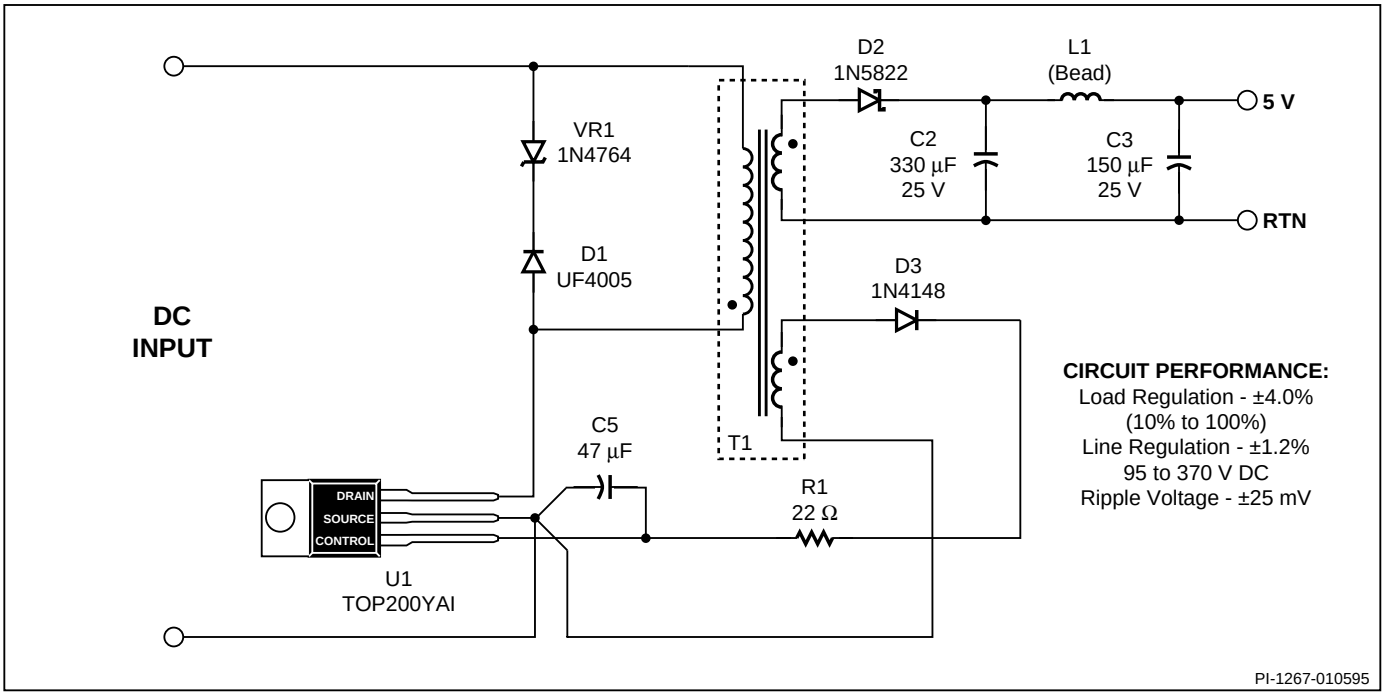

Figure 1. Schematic Diagram of the ST200 Minimum Parts Count 5V, 5W Bias Supply.

2.2 ST202A General Circuit Description

The ST202A is a low-cost, isolated Buck-Boost or flyback switching power supply using the TOP202 integrated circuit. The circuit shown in Figure 2 produces a 7.5 V, 15 W power supply that operates from 85 to 265 VAC input voltage. The 7.5 V output is directly sensed by optocoupler U2 and Zener diode VR2. The output voltage is determined by the Zener diode (VR2) voltage and the voltage drops across the optocoupler (U2) photodiode and resistor R1. Other output voltages are also possible by adjusting the transformer turns ratios and value of Zener diode VR2.

AC power is rectified and filtered by BR1 and C1 to create the high voltage DC bus applied to the primary winding of T1. The other side of the transformer primary is driven by the integrated high-voltage MOSFET within the TOP202. D1 and VR1 clamp the leading-edge voltage spike caused by transformer leakage inductance to a safe value and reduce ringing. The power secondary winding is rectified and filtered by D2, C2, L1, and C3 to create the 7.5 V output voltage. R2 and VR2 provide a slight pre-load on the 7.5 V output to improve load regulation at light loads. The bias winding is rectified and filtered by D3 and C4 to create a bias voltage to the TOP202. L2 and Y1-safety capacitor C7 attenuate common-mode emission currents caused by high-voltage switching waveforms on the Drain side of the primary winding and the primary to secondary capacitance. L2 and C6 attenuate differential-mode emission currents caused by the fundamental and harmonics of the trapezoidal or triangular primary current waveform. C5 filters internal MOSFET gate drive charge current spikes on the Control pin, determines the auto-restart frequency, and together with R1, compensates the control loop.

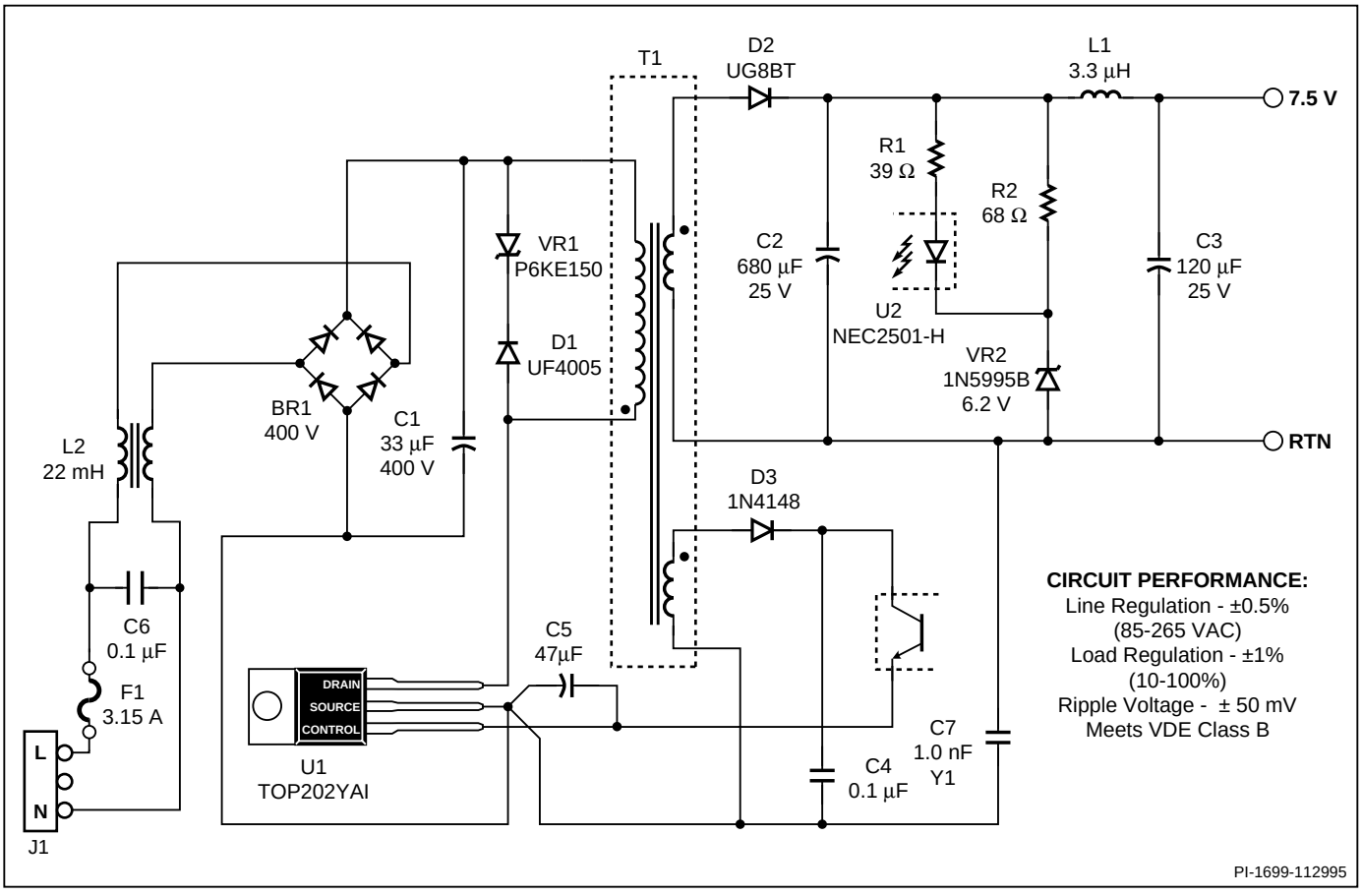

Figure 2. Schematic Diagram of the ST202A Power Supply.

2.3 ST204A General Circuit Description

The ST204A uses the TOP204YAI integrated circuit to implement an isolated Buck-Boost or flyback switching power supply. Figure 3 shows a power supply circuit delivering 30 W at 15 VDC from a universal AC input voltage of 85 to 265 VAC. Output voltage is directly sensed and accurately regulated by a secondary-referenced error amplifier. The error amplifier drives a current error signal through an optocoupler into the *TOPSwitch* Control pin to directly control *TOPSwitch* duty cycle. Output voltage can be fine-tuned by adjusting divider resistors R4 and R5.

AC input voltage is rectified by BR1 and filtered by C1 to create a high voltage DC bus ranging from 100 to 375 VDC. D1 and VR1 clamp leading edge voltage spikes and reduce ringing on the Drain voltage waveform caused by leakage inductance.

The T1 power secondary is rectified by D2 and filtered by C2 to generate DC output voltage. L1 and C3 provide additional filtering to reduce high frequency ripple voltage. R2 improves load regulation at light loads by pre-loading the output voltage.

The T1 bias winding is rectified by D3 and filtered by C4 to create the *TOPSwitch* bias voltage.

L2 and Y1-safety capacitor C7 attenuate common-mode emission currents caused by high-voltage switching waveforms on the Drain side of the primary winding and the primary to secondary capacitance. L2 and C6 attenuate differential-mode emission currents caused by the fundamental and harmonics of the trapezoidal primary current waveform.

C5 filters internal MOSFET gate drive charge current spikes on the Control pin, determines the auto-restart frequency, and together with R1, compensates the control loop.

The TL431 shunt regulator (U3) integrates an accurate 2.5 V bandgap reference, op amp, and driver into a single device used as a secondary-referenced error amplifier. Output voltage is sensed, divided by R4 and R5, and compared with the internal reference. C9 and R4 determine error amplifier frequency response. R1 limits LED current and sets overall control loop DC gain.

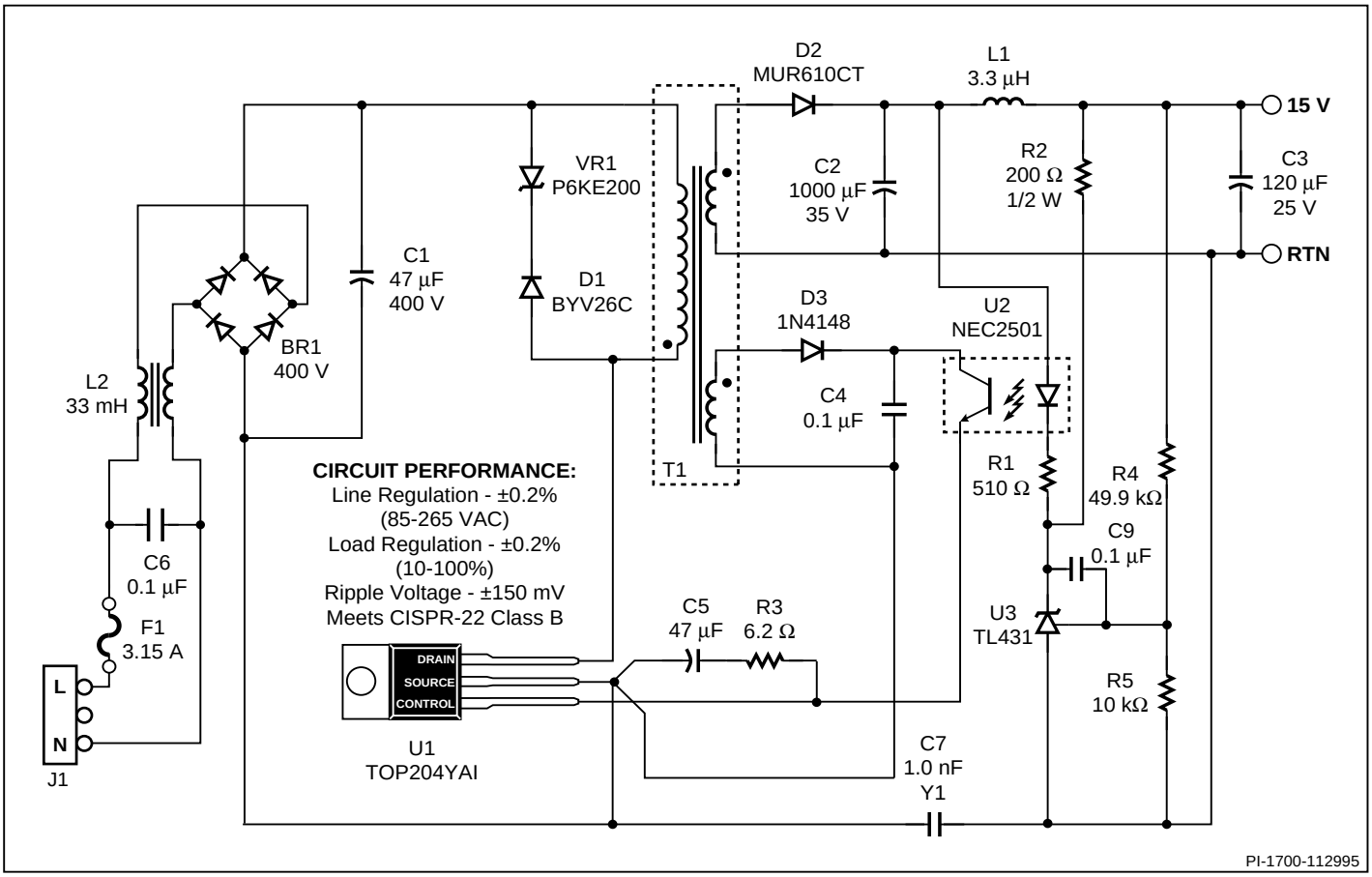

Figure 3. Schematic Diagram of the ST204A Power Supply

3. Drain Clamping

Transformer leakage inductance causes voltage spikes when the *TOPSwitch* output MOSFET turns off. These voltage spikes must be clamped to keep the *TOPSwitch* Drain voltage below the BV_{DSS} rating. The **recommended clamp circuits** shown in Figures 2 and 3 consist of blocking diode D1 and Zener diode VR1. Voltage spikes are effectively clamped below the *TOPSwitch* Drain voltage rating. **RCD clamp circuits are not recommended** because clamping voltage varies with load current. RCD clamp circuits may allow the drain voltage to exceed the data sheet breakdown rating of *TOPSwitch* during overload operation or during turn on with high line AC input voltage. D1 should be an ultra fast recovery, high voltage rectifier with a reverse recovery time t_{rr} of less than 75 nS and breakdown voltage rating of 400V for TOP1XX series and 600V for TOP2XX series. Zener diode VR1 must have sufficient power handling capability in both transient and steady state operation. VR1 should be selected such that clamp voltage is approximately 1.5 times higher than reflected output voltage V_{OR}. V_{OR} should be 60 V or less for TOP1XX devices and 135 V or less for TOP2XX devices. For all *TOPSwitch* power and peak current levels, the low cost, 5 Watt P6KE91-P6KE200 Zener diode transient voltage suppressor series can be used and is available from Motorola and SGS-Thomson. Transient voltage suppressor Zener diode thermal impedance and steady state power dissipation capability depend heavily on lead diameter which should be between 0.037 and 0.043 inch. Other manufacturers (including General Instrument and Fagor) make parts with identical part numbers but (due to smaller lead diameter) have lower effective thermal impedance and less steady state power dissipation capability. The 1.5 Watt 1N5956 (200 V) Zener diode is sufficient for lower power and lower peak drain current levels (below 600 mA) and are available from Motorola. Table 1 shows recommended blocking diodes (D1) and clamp Zener diodes (VR1) for each *TOPSwitch*. Also shown are other Zener diode families that can be used for clamp Zener diode VR1. Refer to AN-16 for more information on reflected output voltage and clamping.

	BLOCKING DIODES			CLAMP ZENER DIODES		
	Philips	**Motorola**	**General Instrument**	**115 VAC Input ($V_{OR} \leq 60V$)**	**Universal Input ($V_{OR} \leq 135V$)**	**Doubled 115 or 230 VAC Input ($V_{OR} \leq 135V$)**
TOP100	BYV26B	MUR140	UF4004	P6KE91		
TOP101	BYV26B	MUR140		P6KE91		
TOP102	BYV26B	MUR140		P6KE91		
TOP103	BYV26B			P6KE91		
TOP104	BYV26B			P6KE91		
TOP200	BYV26C	MUR160	UF4005		1N5956	1N59536
TOP201	BYV26C	MUR160	UF4005		P6KE200	P6KE200
TOP202	BYV26C	MUR160			P6KE200	P6KE200
TOP203	BYV26C	MUR160			P6KE200	P6KE200
TOP214	BYV26C				P6KE200	P6KE200
TOP204	BYV26C				P6KE200	P6KE200

Other clamp Zener diode series that can be used include:

1.0 Watt 1N476X (Motorola)
1.0 Watt VRD Z2XXU (Ishizuka)
1.3 Watt BZX85C (Thomson)
1.5 Watt BZY97 (Philips, Thomson, Fagor)
2 Watt BZ V47C (Thomson)
2.5 Watt BZD23 (Philips)
3.25 Watt BZT03 (Philips, Temic)
5 Watt 1N53XX (Motorola, Thomson)
6 Watt BZW03/D (Temic)

Table 1. Recommended Blocking Diodes (D1) and Recommended Clamp Zener Diodes (VR1).

4. PC Layout

4.1 Single Point Ground/Kelvin Source Pin Connections

Figure 4 shows how auto-restart/compensation capacitor C5 must be connected to the Source pin using a single point ground or Kelvin connection. Proper layout prevents shutdown at turn on or instability due to high Source pin switching currents. High voltage return to input capacitor C1 must be connected directly to the Source pad with a separate trace **and must not share the C5 trace**. Bias/feedback return should also be connected directly to the Source pad with a separate trace as shown.

The Source pin must be kept as short as possible. **Do not bend or extend the Source pin**. Insert *TOPSwitch* fully into the PC board as shown. Extend and bend the Drain pin if additional creepage distance on the PC board is necessary.

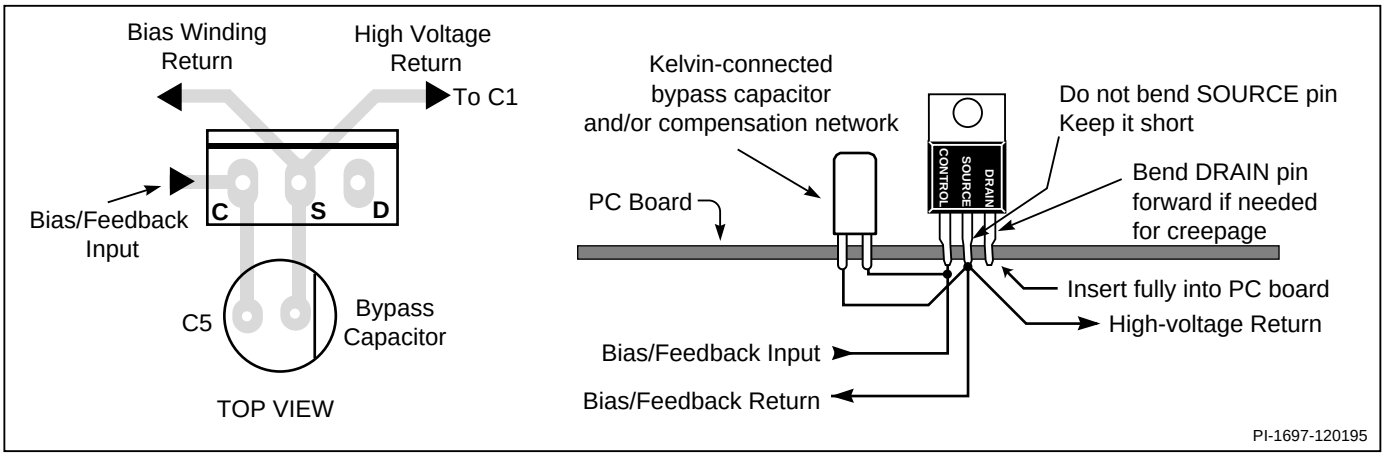

Figure 4. Recommended TOPSwitch Layout.

4.2 Ideal Component Placement

Figure 5 shows ideal component placement and single sided PC trace connections for all critical power and EMI components with the ST204A schematic (Figure 3) used for reference.

A checklist is provided on the next page which is useful for uncovering potential PC layout related problems in any *TOPSwitch* power supply.

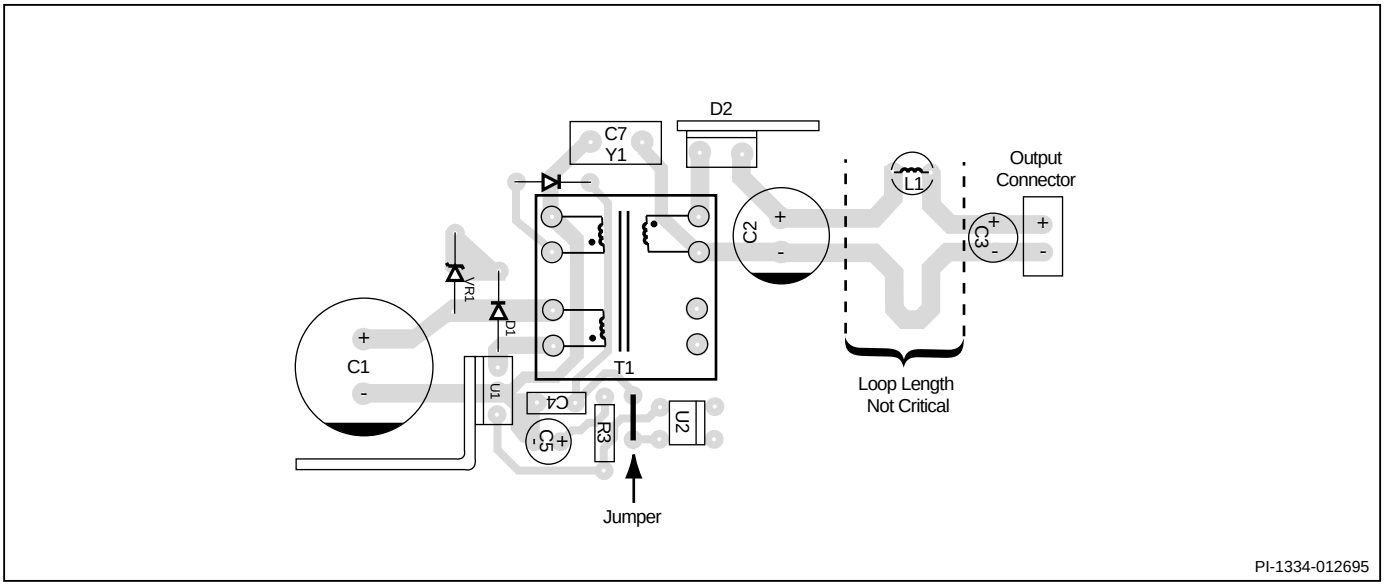

Figure 5. Ideal Placement for Critical Components.

4.3 PC Layout Checklist:

1) *TOPSwitch* (U1), C1, and Transformer T1 primary pins should be very close together to minimize PC trace length and loop area. The traces connecting these components have fast switching currents which cause common mode EMI emissions. Note *TOPSwitch* alignment and right angle heat sink.

2) D1, VR1, and Transformer T1 primary pins should be very close together to minimize PC trace length and loop area. Traces connecting these components have fast switching currents which cause common mode EMI emissions.

3) *TOPSwitch* Drain connection to T1 primary pins and clamp diode D1 must be very short because, in addition to fast switching currents, this trace also has high switching voltage which causes additional common mode EMI emissions.

4) *TOPSwitch* Source pin should connect directly to C1 with no other traces connected to this trace segment.

5) Y1-capacitor C7 should connect directly to the transformer T1 primary bias winding return and secondary output winding return pins with short, wide traces.

6) Transformer T1 primary bias winding return should be connected directly to *TOPSwitch* Source pin. No other components should be connected to this trace segment because lightning surge test voltages induce noise voltage drops.

7) Bias diode D3 should be as close as possible to transformer T1 bias winding pins. This placement minimizes anode trace length (which has high switching voltages) and maximizes length of the relatively quiet cathode trace.

8) Cathode of D3 should connect directly to C4. No other components should be connected to this trace segment because lightning surge voltages and rectification current will induce noise voltage drops. C4 should then be connected through a PC trace and top side wire jumper to optocoupler U2.

9) Capacitor C4 should be connected directly to *TOPSwitch* Source pin with no other traces connected to this trace segment. No other components should be connected to this trace segment because lightning surge test voltages will induce noise voltage drops.

10) Capacitor C5 should be connected directly to *TOPSwitch* Source pin with no other traces connected to this trace segment. No other components should be connected to this trace segment because lightning surge test voltages will induce noise voltage drops.

11) Output rectifier D2, C2, and Transformer secondary pins should be very close together to minimize PC trace length and loop area. Traces connecting these components have fast switching currents which cause common mode EMI emissions. PC traces should be wide because peak currents are much higher than DC load current.

12) C3 should be close to the output connector and directly across the traces connecting to the output connector to minimize output switching noise. Note that the PC traces run right through the capacitor lead pads and that no additional PC traces have been placed in series with C3. Note also that PC traces in series with L1 and the PC trace connecting C2 and C3 can be narrower and longer because current flow is essentially DC.

13) Heat sinks should be either connected only to *TOPSwitch* tab or completely isolated from both *TOPSwitch* tab and circuit. If the heat sink is connected elsewhere in circuit but isolated from *TOPSwitch* tab, capacitance between *TOPSwitch* tab and heat sink can resonate with circuit inductance causing high frequency ringing currents which may trigger *TOPSwitch* shutdown latch.

5. Flyback Power Supply Transformer

5.1 Power and Inductance Ranges

Nominal output power and primary inductance ranges are given in Table 2 for each *TOPSwitch* under the following AC input voltage conditions and transformer reflected output voltage V_{OR}.

- North America, Japan, and Taiwan (85 - 132 VAC, 50/60 Hz), V_{OR} = 60 V.
- Universal Input (85 - 265 VAC, 50/60 Hz), V_{OR} =135 V.
- Europe and Asia (195 - 265 VAC, 50/60 Hz), V_{OR} = 135 V.

These output power ranges are rough guidelines intended only for initial *TOPSwitch* selection and as a starting point for design. Output power levels outside the given ranges can be used with proper attention to transformer design, heat sinking, and mechanical packaging. For more information, refer to AN-16 for flyback power supply design guidelines. Refer to AN-17 for transformer design and AN-18 for transformer construction guidelines.

Values in the table are based on the following assumptions:

Minimum Available Peak Power (P_{PEAK}) is based on the trapezoidal, continuous mode Drain current waveform shown in Figure 6a and maximum primary inductance L_{MAX} for each *TOPSwitch* shown in Table 2. Ripple current to peak current ratio K_{RP} is typically 0.4 for 100/115 VAC or universal input and K_{RP} is 0.6 for 230 VAC input. P_{PEAK} is the minimum peak power available at 90% of the minimum specified *TOPSwitch* Current Limit (I_{LIMIT}) and low line AC input voltage. Continuous output power will approach P_{PEAK} with infinite heat sinking. **P_{MAX}** is based on empirical data with moderate heat sinking in continuous mode operation with L_{MAX} for each *TOPSwitch* shown in Table 2.

P_{MIN} is based on empirical data with moderate heat sinking in discontinuous mode operation with the triangular Drain current waveform shown in Figure 6b and L_{MIN} for each *TOPSwitch* shown in Table 2.

Input storage capacitor values:

3 µF per Watt of output power for 100/115 or universal mains voltage (85 VAC minimum)

1 µF per Watt of output power for 230 VAC mains voltage (195 VAC minimum)

100/115 VAC INPUT, V_{OR} = 60 V, K_{RP} = 0.4						
Part #	Suggested Primary Inductance (µH)		Suggested Output Power (W)			
	L_{MIN}	L_{MAX}	P_{MIN}	P_{NOM}	P_{MAX}	$*P_{PEAK}$
TOP100	504	1128	0	10	19	19
TOP101	357	649	15	24	33	33
TOP102	268	446	20	33	45	48
TOP103	214	340	25	40	55	63
TOP104	179	293	30	45	60	73
UNIVERSAL INPUT, V_{OR} = 135 V, K_{RP} = 0.4						
	L_{MIN}	L_{MAX}	P_{MIN}	P_{NOM}	P_{MAX}	$*P_{PEAK}$
TOP200	1963	3537	0	6	12	13
TOP201	1150	1703	10	16	22	27
TOP202	766	1150	15	23	30	40
TOP203	575	958	20	28	35	48
TOP214	460	754	25	34	42	61
TOP204	383	630	30	40	50	73
230 VAC INPUT, V_{OR} =135 V, K_{RP} = 0.6						
	L_{MIN}	L_{MAX}	P_{MIN}	P_{NOM}	P_{MAX}	$*P_{PEAK}$
TOP200	2594	3677	0	9	18	18
TOP201	1418	1789	20	29	37	37
TOP202	946	1203	30	43	55	55
TOP203	709	988	40	54	67	67
TOP214	567	788	50	68	84	84
TOP204	473	662	60	80	100	100

$*P_{PEAK}$ is the minimum available peak power at 90% of the minimum specified *TOPSwitch* current limit (I_{LIMIT}) and low line AC input voltage.

Table 2. Recommended Flyback Power Supply Primary Inductance and Output Power Ranges.

For applications requiring high efficiency and low power loss, start with appropriate P_{MAX} column to select the proper *TOPSwitch*. Then pick the transformer primary inductance from the L_{MAX} column. For example, for a universal input and 22 Watt output, start with the Universal Input table and P_{MAX} column. The TOP201 will be the first choice. Primary inductance is read from the L_{MAX} column and found to be 1703 µH.

Applications requiring a small size transformer should start with the appropriate P_{MIN} column to select the proper *TOPSwitch*. Then pick the transformer primary inductance from the L_{MIN} column. For example: for a 115 VAC input and 20 Watt output, start with the 100/115 VAC Input table and P_{MIN} column. The TOP102 is the first choice. Primary inductance is read from the L_{MIN} column and found to be 268 µH.

P_{PEAK} is critical for power supply applications with large peak loads such as disk drives, printers, and audio amplifiers. Heat sinking and component temperature rise determines the length of time that *TOPSwitch* can deliver peak power P_{PEAK}.

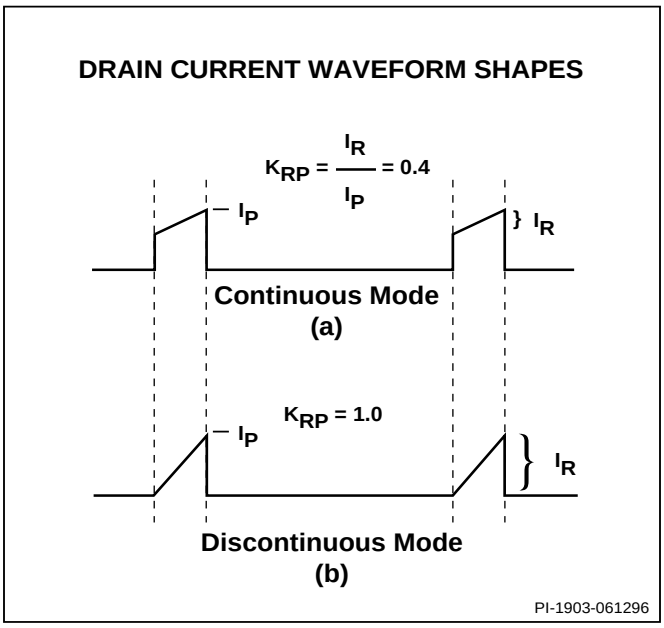

Figure 6. Current Waveform Shapes.

5.2 Transformer Turns Ratio Curves

The transformer turns ratio is determined from the low line minimum DC input voltage V_{MIN}, output voltage V_O, and reflected output voltage V_{OR}. V_{MIN} depends on the energy storage input capacitance. A general rule is to use 3 µF/watt of output power for universal input or 100/115 VAC applications and 1 µF/watt of output power for 230 VAC input applications. Applications using doublers to get the higher effective DC voltage from a 100/115 VAC input should use two series capacitors, each with a value of 2 µF/watt of output power. These capacitor guidelines result in a minimum V_{MIN} of approximately 90 VDC for universal input or 100/115 VAC applications and 240 VDC for 230 VAC or doubler applications.

Applications using the TOP2XX series devices and operating from universal input voltage, 230 VAC, or using a doubler from 100/115 VAC should have a transformer designed for a reflected voltage V_{OR} of 135 V or less to limit peak Drain voltage stress. Applications using the TOP1XX series devices operating from 100/115 VAC should design for a reflected output voltage V_{OR} of 60 V or less. Some applications can benefit by designing for slightly lower reflected output voltage V_{OR} to reduce voltage stress when operating at high line.

The transformer turns ratio is given below where N_p is the primary number of turns, N_S is the secondary number of turns, V_{OR} is the reflected output voltage, V_O is the output voltage, and V_D is the diode forward voltage.

$$\frac{N_P}{N_S} = \frac{V_{OR}}{V_O + V_D}$$

Turns ratio curves derived from the above equation are shown in Figure 7 for reflected output voltages of 60 V and 135 V. V_{DIODE} is assumed to be 0.7 V.

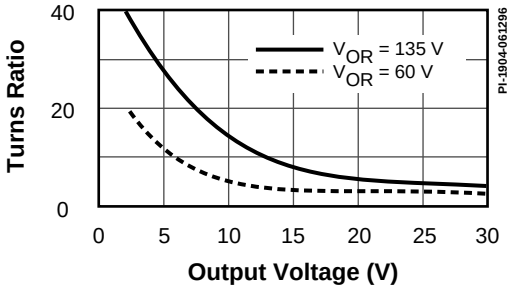

Figure 7. Transformer Turns Ratio for Various Minimum DC Input Voltages and Duty Cycles.

6. Optimizing Power Supply Efficiency

Efficiency is typically greater than 80% for most *TOPSwitch* power supplies above 10 Watts. Efficiency can be enhanced to as high as 90% with the following changes:

Design for higher output voltage (up to 30 Volts). For example, if a choice is available between output voltages of 12 and 15 Volts, the 15 Volt design will have better efficiency.

Use Schottky output rectifiers. Universal input voltage operation will require a transformer designed for 135 V reflected output voltage V_{OR} to keep secondary voltage stress below Schottky rectifier breakdown rating.

Increase transformer primary inductance for continuous mode operation to reduce *TOPSwitch* RMS current and conduction power loss. Figure 6a shows the trapezoidal, continuous mode Drain current waveform. The ripple current to peak current ratio (K_{RP}) has a practical lower limit of 0.4 (0.6 for 230 VAC input). To maintain control loop stability when operating in the continuous mode, output capacitor size or compensation circuitry may need to change.

Reduce transformer leakage inductance with split primary winding.

Remove primary RC damping networks. A properly designed primary clamp circuit will reduce primary ringing so that a damping circuit is not necessary.

Remove secondary RC damping network. Proper attention to PC board layout and selection of EMI filter components may eliminate the need for the secondary RC damping network.

Choose higher current bridge rectifier diodes and common mode choke to reduce power losses due to input current.

Remove minimum load circuit if application allows.

Use higher power *TOPSwitch* with lower $R_{DS(ON)}$.

Add heat sinks to *TOPSwitch* and output rectifier D2.

Refer to AN-19 for more information.

7. Thermal Design

7.1 Heat Sinking

TOPSwitch, clamp Zener diode VR1, and output rectifier D2 are the critical power bearing components. Temperature data should be taken on each of these three components at rated load current and input voltage in the mechanical package used for the actual application. Excessive component temperature can be reduced by selecting components with higher rating, using mounting techniques with better heat transfer, or adding heat sinks.

Heat sinking *TOPSwitch* is very simple. The TO220 tab is simply attached directly to the heat sink using a screw, bolt, or clip. Power supplies in plastic enclosures usually require a simple, non-safety-isolated, sheet metal stamped heat sink mounted along the edge of the PC board to transfer heat to the inside wall of the enclosure. In forced air applications, *TOPSwitch* is also directly attached to a non-safety-isolated, free standing heat sink located in the moving air path. Applications with metal chassis or cold plates require safety insulation beneath the *TOPSwitch* tab.

Axial output rectifiers and Zener diodes conduct heat through the mounting leads. Thermal impedance can be reduced and power handling improved by mounting axial rectifiers with short leads to wide copper traces on the PC board. Thermal impedance through each lead can be different if the die is bonded directly to one lead and connected to the other lead through a bonding wire. With vertical mounting, the lead with the lowest thermal impedance should be kept very short to minimize device junction temperature. A larger T0-220 style diode can also be used with the various heat sinks described above.

7.1 Heat Sinking (continued)

The clamp Zener diode must also be mounted with very short leads and wide copper traces for lowest thermal impedance. For example: the Motorola 5 Watt 1N5333B-1N5388B Zener diode series has a primary thermal conduction path through the cathode lead which should be the shorter lead when vertically mounted. Dissipation in clamp Zener diode VR1 can also be minimized by reducing transformer leakage inductance.

7.2 Thermally Protecting Entire Power Supply

TOPSwitch on-chip overtemperature protection will protect the entire power supply during overload conditions that are not severe enough to trigger auto-restart. Clamp Zener diode VR1 and output rectifier D2 must be selected and mounted to withstand overload conditions at high line input long enough for the *TOPSwitch* junction temperature to reach the Thermal Shutdown Temperature threshold. The output rectifier should have slightly better heat sinking compared with *TOPSwitch* (U1) in most applications. For example, the 15 Watt ST202A power supply using the TOP202YAI (Figure 2) has no *TOPSwitch* heat sink but has a small (0.8 inch x 0.8 inch, 40 mil thick), stamped copper plate style heat sink attached to the output rectifier. The 30 Watt ST204A power supply using the TOP204 (Figure 3) has a *TOPSwitch* heat sink (1.0 inch x 1.0 inch, 40 mils thick) and a larger heat sink (1.4 inch x 1.0 inch, 40 mils thick) on output rectifier D2.

8. Auto-Restart

Aluminum electrolytic auto-restart capacitor C5 determines the amount of time allowed for power supply start-up. When power is first applied, C5 charges to 5.7 Volts before the *TOPSwitch* MOSFET is enabled and the power supply starts. The output voltage must become regulated before C5 discharges from 5.7 V to approximately 4.7 V or *TOPSwitch* will disable the MOSFET and enter the auto-restart mode. During auto-restart, C5 goes through 8 charge/discharge cycles before the *TOPSwitch* MOSFET is enabled again for another try. C5 may have a series resistor up to 100 Ω which has little effect on auto-restart.

Low DC input voltage (below 40 V) will cause the auto-restart time intervals to increase and auto-restart frequency to decrease. AC mains voltage is rectified and filtered resulting in a minimum high voltage DC bus of at least 85 VDC. During AC input voltage transients or dropout conditions, input storage capacitor C1 can discharge below 40 V which reduces *TOPSwitch* Control Pin Charging Current I_C, increases charging time for auto-restart capacitor C5, and decreases the auto-restart frequency. Short interruptions of AC power will cause *TOPSwitch* to enter the 8-count auto-restart cycle before starting again if input energy storage capacitor C1 is not completely discharged and auto-restart capacitor C5 is not discharged below the Control pin internal Power Up Reset Voltage Threshold. A short delay due to auto-restart will be observed when starting after a short interruption in input power.

The Control pin voltage also has the 8 count, hysteretic auto-restart waveform whenever the output MOSFET is disabled. This includes latching shutdown where the output MOSFET has been latched off. When the internal shutdown latch is set, the hysteretic waveform on the Control pin will continue until *TOPSwitch* is reset by removing input power or shorting the Control pin to the Source pin.

9. Output Overvoltage Protection

Figure 8 shows a discrete SCR circuit which turns *TOPSwitch* off when an overvoltage condition is sensed on the primary bias winding. This circuit latches externally and holds the Control pin low. Overvoltage latching occurs when the bias voltage exceeds the sum of the Zener diode voltage and the NPN transistor base-emitter voltage drop (0.7 V).

Figure 9 shows a DIAC (or silicon bi-directional switch) circuit which triggers the internal shutdown latch and turns *TOPSwitch* off when an overvoltage condition causes the primary bias winding to exceed the DIAC trigger voltage.

A Zener diode can be used to limit the output voltage as shown in Figure 10. If the optocoupler or secondary reference fails, regulation will default to the primary connected Zener for output voltage control.

10. Current to Duty Cycle Conversion

TOPSwitch is a voltage-mode device that produces a duty cycle inversely proportional to Control pin current. *TOPSwitch* is not a current-mode device. Increasing Control pin current will linearly decrease the duty cycle down to the minimum duty cycle value. Further increases in Control pin current will have no effect on the duty cycle until reaching the Latched Shutdown Trigger Current (I_{SD}) threshold at which point *TOPSwitch* shuts down.

11. Minimum Duty Cycle Operation

TOPSwitch internal supply current remains constant and does not vary with duty cycle because of the minimum Duty Cycle DC_{MIN}. In some cases, a small pre-load may be necessary to keep a lightly loaded or unloaded output voltage within the desired range due to DC_{MIN}. Shunt resistance or a Zener diode with the proper power rating can simply be added across the output voltage to provide preload current. Figure 2 shows how R2 and VR2 provide minimum loading for the ST202A without adding a large power component. R2 is a small, 1/8 Watt resistor which passes minimum load current through the existing 500 mW Zener diode (VR2). Figure 3 shows a variable minimum loading approach used on the ST204A. R2 dissipates the most power when the power supply output is lightly loaded and the TL431 (U3) output is saturated low to decrease *TOPSwitch* duty cycle. During normal operation, when wider duty cycles are necessary, *TOPSwitch* Control pin current is lower, TL431 output voltage is higher, R2 power dissipation is lower, and overall efficiency is improved.

12. Control Loop

12.1 Basic Techniques

The *TOPSwitch* control function has two poles and a zero. One pole is due to an internal RC filter with a typical corner frequency of 7 kHz. This RC network filters switching noise but contributes little phase shift at normal crossover frequencies of 1 to 2 kHz. Auto-restart capacitor C5 (typically 47 µF) together with the Control pin dynamic impedance (typically 15Ω) contributes the second pole of approximately 226 Hz. C5 as shown in Figure 11a has equivalent series resistance (typically 2Ω) which creates a zero at approximately 1.7 kHz. This compensation method is used for power supplies operating in discontinuous mode or lightly continuous mode at duty cycles of 50% or less (such as the ST202A in Figure 2).

Additional series resistance R3 (between 2 Ω and 15 Ω) can be added as shown in Figure 11b to move the zero lower in frequency. This compensation method is used for power supplies operating in continuous mode (such as the ST204A in Figure 3).

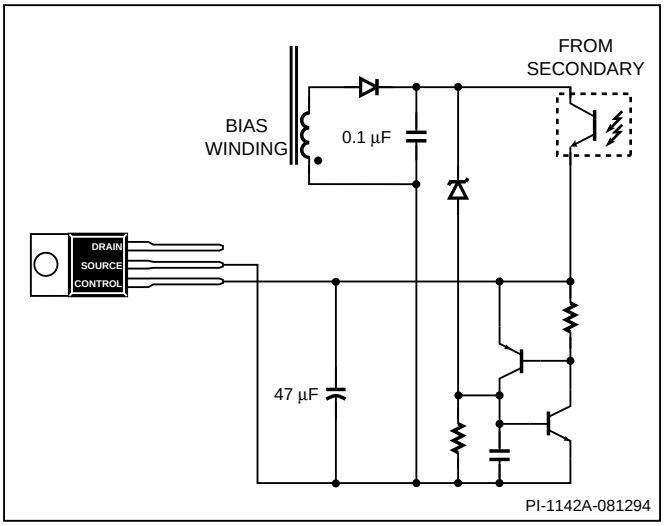

Figure 8. Latching Overvoltage Protection Using an SCR.

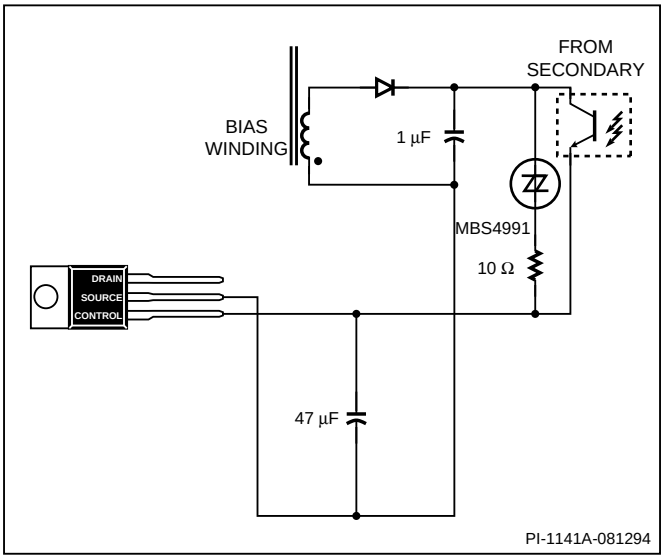

Figure 9. Latching Overvoltage Using a Diac.

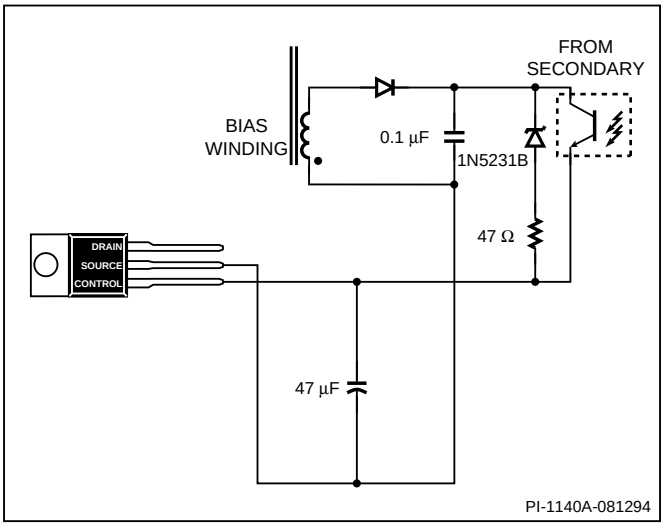

Figure 10. Bias Winding Regulator to Limit Output Voltage.

12 Control Loop (continued)

R3 can be increased beyond 15Ω up to a maximum value of 100Ω to eliminate the effect of auto-restart capacitor C5 from the control loop but bypass capacitor C10 must then be added as shown in Figure 11c. This compensation method is good for power supplies with sophisticated, secondary side compensation schemes that do not require the dominant pole caused by auto-restart capacitor C5. **R3 values beyond 100Ω are not recommended** because auto-restart timing intervals will decrease and auto-restart frequency will increase significantly.

In optocoupler feedback (such as the ST204A in Figure 3 and the ST202A in Figure 2), series resistor R1 determines loop gain. The initial value of R1 is selected using the following "5% Rule": with the power supply operating at nominal line and full load conditions, the average voltage across R1 should be approximately 5% of the output voltage. To help compensate the control loop, R1 can be increased above the 5% value to reduce loop gain. In optocoupler circuits which use a Zener diode (such as the ST202A circuit in Figure 2), reducing R1 below the 5% value will improve load regulation but will also increase loop gain.

Stability can be examined with a step load change applied to the power supply output. A current step from 75% to 100% of rated output current is normally used. The voltage response is observed for settling time and damping. In primary bias power supplies, the bias voltage should be tested separately with a step load change of 25% (typically 1 mA).

An LC postfilter effectively reduces output switching frequency ripple voltage and high frequency noise but can cause circuit instability due to additional phase shift. The ST202A power supply (Figure 2) shows the proper connection for simple optocoupler circuits (to the rectifier side of L1). The ST204A power supply (Figure 3) shows the proper connection for accurate optocoupler circuits. The optocoupler is connected to the rectifier side of L1 but the resistor divider senses the voltage directly at the power supply output which makes load regulation independent of the DC resistance of L1. In this method, DC feedback comes directly from the output while AC feedback comes from before the postfilter to avoid additional phase shift.

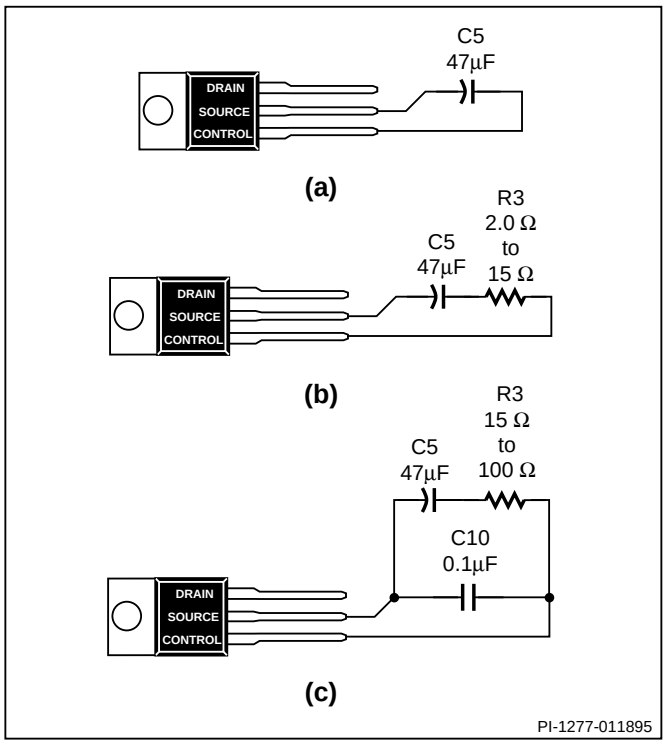

Figure 11. Control Pin Compensation.

12.2 TOPSwitch Circuit with Enhanced Bandwidth

Simple circuit improvements reduce output voltage line frequency ripple and improve transient response in *TOPSwitch* power supplies using a TL431 shunt regulator and optocoupler for control loop feedback. Figure 12 shows how the control circuitry of a typical *TOPSwitch* power supply (such as the ST204A Reference Design using the TOP204YAI) can be easily modified to increase control loop gain and bandwidth which reduces output voltage line frequency ripple while also improving transient response. Reducing capacitance C9 down to 0.01 µF improves TL431 frequency response. Increasing R3 to 13 Ω improves loop phase margin. Adding 100 kΩ resistor R6 as shown increases overall gain and also increases phase margin.

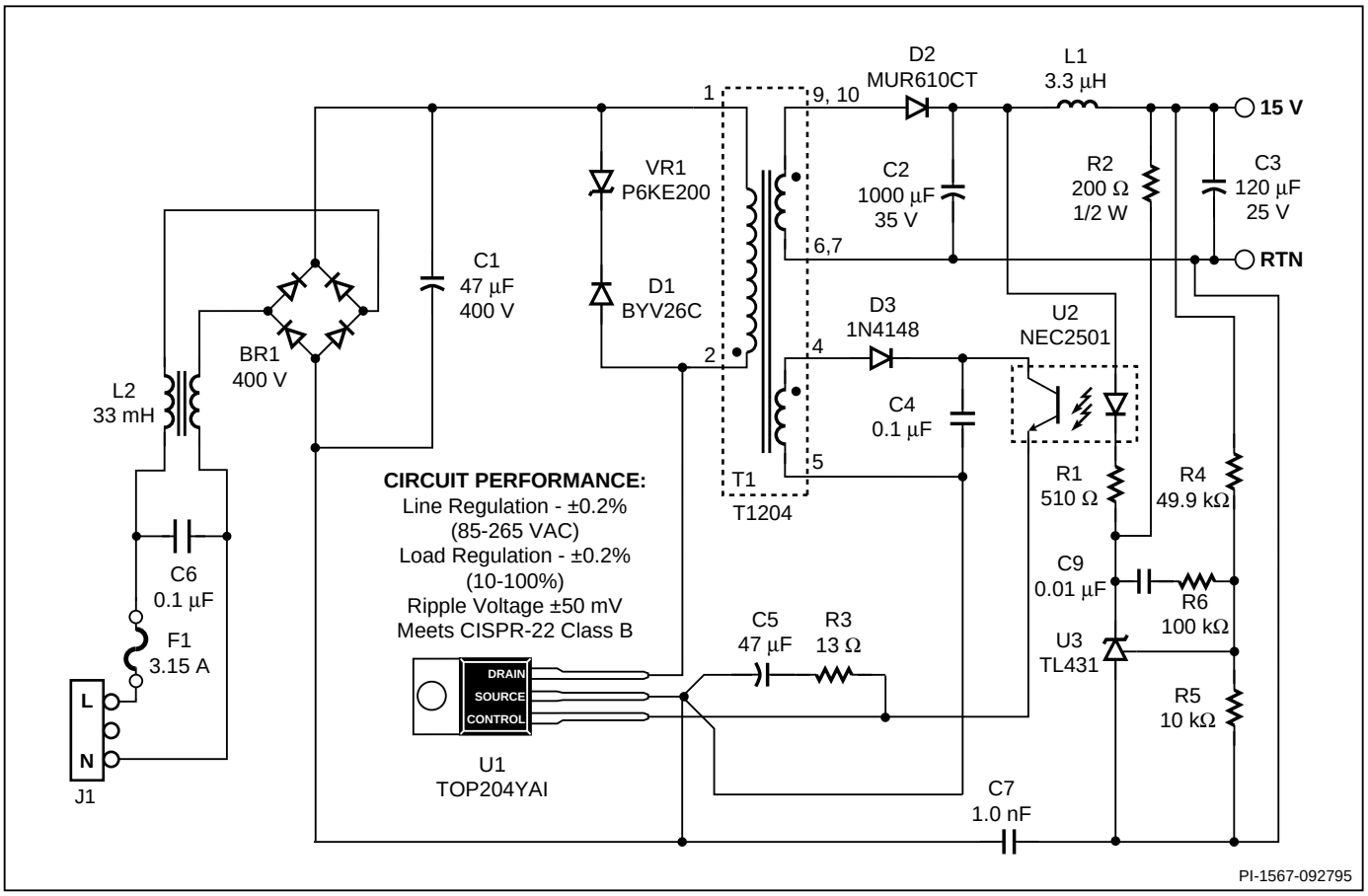

Figure 12. Schematic Diagram of the ST204A Power Supply with Enhanced Bandwidth and Lower Line Frequency Ripple Voltage.

13. EMI

13.1 *TOPSwitch* Advantages

Common mode EMI is lower with *TOPSwitch* because of the Source connected TAB and controlled turn-on.

The *TOPSwitch* thermal tab is connected to the quiet Source of the output MOSFET. The tab of discrete power MOSFET transistors act as antennae, broadcasting common-mode emissions because the tab is connected to the Drain which is switching at high frequency. The discrete MOSFET common-mode emissions are even higher when a heat sink is added.

The *TOPSwitch* internal MOSFET has a controlled turn-on characteristic which determines falling edge dv/dt (typically 50 ns) and further decreases common-mode emissions. Discrete controller/MOSFET solutions require extra components to properly tailor the turn-on fall time. Drain trace length should be kept as short as possible to minimize radiated EMI.

13.2 EMI Filter Topology

General EMI filter topology is shown in both the ST202A (Figure 2) and ST204A (Figure 3) schematics. Common mode emission currents are attenuated by common mode choke L2 and Y1-capacitor C7. L2 and C6 attenuate difference mode emission currents due to the fundamental and harmonics of the trapezoidal or triangular current waveform flowing in the transformer primary, *TOPSwitch* MOSFET, and C1. Figures 2 and 3 show a single reinforced insulation Y1 safety capacitor C7 (Murata DE1110E102M ACT4K-KD, Roederstein WKP102MCPE.OK or Rifa part number PME294RB4100M), rated for direct connection between primary and secondary. When using standard Y2-capacitors, two larger capacitors (typically 2200 pF) must be used in series to meet safety requirements. Refer to AN-15 for more information.

14. Soft Start

14.1 Optocoupler Feedback

Soft Start can be added to eliminate turn-on overshoot in optocoupler feedback applications with a 4.7 µF to 47 µF aluminum electrolytic capacitor (C_{SS}) placed across the shunt element as shown in Figure 13. Soft start capacitor C_{SS} increases optocoupler current during turn-on to limit the duty cycle and slow down the rising output voltage. C_{SS} has minimal effect on the control loop during normal operation. R2 discharges soft start capacitor C_{SS} when input power is removed.

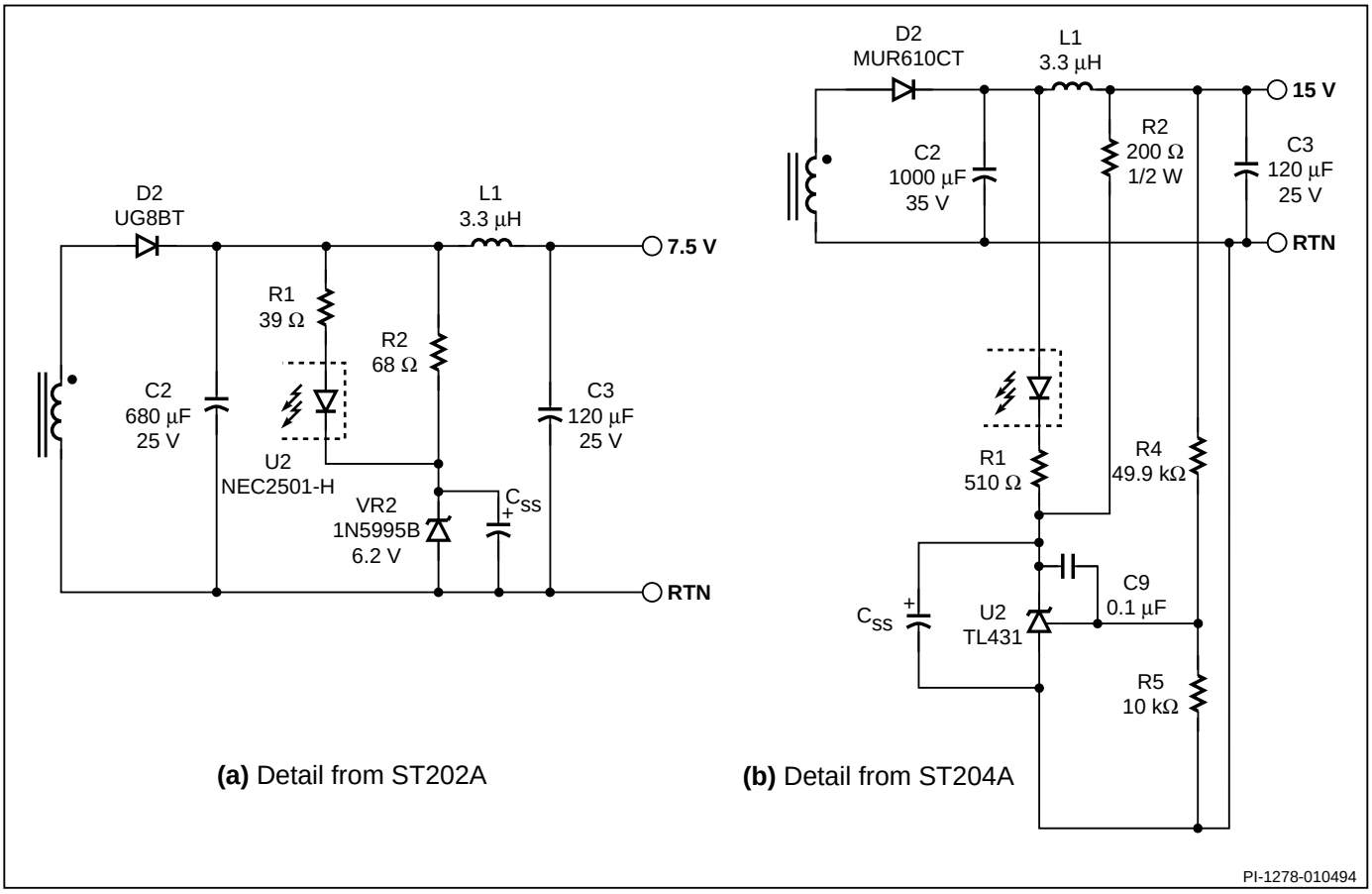

Figure 13. Implementing Soft Start with Optocoupler Feedback.

14.2 Bias Winding Feedback

Soft Start can be implemented to eliminate turn-on overshoot in primary regulated feedback applications with the circuit shown in Figure 14. Soft start capacitor C_{SS} increases *TOPSwitch* control pin current during turn-on to limit the duty cycle and slow down the rising output voltage. Resistor R_D discharges C_{SS} when the power supply is turned off.

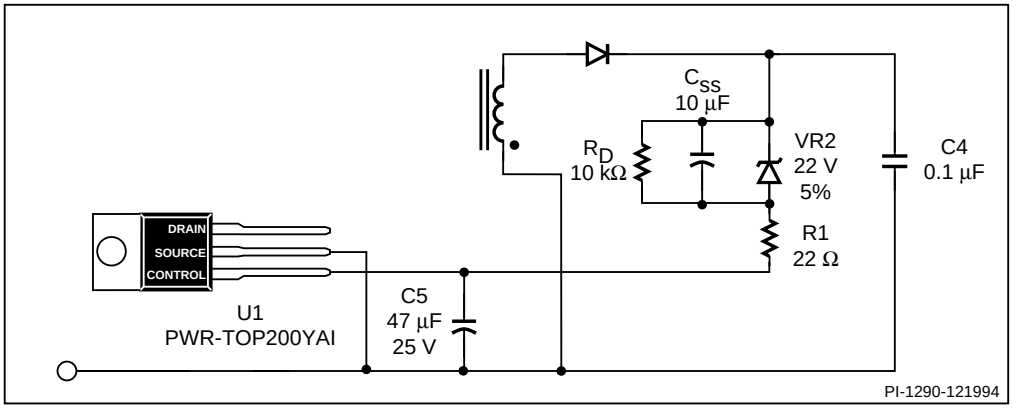

Figure 14. Implementing Soft Start with Bias Winding Feedback

15. Bench Testing

Figure 15 shows a *TOPSwitch* general test circuit for measuring most data sheet parameters. This test circuit is not applicable for current limit or output characteristic measurements. Under some conditions, externally provided bias or supply current driven into the Control pin from a low impedance source (<1 kΩ) can stall *TOPSwitch* in an auto-restart cycle indefinitely and prevent starting. Shorting the Control pin to the Source pin will reset the shutdown latch within *TOPSwitch*, which will then begin a normal start-up cycle. To avoid this problem when doing bench evaluation, it is recommended that power should be applied to the Control pin before the Drain voltage is applied.

Do not plug the *TOPSwitch* device into a "hot" IC socket during test. Capacitors mounted on the PC board may be charged and deliver a surge current into the low impedance Control pin. This surge current may be sufficient to trigger the *TOPSwitch* shutdown latch.

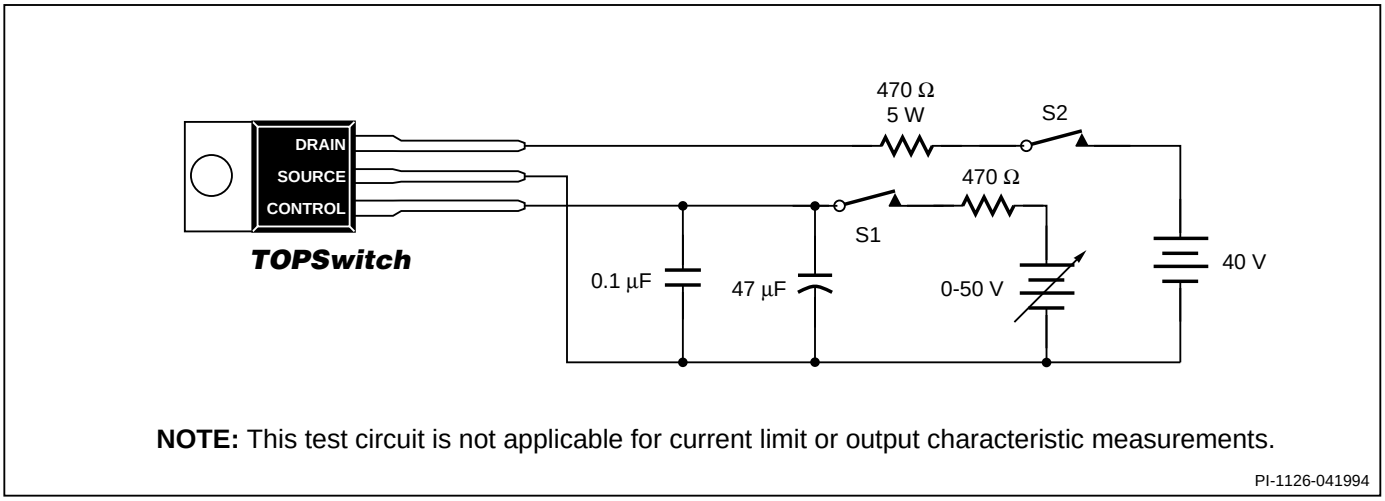

Figure 15. TOPSwitch General Test Circuit.

16. Optocoupler Recommendations

Optocouplers graded for minimum current transfer ratio (CTR) variation with minimum CTR above 50% and maximum CTR below 200% are recommended. CTR below 50% will require excessive photodiode currents to properly control *TOPSwitch* duty cycle. CTR above 200% could trigger the *TOPSwitch* shutdown latch during start up or load transients. The 5% rule for R1 selection (Section 12.1) will compensate for nominal CTR value. Table 3 lists many suitable optocouplers from various manufacturers. (Isocom requires an "X" suffix for safety agency approved versions.) *Generic 4NXX series optocouplers (including 4N25, 4N26, etc.) are not recommended because CTR is uncontrolled.*

	CTR(%)	BVCEO	MFG
6 Pin Dip			
CNY17-2	63-125	70 V	Motorola, Siemens, Toshiba Quality Technologies, Isocom
CNY17-3	100-200	70 V	Motorola, Siemens, Toshiba Quality Technologies, Isocom
SFH600-1	63-125	70 V	Siemens, Isocom
SFH600-2	100-200	70 V	Siemens, Isocom
PC702V2	63-125	70 V	Sharp
PC702V3	100-200	70 V	Sharp
PC714V1	80-160	35 V	Sharp
6 Pin Dip, 8 mm Spacing			
PC110L1	50-125	35 V	Sharp
PC112L2	80-200	70 V	Sharp
CNY17G-2	63-125	32 V	Temic
CNY17G-3	100-200	32 V	Temic
6 pin DIP, No Base Connection, 8mm Spacing			
MOC8101	50-80	30 V	Motorola, Isocom
MOC8102	73-117	30 V	Motorola, Isocom
MOC8103	108-173	30 V	Motorola, Isocom
CNY17F-2	63-125	70 V	Siemens, Quality Technologies, Isocom
CNY17F-3	100-200	70 V	Siemens, Quality Technologies, Isocom
CNY75A	63-125	90 V	Temic
CNY75B	100-200	90 V	Temic
6 pin DIP, No Base Connection			
PC111L1	50-125	35 V	Sharp
PC113L2	80-200	70 V	Sharp
CNY75GA	63-125	90 V	Temic
CNY75GB	100-200	90 V	Temic
4 pin DIP			
PC816A	80-160	70 V	Sharp
PC817A	80-160	35 V	Sharp
SFH 610A-2	63-125	70 V	Siemens
SFH 610A-3	100-200	70 V	Siemens
PS2501-H	80-160	40 V	NEC

Table 3: Suggested Optocouplers with CTR Between 50 and 200.

17. Input Undervoltage Lockout Circuitry

17.1 Optocoupler Feedback Control

Figure 16 shows a circuit for implementing input undervoltage lockout with optocoupler feedback control. This circuit holds the Control pin voltage (V_C) low through D5 and Q1 until the voltage at the base of transistor Q1 set by the R6-R7 voltage divider exceeds approximately 4.4 Volts. This circuit prevents *TOPSwitch* from starting until the DC input voltage V_{DC} across C1 is high enough for regulation. When V_{DC} is low, base current through R7 biases PNP transistor Q1 on and holds the *TOPSwitch* Control voltage below the internal UV lockout threshold voltage (typically 4.7 Volts). As V_{DC} rises, the Q1 base voltage will rise high enough to cut off Q1 and allow the power supply to start. For example, for R6 of 1 MΩ, transistor base emitter voltage (V_{BE}) and diode voltage (V_D) of 0.65 V, and V_{DC} of 100 V, R7 is found to be 46.4 kΩ. During steady state operation, diode D5 is reverse biased and Q1 may be on with current limited by R8. To minimize power dissipation, bias voltage V_{BIAS} can be set to as low as 12 V or an optional resistor can be inserted between the emitter of Q1 and V_{BIAS}.

When AC input voltage is removed, V_{DC} decreases as C1 discharges until output voltage V_O falls out of regulation and allows C5 to discharge. The discharge current through Q1 and D5 is set by R8 to a value larger than the internal Control Pin Charging Current (I_C) to ensure that the Control pin voltage will be pulled below the internal UV Lockout Threshold Voltage to turn *TOPSwitch* off. Q1 continues to hold the Control pin voltage low until AC input voltage is applied and V_{DC} becomes high enough for the power supply to regulate again.

$$R_7 = R_6 \times \frac{V_C - V_{BE} - V_D}{V_{DC} - (V_C - V_{BE} - V_D)}$$

$$= 1M \times \frac{4.4}{100 - 4.4}$$

$$\cong 46.4\ k\Omega$$

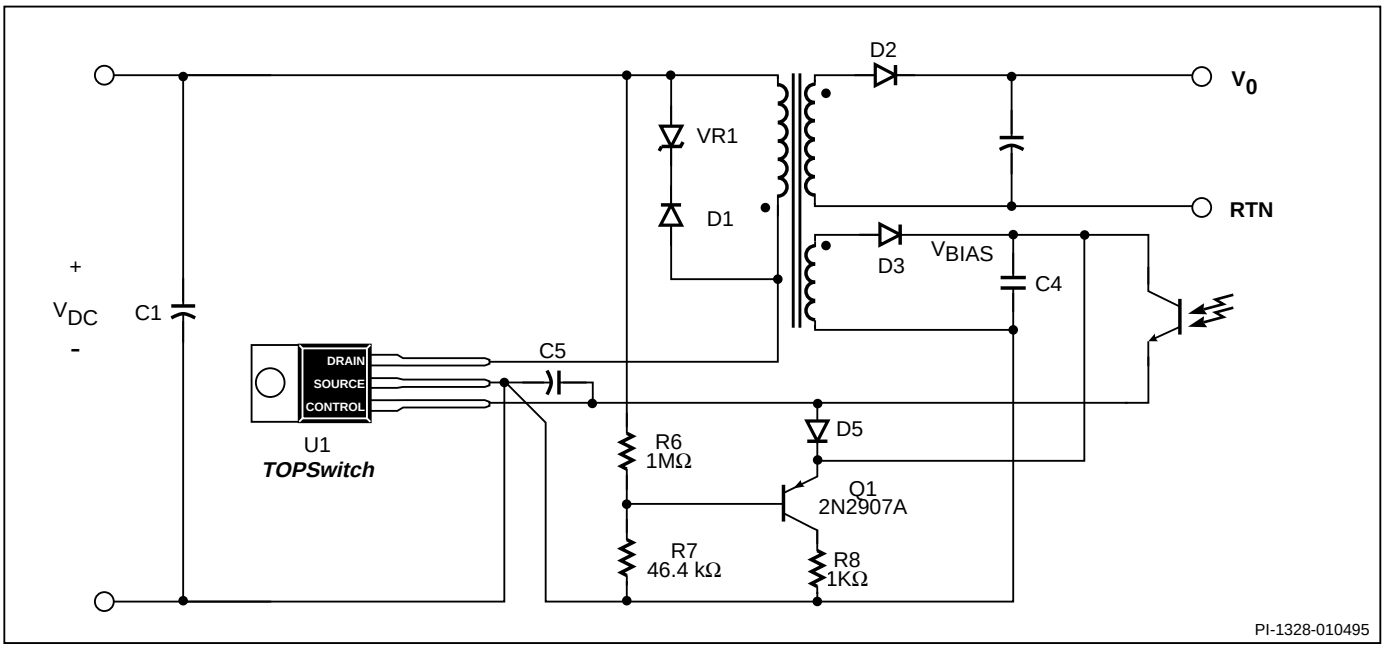

Figure 16. Input Under Voltage Lockout Circuitry for Optocoupler Feedback Control.

17.2 Bias Winding Feedback Control

Figure 17 shows a circuit for implementing input undervoltage lockout with Bias Winding Feedback Control. This circuit holds the Control pin voltage (V_C) low through Q1 until the voltage at the cathode of D4 set by the R6-R7 voltage divider exceeds approximately 4.4 Volts. This circuit prevents *TOPSwitch* from starting until the DC input voltage V_{DC} across C1 is high enough for regulation. When V_{DC} is low, base current through D4 and R7 biases PNP transistor Q1 on and holds the *TOPSwitch* Control voltage below the internal UV lockout threshold voltage (typically 4.7 Volts). As V_{DC} rises, the voltage at the cathode of D4 will rise high enough to cut off Q1 and allow the power supply to start. Use the equation from section 17.1. For example, for R6 of 1MΩ, transistor base emitter voltage (V_{BE}) and diode voltage (V_D) of 0.65 V, and V_{DC} of 100 V, R7 is found to be 46.4 kΩ. Q1 is cut off during steady state operation and D4 prevents excessive reverse base emitter voltage.

When AC input voltage is removed, V_{DC} decreases as C1 discharges until output voltage V_O falls out of regulation and allows C5 to discharge. The discharge current through Q1 is set by R8 to a value larger than the internal Control Pin Charging Current (I_C) to ensure that the Control pin voltage will be pulled below the internal UV Lockout Threshold Voltage to turn *TOPSwitch* off. Q1 continues to hold the Control pin voltage low until AC input voltage is applied and V_{DC} becomes high enough for the power supply to regulate again.

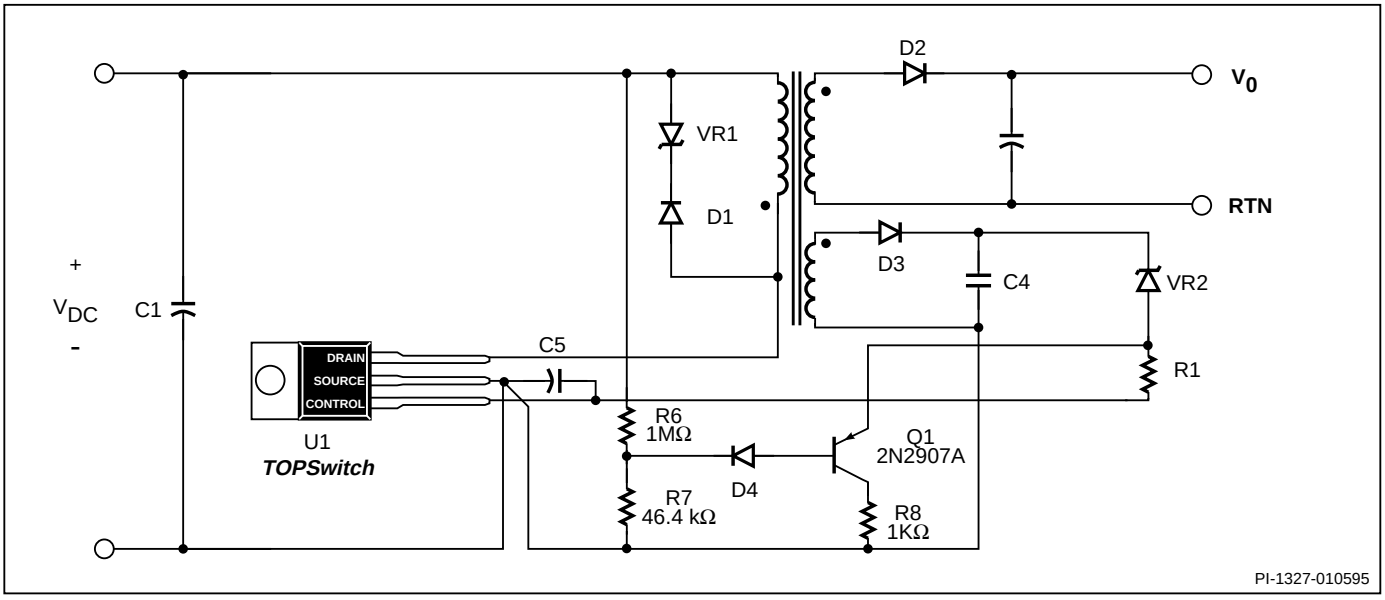

Figure 17. Input Under Voltage Lockout Circuitry for Bias Winding Feedback Control.

18. Doubler Input for Increased Output Power

Figure 18 shows a voltage doubler circuit for generating a nominal 300 Volt DC bus from 110 VAC input. Removing jumper J1 allows the circuit to operate as a full wave bridge rectifier from 230 VAC input. Both capacitors are rated for 200 to 250 Volts DC with approximately 2 µF for each Watt of output power. Because of capacitor DC leakage current, balance resistors may be necessary to keep the voltage across each capacitor equal and within rating. For 100/110V only operation, D_A, D_B, R_A and R_B can be removed to reduce cost.

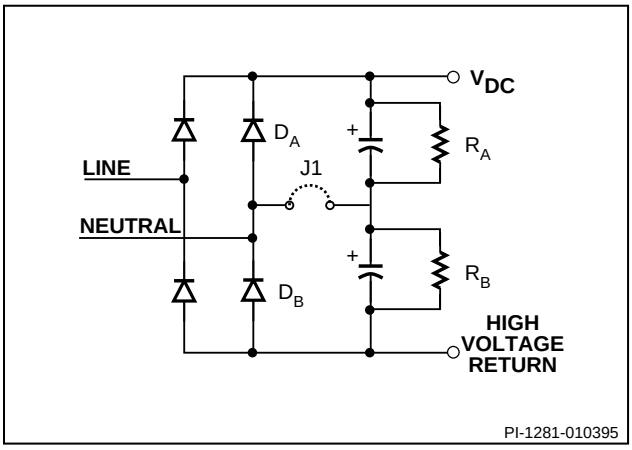

Figure 18. Voltage Doubler.

19. Power Factor Correction (PFC)

Nominal output power ranges for PFC applications are given in Table 4 for each *TOPSwitch*. Refer to DN-7 for recommended inductance and precompensation resistance values.

Part #	PFC Output Power 230/277 VAC Input
TOP200	0 - 25 W
TOP201	20 - 50 W
TOP202	30-75 W
TOP203	50 - 100 W
TOP214	60 - 125 W
TOP204	75 - 150 W
Part #	**PFC Output Power 110 VAC Input**
TOP100	0 - 30 W
TOP101	25 - 50 W
TOP102	35 - 70 W
TOP103	45 - 90 W
TOP104	55 - 110 W

Table 4. Recommended PFC Output Power Ranges.

19.1 Reverse Drain Voltage

Do not allow the Drain voltage to ring below the Source. Add a fast recovery, high voltage (200 to 400 V) diode (D2 in Figure 19) in series with the Drain when using *TOPSwitch* in a PFC circuit. Negative voltages on the Drain will forward bias the output MOSFET body diode and trigger the internal shutdown latch. Recycling input power or shorting the Control pin to the Source pin will be necessary to restart *TOPSwitch*.

19.2 Auto-Restart

In PFC applications, precompensation resistor R1 (Figure 19) drives sufficient current into the Control pin to overcome the discharge current and effectively stalls auto-restart. If the PFC circuit does not start the first time, an overload condition exists, or a short input power interruption occurs, *TOPSwitch* will enter and stall in auto-restart. Adding a parallel resistor between typically 2.7 kΩ and 6.8 kΩ across C3 provides an additional discharge path allowing the auto-restart circuit to function properly. C3 may have to be adjusted for proper auto-restart timing.

19.3 Example Power Factor Correction Circuit

The circuit shown in Figure 19 operates from 230 VAC input with typically 0.985 power factor and 8% Total Harmonic Distortion (THD) while providing 65 Watts of output power at 410 VDC. Bridge Rectifier BR1 full wave rectifies the AC input voltage. L1, D1, C4, and *TOPSwitch* make up the boost power stage. D2 prevents reverse current through the *TOPSwitch*

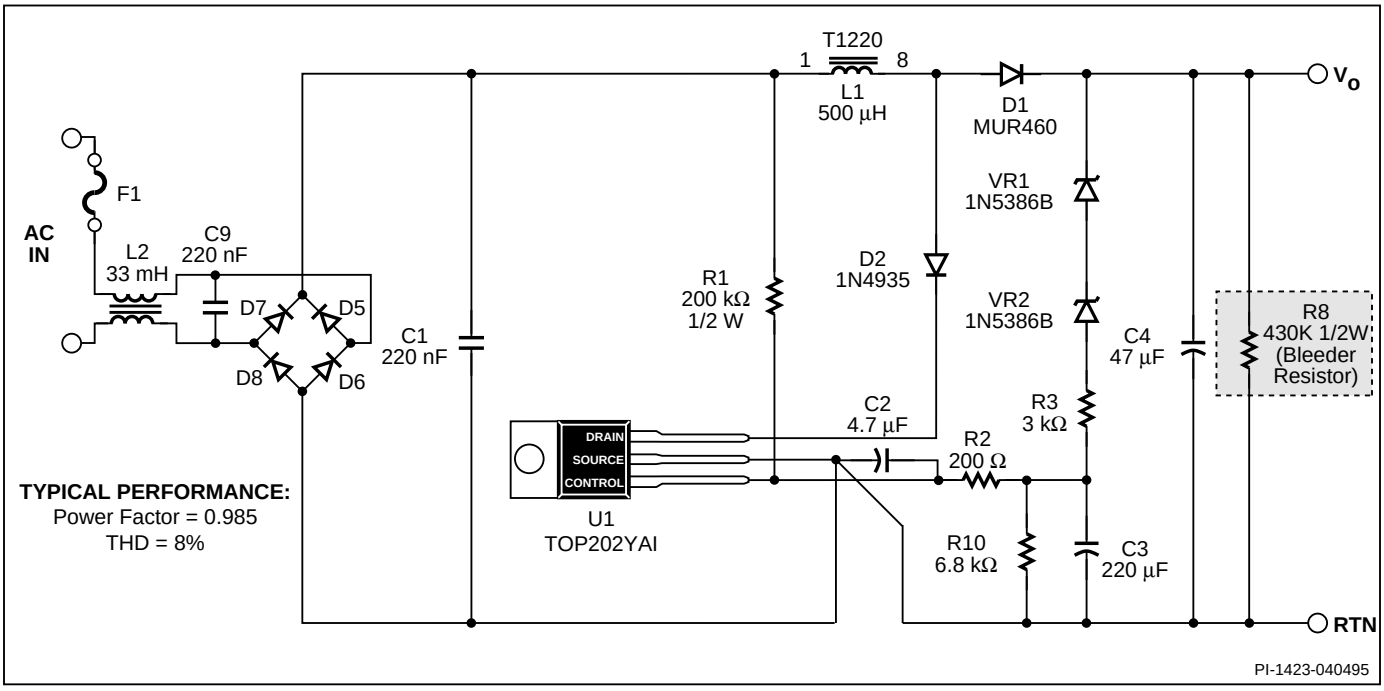

Figure 19. Schematic Diagram of a 65W, 230 VAC Input Boost Power Factor Correction Circuit Utilizing the TOP202.

19.3 Example Power Factor Correction Circuit (continued)

body diode. R1 generates a precompensation current proportional to the instantaneous rectified AC input voltage which directly varies the duty cycle. C2 filters high frequency switching currents while having no filtering effect on the line frequency precompensation current from the large filter capacitor C3 to prevent an averaging effect which would increase total harmonic distortion. C1 filters high frequency noise currents which could cause errors in the precompensation current.

When the Output voltage becomes regulated, series connected Zener diodes VR1 and VR2 drive current into the *TOPSwitch* control pin and directly control the duty cycle. C3 together with R3 perform low pass filtering on the feedback signal to prevent output line frequency ripple voltage from varying the duty cycle.

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WORLD HEADQUARTERS
Power Integrations, Inc.
477 N. Mathilda Avenue
Sunnyvale, CA 94086
USA
Main: 408•523•9200
Customer Service:
Phone: 408•523•9265
Fax: 408•523•9365

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EUROPE & AFRICA
Power Integrations (Europe) Ltd.
Mountbatten House
Fairacres
Windsor SL4 4LE
United Kingdom
Phone: 44•(0)•1753•622•208
Fax: 44•(0)•1753•622•209

JAPAN
Power Integrations, K.K.
Keihin-Tatemono 1st Bldg.
12-20 Shin-Yokohoma 2-Chome, Kohoku-ku
Yokohama-shi, Kanagawa 222 Japan
Phone: 81•(0)•45•471•1021
Fax: 81•(0)•45•471•3717

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Other _____

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Please fill in Application Parameters:

AC Input Voltage _____ to _____

DC Input Voltage _____ to _____

Output Power, Steady State _____

Output Power, Peak _____

EMI Specification _____

Safety Specification _____

	Output Voltage	Steady State Output Current	Peak Output Current
1)	_____	_____ to _____	_____
2)	_____	_____ to _____	_____
3)	_____	_____ to _____	_____
4)	_____	_____ to _____	_____