Interfacing Various Bit-size DRAMs to the H8/300H

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TN-0154

The H8/300H microcontroller family facilitates the task of interfacing various types of memory devices within its linearly addressed memory map. In particular, dynamic random access memories can be easily connected given the addition of a Refresh Controller module into the H8/300H chip which provides properly timed control signals (RAS, CAS, WE, RD) as to insure smooth access and refresh cycles. In addition, external device decoding logic is kept to a bare minimum since the microcontroller provides chip select signals for each memory block area. The H8/3003 Hardware Manual, Application Note AE-0043, and technote TN-0131 discuss in detail how x16 DRAMs can be interfaced to the H8/3003 as well as the necessary timing considerations. This technote will illustrate how other DRAM parts can be properly connected to the microcontroller.

DRAMs of x1, x4 and x8 bit-size can also be directly (or with a minimum amount of glue logic) attached to the H8/300H family. Figure 1 below shows bit-by-bit how the Refresh Control Register (RFSHCR) must be programmed for these particular interfaces. The CAS/WE bit can be programmed either way since no byte control is required. If this bit is set, then the CAS signal will be provided through both HWR and LWR pins, and the WE signal will be provided via the RD line. If the CAS/WE bit is cleared, the CAS signal will be available at the RD pin, and the WE signal can be wired from either the HWR or the LWR pins of the H8/300H. The M9/M8 bit must be set to 1 for DRAM devices that use 9-bit or higher column address mode; most x1, x4, and x8 available DRAMs use this mode.

7	6	5	4	3	2	1	0
SRFMD	PSRAME	DRAME	CAS/WE	M9/M8	RFSHE	Reserved	RCYCE
X	0	1	0 or 1	0 or 1	X	1	X

Figure 1. Refresh Control Register Settings.

Figures 2-8 show the following examples of generic x4 and x8 bit-size DRAM connections via either 8-bit or 16-bit data bus along with its corresponding memory map for the 16MByte expanded modes:

Example 1 (fig. 2-3):

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A Hitachi HM514800 512K x 8 is interfaced to the H8/300H via an 8-bit data bus. Since the DRAM uses a 10 rows x 9 columns addressing mode, lines A0 - A9 will provide the row address, and lines A1 - A9 will output the column address. A0 is connected to pin A9 of the DRAM since its state remains unchanged during both row and column addressing. The CAS signal is obtained from the HWR line of the microcontroller, and the WE signal is provided at the RD pin (assuming the CAS/WE bit of RFSHCR is set). The RAS pin of the H8/300H is connected to the CAS pin of the DRAM since these signals are multiplexed inside the microcontroller. Given this hardware configuration, the addressable DRAM memory occupies 512KBytes between H'600000 and H'67FFFF.

Example 2 (fig. 3-4):

Four Hitachi HM514256 256K x 4's are connected to the H8/300H via a 16-bit data bus. The RAS, CAS, and WE signals are provided as described in the example above. Since the DRAM uses a 9 rows x 9 columns addressing mode, lines A1 - A9 will provide both row and column address. The A0 line from the H8/300H is not connected since word accesses are performed (see explanation in AE-0043). The addressable DRAM memory occupies the same boundaries as in the previous example.

Example 3 (fig. 5-6):

Two Hitachi HM514800 512K x 8's are interfaced to the H8/300H via a 16-bit data bus. The RAS, CAS, and WE signals are provided as described in the previous examples. The DRAMs use a 10 row x 9 column addressing mode. One device will store the upper bytes, and the other will contain the lower bytes. A0 is not connected since word accesses are performed. Therefore, the row address will be provided through lines A1 - A9 and A19, while the column address via lines A1 - A9. The memory is mapped identically to the previous examples.

Example 4 (fig. 7-8):

Two Hitachi HM514800 512K x 8's are connected to the H8/300H via an 8-bit data bus. The CAS and WE signals are provided as described in the previous examples. Since the first DRAM will contain the 512KBytes between H'600000 and H'67FFFF, and the second device will contain the remaining 512KBytes between H'680000 and H'6FFFFF, additional decoding logic is necessary. The first device must be enabled for either byte transfers (if A19 = 0 and CS3 goes low), or for refresh cycles (if A19=0 and both CS3 and RFSH go low). The second DRAM must be enabled for byte transfers or refresh cycles if A19=1. The address lines are connected as described in example 1.

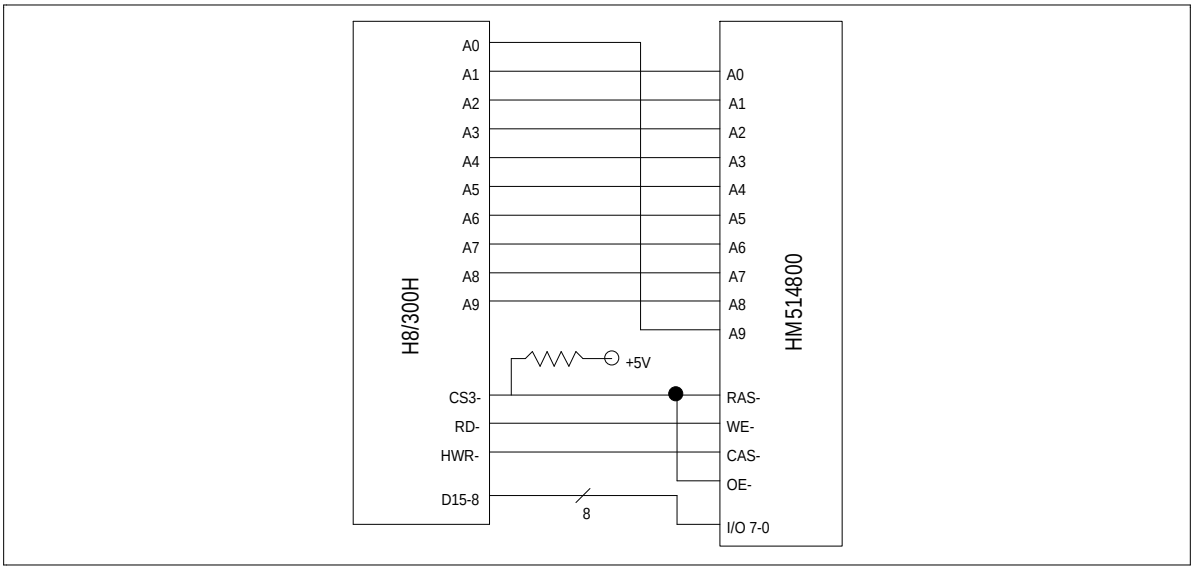

Fig. 2. DRAM Connection

Fig. 3. Memory Mapping

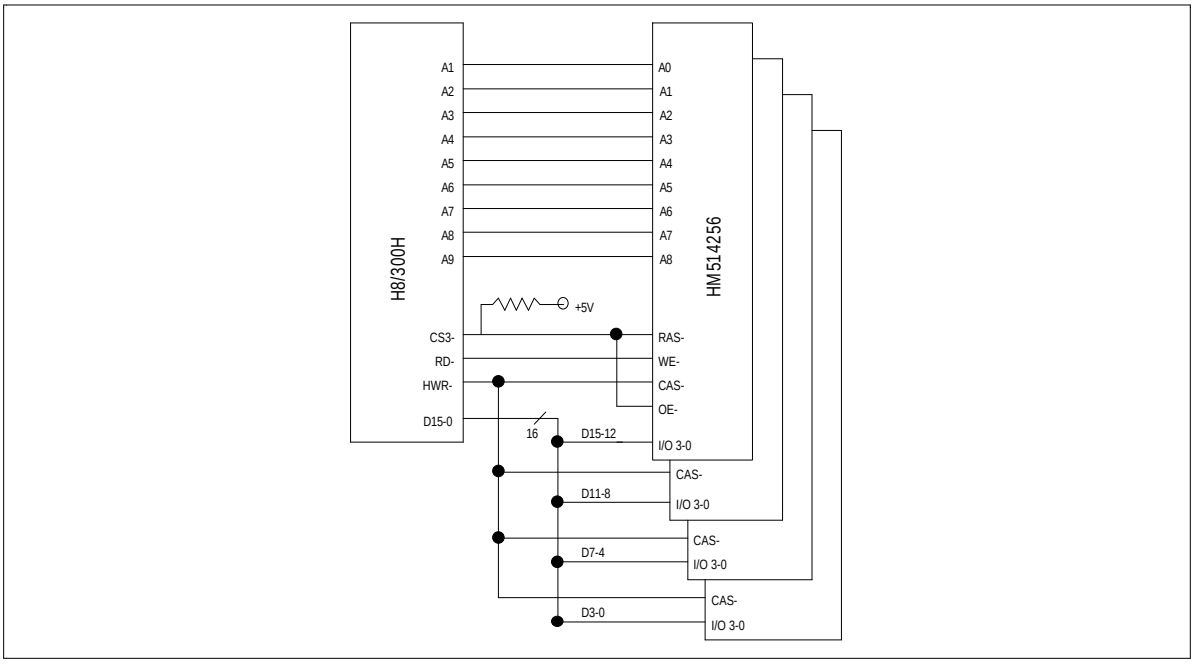

Fig. 4. DRAM Connection

Fig. 5. Memory Mapping

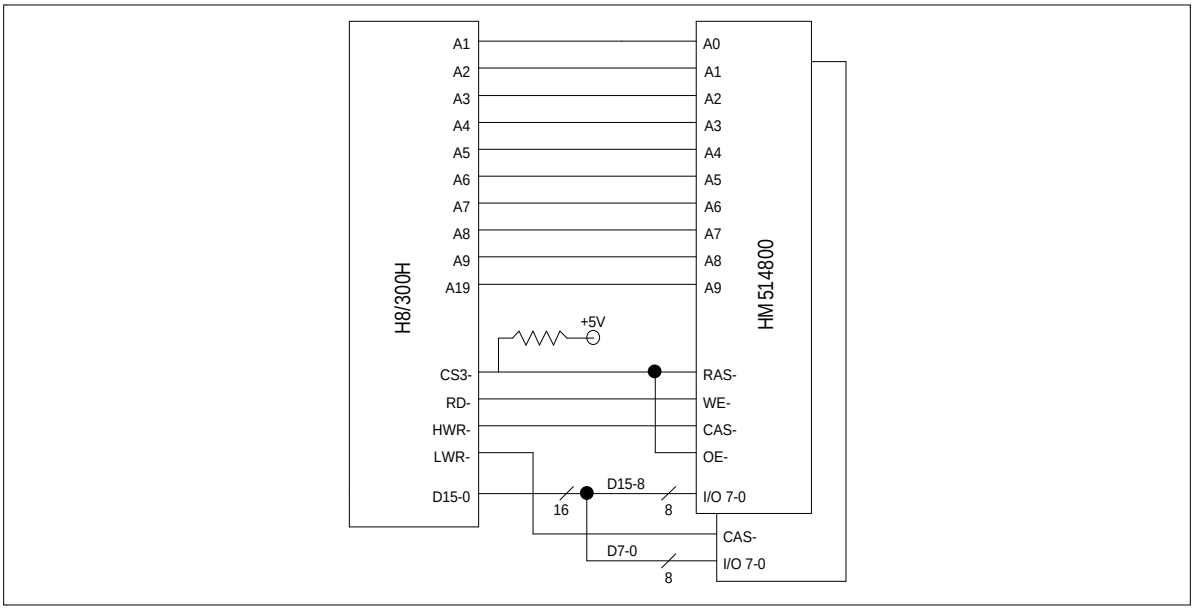

Fig. 6. DRAM Connection

Fig. 7. Memory Mapping

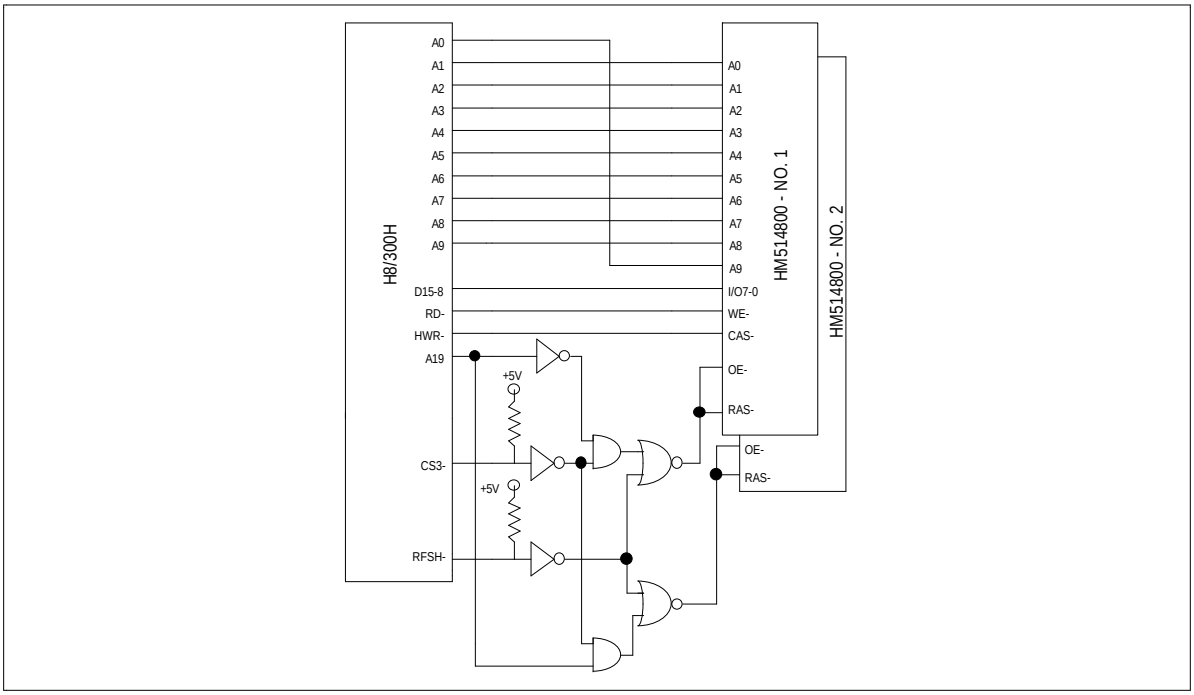

Fig. 8. DRAM Connection

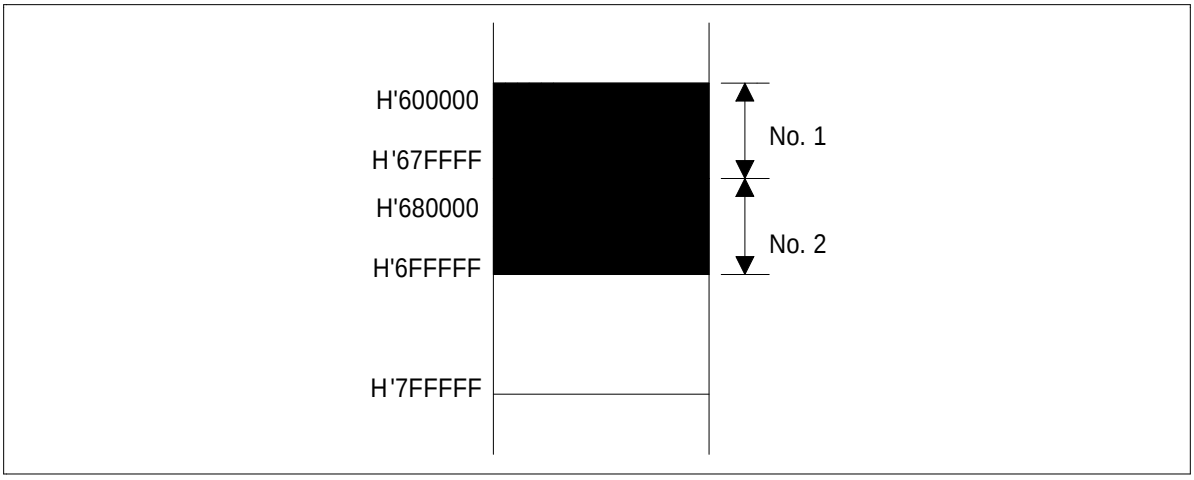

Fig. 9. Memory Mapping