Application Note 47

PACMan Circuit Ideas

NOVEL CLOCK MANAGEMENT

The Programmable Adaptive Clock Manager (PACMan) circuits offered by Micro Linear give the design engineer the ability to lay out clock systems with minimal consideration to trace length. The elegance of the clock managers is that all the clock inputs are driven simultaneously, even though the clocks are located different distances from the clock manager. Questions have arisen about the operation of the adaptive clock managers. This application note provides answers to those questions and provides some circuit ideas, such as increasing the output drive and generating 64 clocks deskewed within 1ns. Further reference material is available in Application Note 21 and the data sheet.

POWER UP SEQUENCE — ML6508

The ML6508 clock manager generates eight clock signals that are individually phased so that all their rising edges arrive at their respective clock loads within 500ps. The operating method by which this is achieved is as follows. First, power is applied to the power input pins, and then a clock — either TTL or PECL — is applied to the CLKINH and CLKINL pins. Using these clock inputs, the ML6508 creates two internal reference clocks called “Zero Delay” and “Max Delay” that have the programmed output frequency. Max Delay follows Zero delay by 5ns. The Max Delay clock is the reference for all eight clock signals (more on this later). Max Delay is fed back to the system PLL where it is locked to the clock input at CLKINH and CLKINL, minimizing input propagation delay. Zero Delay actually precedes the clock input and Max Delay. The time for the system PLL to lock is about 4ms The Max Delay clock is fed to the Phase Detector input of the eight deskew buffers. The Zero Delay clock is fed to the voltage control delay input of the eight deskew buffers. When the Zero Delay is present at the voltage control delay input, the buffers begin to generate output clocks with no phase shift.

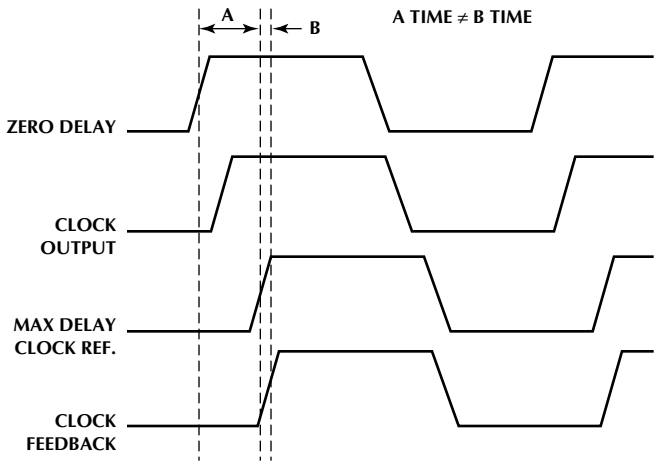


Figure 1. At start up the Clock Output is not delayed so the clocks are variously skewed.

Each clock signal travels down the output trace to the clock load, and then returns to the ML6508 via the feedback trace. The output trace and the feedback trace must each be of equal length so that their contribution to the delay is equal. When the Clock Output begins, a Phase Detector inside the deskew buffer begins to accumulate the high logic overlap of the Max Delay clock and the Clock Output. When the Clock Feedback signal arrives at the deskew buffer, the Phase Detector accumulates the high logic overlap of the Max Delay clock and the Clock Feedback. The difference in overlap determines which way the voltage controlled delay will adjust the clock output. If the Clock Output overlaps the Max Delay greater than Clock Feedback then the output delay is reduced. If the Clock Feedback overlaps the Max Delay greater than Clock Output then the output delay is increased. The overlaps are equal when the output delay is constant. This condition is met when the center of the phase difference between the Output Clock signal and the Clock Feedback is locked on the clock reference, Max Delay. The time for all the deskew buffers to stabilize is about 7ms.

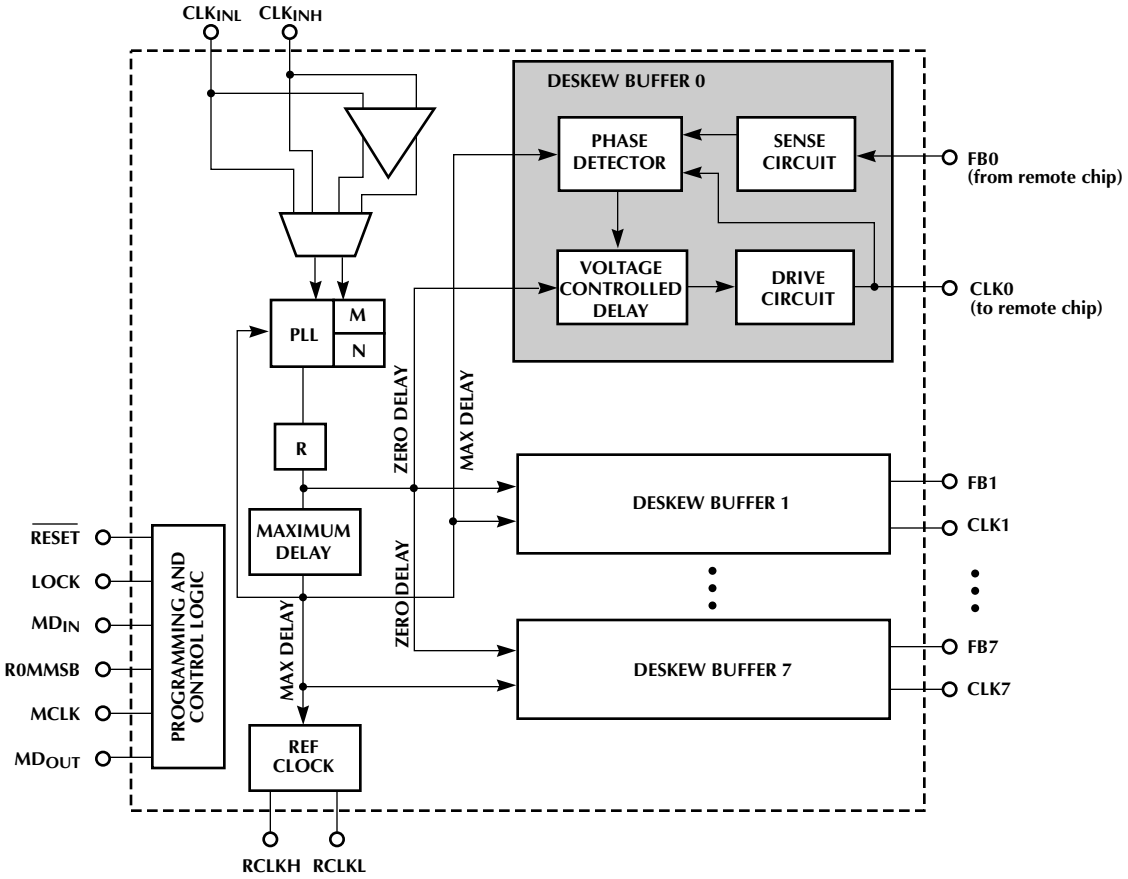


Figure 2. ML6510 Block Diagram

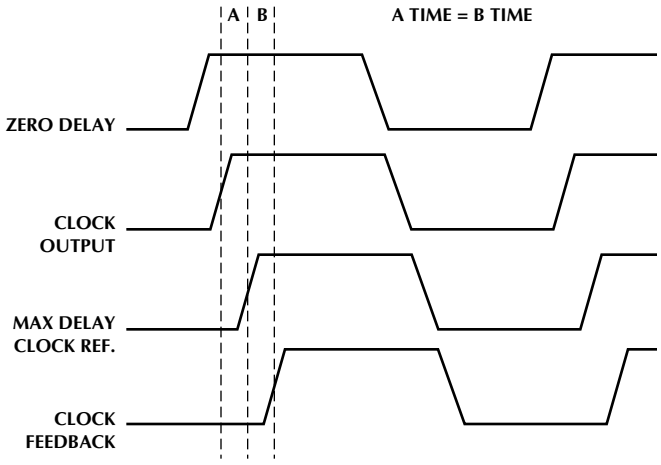


Figure 3. The clock signal is deskewed with respect to the other clocks when Max Delay is phase locked equally between the Clock Output and Clock Feedback

THE FEEDBACK SIGNAL — ML6508

Unequal Lengths

The feedback trace must be equal in length to the output trace for proper deskewing to take place. If the system requires a clock signal to arrive 0.5ns earlier than the other clock signals then the feedback trace can be modified to accomplish this. The propagation velocity on a fiberglass PCB is about 0.144ns per inch. The clock signal will arrive 0.5ns earlier if the feedback trace is 7" longer than the output trace. This feedback timing imbalance tricks the ML6508 into sending the clock signal earlier.

$$\text{Extra Length} = \left(\frac{\text{Required Delay Time}}{0.144\text{ns/inch}}\right) \times 2 \qquad (1)$$

Terminated Loads

Terminating at the Clock Loads doesn't affect the deskewing as long as the feedback signal exceeds the input threshold for the feedback buffer. The threshold level is 1.5V. Remember that the input to the feedback pin must be terminated with a 80/130Ω terminator which is a 50Ω thevienin equivalent. (see Figure 6).

Extra Buffers

The insertion of a buffer into the clock signal path on the output trace is allowed as long as the feedback trace has a matched buffer. The maximum delay that can be deskewed is 10ns. The propagation of the clock signal on the PCB trace and the combined buffers' propagation delay must be taken into account when determining the total round trip time.

EXTRA LONG TRACES

Longer traces can be driven when the time to complete the round trip falls within regions called lock zones. The ML6508 requires a high clock feedback signal when the Clock Output is high to determine the phase relation. If the Output Clock goes low before the Clock Feedback goes high the ML6508 will be unable to determine the proper phase. If the proper phase relation is determined the ML6508 can delay the output so that the clock loads are deskewed. It is possible to deceive the ML6508 by making the round trip time equal to an integer multiple of the period plus one half of the clock period, or mathematically stated:

$$\text{Round Trip Time} = \text{Clock Period} \times N + \frac{1}{2}\,\text{Clock Period} \qquad (2)$$

In this situation, the deskew buffer compares the 2nd high clock period of the Clock Output to the 1st high clock period at the Clock Feedback.

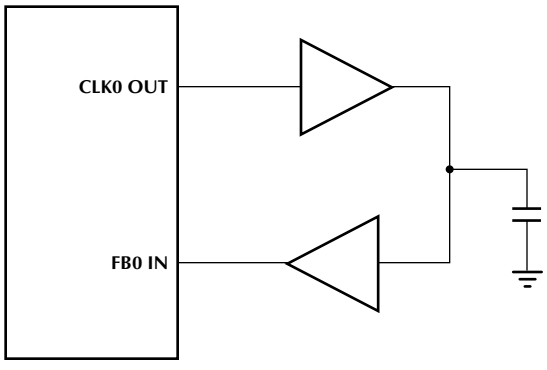


Figure 4. An extra buffer can be added to increase the output drive capability as long as a matched buffer delay is added to the feedback path.

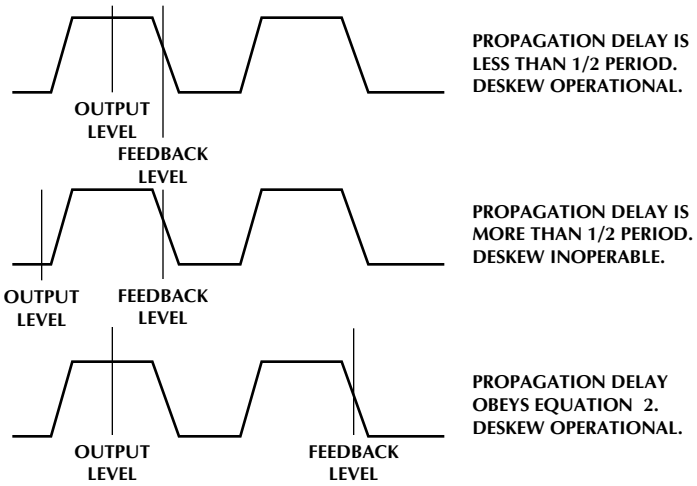


Figure 5. The ML6508 can drive longer clock traces when the PCB design takes into account the timing relationship between the output pin and the feedback pin.

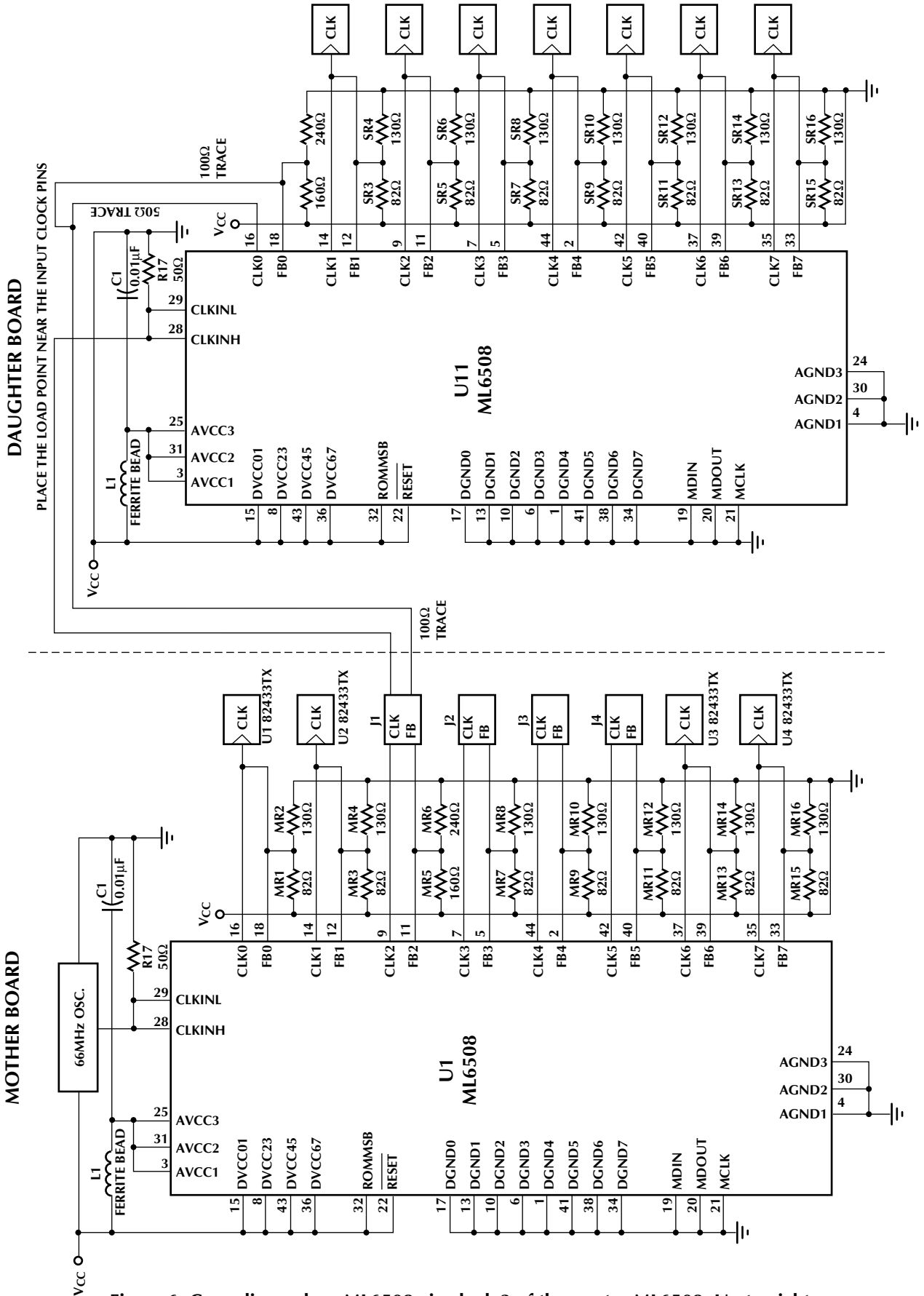


Figure 6. Cascading a slave ML6508 via clock 2 of the master ML6508. Up to eight slaves can be added to the master, producing 56 clock outputs with a 1ns deskewed range.

SLAVE DEVICE — ALTERNATE METHOD

A second ML6508 can be cascaded in one of two ways. Connecting the output reference clock pins of the master device to the input clock pins of the slave device is the simplest circuit for cascading two devices. An alternative method drives the slave TTL clock input with a clock output from the master ML6508. An output of the slave device is then routed to put its load near the clock input of the slave device. The feedback trace for the master clock is then derived from this load point. This circuit eliminates the clock delay introduced by the slave device input clock section. By eliminating the delay multiple device clocks can be deskewed to within 1000ps. The typical deskew of an ML6508 is 400ps, which means a typical deskew range for a system of 800ps. This enables the placement of slave clock drivers on daughter boards or on other boards.

POWER UP SEQUENCE — ML6510

The ML6510 clock manager powers up internally exactly like the ML6508 (See Power Up Sequence — ML6510). The only differences are the output and feedback circuits described below.

Each clock signal has a 50Ω source and drives the 50Ω trace to one half of the clock voltage. When the clock edge gets to the load the clock edge reflects back positively because the load is a high impedance. The reflected wavefront brings the voltage up to the total clock voltage and returns to the ML6510's feedback pin. When the Clock Output begins, a Phase Detector inside the deskew buffer begins to accumulate the high logic overlap of the Max Delay clock and the Clock Output. When the Clock Feedback signal arrives at the deskew buffer, the Phase Detector accumulates the high logic overlap of the Max Delay clock and the Clock Feedback. The difference in overlap determines which way the voltage controlled delay will adjust the clock output. If the Clock Output overlaps the Max Delay greater than Clock Feedback then the output delay is reduced. If the Clock Feedback overlaps the Max Delay greater than Clock Output then the output delay is increased. The overlaps are equal when the output delay is constant. This condition is met when the center of the phase difference between the Output Clock signal and the Clock Feedback is locked on the clock reference, Max Delay. The time for all the deskew buffers to stabilize is about 7ms.

THE FEEDBACK SIGNAL — ML6510

Single Trace

The output/feedback trace must be a 50Ω transmission line for proper deskewing to take place. Unintentional impedance mismatches should not be great enough to cause a reflected waveform to trigger the feedback. The threshold level is 3.25V for the 80MHz part. If the system requires a clock signal to arrive 0.3ns earlier than the other clock signals, then the transmission trace should continue beyond the load by 2". The propagation velocity on a fiberglass PCB is about 0.144ns per inch. The clock signal will arrive 0.3ns earlier from the end of the trace. This trace extension allows the clock signal to arrive earlier at the load than at the end of the trace.

Terminated Loads

Terminating at the Clock Loads with a 50Ω impedance will load the output so the feedback threshold is not exceeded. A 50Ω termination will load the clock output to 2.5V.

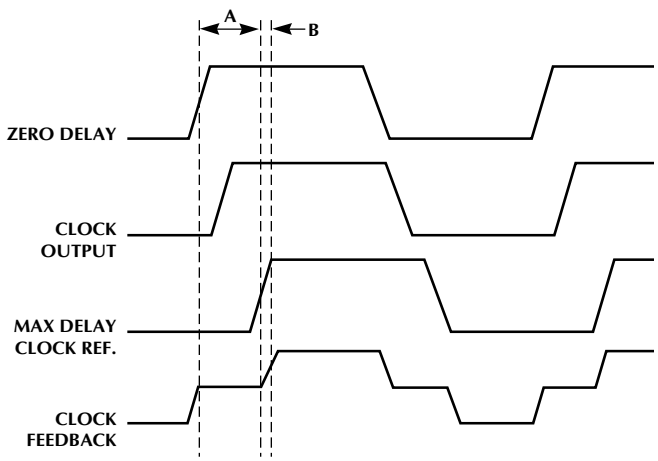


Figure 7. At start up the clock output is "Zero Delay" and the clock is unskewed.

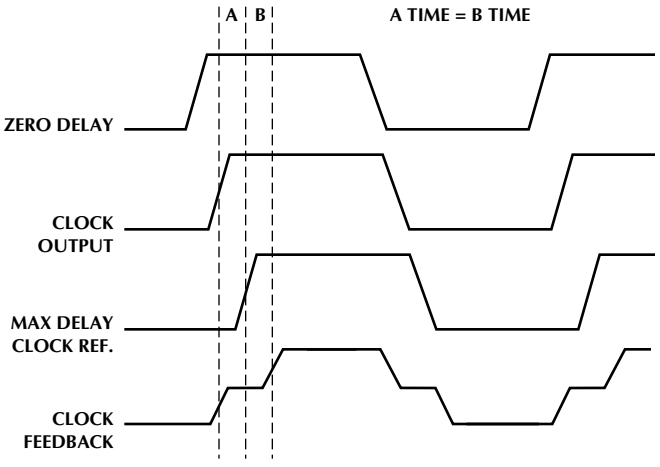
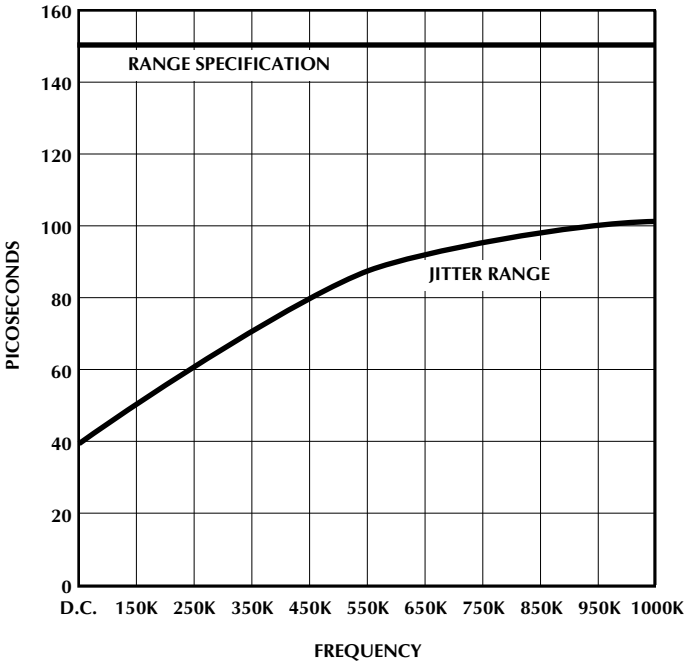


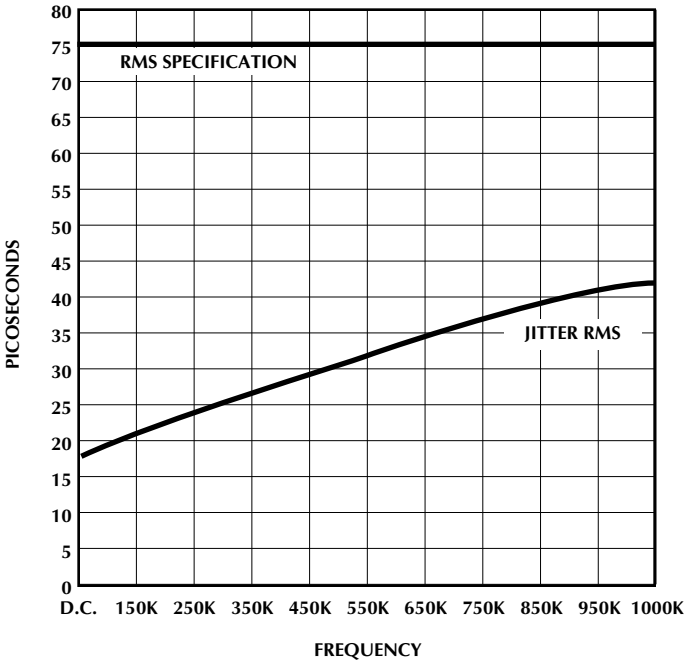
Figure 8. The clock signal at C_L is deskewed with respect to the other clocks when Max Delay is phase locked equally between the Output Clock the Feedback Clock.

Noise Immunity

PACMan products exhibit high immunity to power supply noise. There are many sources of noise from external sources to inner-system sources. The frequency components of noise sources can vary widely. A comprehensive attempt to expose the PACMan devices to real world transients would be excessive. Controlled frequencies at 200mV were injected into the various PACMan EVAL kits to determine the effect of noise on the power supply. The frequency range from 100kHz to 1MHz was swept in 50kHz increments. The jitter was measured with a network time analyzer. The clock period was measured 5000 times and standard deviation (RMS) and min./max. range were obtained. The results are plotted in graphs 1 and 2.



Graph 1. Jitter range versus frequency



Graph 2. RMS Jitter versus Injected Frequency

Note: The "Range Specification" in Graph 1 and "RMS Specification" in Graph 2 are for environments in which there is no noise.

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