NX25F011B
NX25F021B
NX25F041B

NexFlash® Technologies, Inc.

1M-BIT, 2M-BIT, AND 4M-BIT SERIAL FLASH MEMORIES WITH 4-PIN SPI INTERFACE

PRELIMINARY
JUNE 2000

FEATURES

- **Flash Storage for Resource-Limited Systems**
  - Ideal for portable/mobile and microcontroller-based applications that store voice, text, and data
- **0.35µ *NexFlash* Memory Technology**
  - 1M/2M/4M-bit with 512/1024/2048 sectors
  - Small 264-byte sectors
  - Erase/Write time of 5 ms/sector (typical)
  - 10K (Sector) / 100K (Block) write cycles
  - Optional 8KB (32 sector) block erase for faster programming
- **Ultra-low Power for Battery-Operation**
  - Single 5V or 3V supply for read and erase/write
  - 1 µA standby current, 5 mA active @ 3V (typical)
  - Low frequency read command for lower power
- **4-pin SPI Serial Interface**
  - Easily interfaces to popular microcontrollers
  - Clock operation as fast as 16 MHz
- **On-chip Serial SRAM**
  - Single 264-byte Read/Write SRAM buffer
  - Use in conjunction with or independent of Flash
  - Off-loads RAM-limited microcontrollers
- **Special Features for Media-Storage Applications**
  - Byte-level addressing for reads and SRAM writes
  - Transfer or compare sector to SRAM
  - Versatile hardware and software write-protection
  - In-system electronic part number option
  - Removable Serial Flash Module package option
  - Auto verify for increased endurance
  - Serial Flash Development Kit

DESCRIPTION

The NX25F011B, NX25F021B, and NX25F041B Serial Flash memories provide a storage solution for systems limited in power, pins, space, hardware, and firmware resources. They are ideal for applications that store voice, text, and data in a portable or mobile environment. Using *NexFlash's* patented single transistor EEPROM cell, the devices offer a high-density, low-voltage, low-power, and cost-effective non-volatile memory solution. The devices operate on a single 5V or 3V (2.7V-3.6V) supply for Read and Erase/Write with typical current consumption as low as 5 mA active and less than 1 µA standby. Sector erase/write speeds as fast as 5 ms increase system performance, minimize power-on time, and maximize battery life.

The NX25F011B, NX25F021B, and NX25F041B provide 1M-bit, 2M-bit, and 4M-bit of flash memory organized as 512, 1024, or 2048 sectors of 264 bytes each. Each sector is individually addressable through basic serial-clocked commands. The 4-pin SPI serial interface works directly with popular microcontrollers. Special features include: on-chip serial SRAM, byte-level addressing, double-buffered sector writes, transfer/compare sector to SRAM, hardware and software write protection, alternate oscillator frequency, electronic part number, and removable Serial Flash Module package option. Development is supported with the PC-based SFK-SPI Serial Flash Development Kit.

FUNCTIONAL OVERVIEW

An architectural block diagram of the NX25F011B, NX25F021B, and NX25F041B is shown in Figure 2. Key elements of the architecture include:

- SPI Interface and Command Set Logic
- Serial Flash Memory Array
- Serial SRAM and Program Buffer
- Write Protection Logic
- Configuration and Status Registers
- Device Information Sector

Pin Descriptions

Package

The NX25F011B, NX25F021B, and NX25F041B are available in a 28-pin TSOP (Type I) surface mount package. The NX25F011B and NX25F021B are available in either an 8-pin SOIC and a 14-pin TSOP package (contact NexFlash for information on the 14-pin TSOP package). See Figure 3A, 3B and Table 1 for pin assignments. All interface and supply pins are on one side of the TSOP package. The "No Connect" (NC) pins are not connected to the device, allowing the pads and the area around them to be used for routing PCB system traces. The devices are also available in a cost-effective and space-efficient removable Serial Flash Module package.

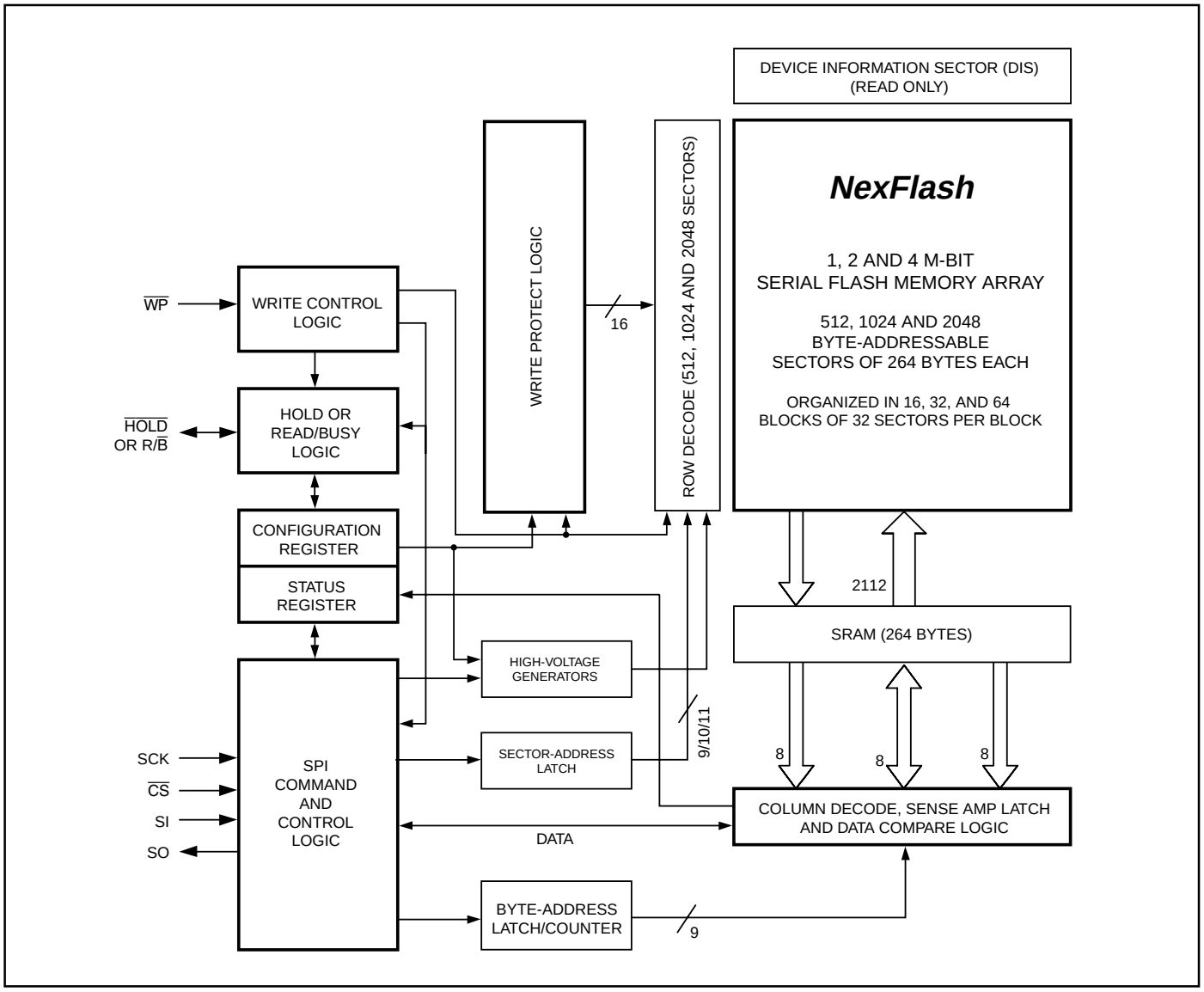


Figure 2. NX25F011B, NX25F021B, and NX25F041B Architectural Block Diagram

Serial Data Input (SI)
The SPI bus Serial Data Input (SI) provides a means for data to be written to (shifted into) the device.

Serial Data Output (SO)
The SPI bus Serial Data Output (SO) provides a means for data to be read from (shifted out of) the device during a read operation. When the device is deselected ($\overline{CS}$=1 or $\overline{HOLD}$=0) the SO pin is in a high-impedance state.

Serial Clock (SCK)
All commands and data written to the Serial Input (SI) are clocked relative to the rising edge of the Serial Clock (SCK). All data read from the Serial Data Output (SO) is clocked relative to the falling or rising edge of SCK as specified in the non-volatile configuration register. The data output clock edge is factory-programmed to the default condition of the falling edge, allowing compatibility with standard SPI systems. Clock rates of up to 16 MHz are supported.

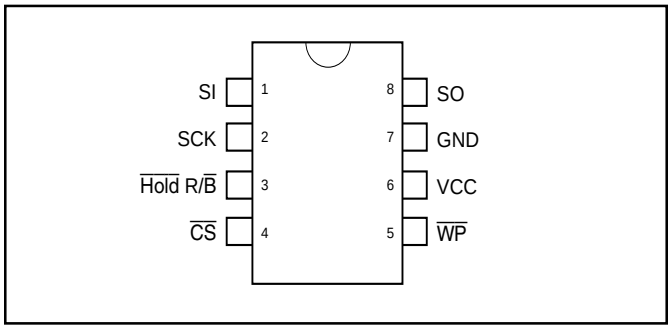


Figure 3A. NX25F011B and NX25F021B Pin Assignments, 8-Pin SOIC

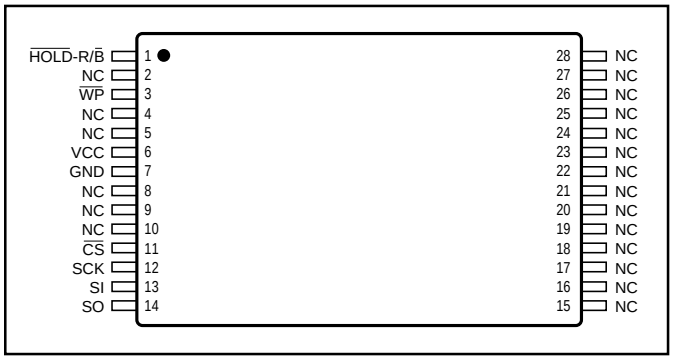


Figure 3B. NX25F011B, NX25F021B, and NX25F041B Pin Assignments, 28-Pin TSOP (Type I)

Chip Select ($\overline{CS}$)
The NX25F011B, NX25F021B, and NX25F041B are selected for operation when the Chip Select input ($\overline{CS}$) is asserted low. SCK must be low when ($\overline{CS}$) is asserted to a low state. Upon power-up, an initial low-to-high transition of $\overline{CS}$ is required before any command sequence will be acknowledged. The device can be deselected to a non-active state when $\overline{CS}$ is brought high. Once deselected, the SO pin will enter a high-impedance state and power consumption will decrease to standby levels unless programming is in process, in which case standby will resume when programming is complete.

Write Protect ($\overline{WP}$)
The Write Protect input ($\overline{WP}$) works in conjunction with the write protect range set in the configuration register bits. When $\overline{WP}$ is asserted (active low) the entire Flash memory array is write protected. When high, any Flash memory sector can be written to unless its address is within the write protect range that is set in the configuration register.

Hold or Ready/Busy ($\overline{HOLD}$ or R/$\overline{B}$)
This multifunction pin can serve either as a Hold input ($\overline{HOLD}$) or as a Ready-Busy output (R/$\overline{B}$). The pin function is user-programmable through the non-volatile configuration register. Factory-programmed as a no-connect, the pin can be reconfigured as a Ready-Busy output or as a Hold input by setting the configuration register. See the configuration register section of this data sheet for further details.

Power Supply Pins (Vcc and GND)
The NX25F011B, NX25F021B, and NX25F041B support single power supply Read and Erase/Write operations in 5V and 3V versions. Typical active power is as low as 5 mA for the 3V version with standby current less than 1 µA.

Table 1. Pin Descriptions

SI	Serial Data Input
SO	Serial Data Output
SCK	Serial Clock Input
$\overline{CS}$	Chip Select Input
$\overline{WP}$	Write Protect Input
$\overline{Hold}$, R/$\overline{B}$	Hold Input or Read Busy Output
Vcc	Power Supply

Serial Flash Memory Array

The NX25F011B, NX25F021B, and NX25F041B Serial Flash memory arrays are organized as 512, 1024, and 2048 sectors of 264-bytes (2,112 bits) each, as shown in Figure 4.

The Serial Flash memory of the NX25F011B, NX25F021B, and NX25F041B is byte-addressable for read operations. This allows a single byte, or specified sequence of bytes, to be read without having to clock an entire 264-byte sector out of the device. Data can be read directly from a sector in the Flash memory array by using a *Read from Sector* command.

Data can be written to the Flash memory array one sector (264-bytes) at a time through the Serial SRAM using a *Write to Sector* command or a *Transfer SRAM to Sector* command. After a sector has been written, the memory array will become busy while it is programming the specified non-volatile memory cells of that sector. This busy time will not exceed t_{WP} during which time the Flash array is unavailable for read or write access. The device can be tested to determine the array's availability using the Ready/Busy status that is available during most read commands, through the status register, or on the Ready/Busy pin. Note that the SRAM is generally available, even when the memory array is busy. See the Serial SRAM section for more details.

The NX25F011B, NX25F021B, and NX25F041B do not require pre-erase. Instead, the device incorporates an auto-erase-before-write feature that automatically erases the addressed sector at the beginning of the write operation.

Separate commands for *Erase Sector, Erase Block (32 sectors)*, and *Write Sector Only* are also available to improve performance for applications that can accommodate pre-erase. An internal auto-verify is performed after every erase and write command. The results of the auto-verify are available in the status register. The status register EE and EW bits must be checked to confirm proper erase or write operation.

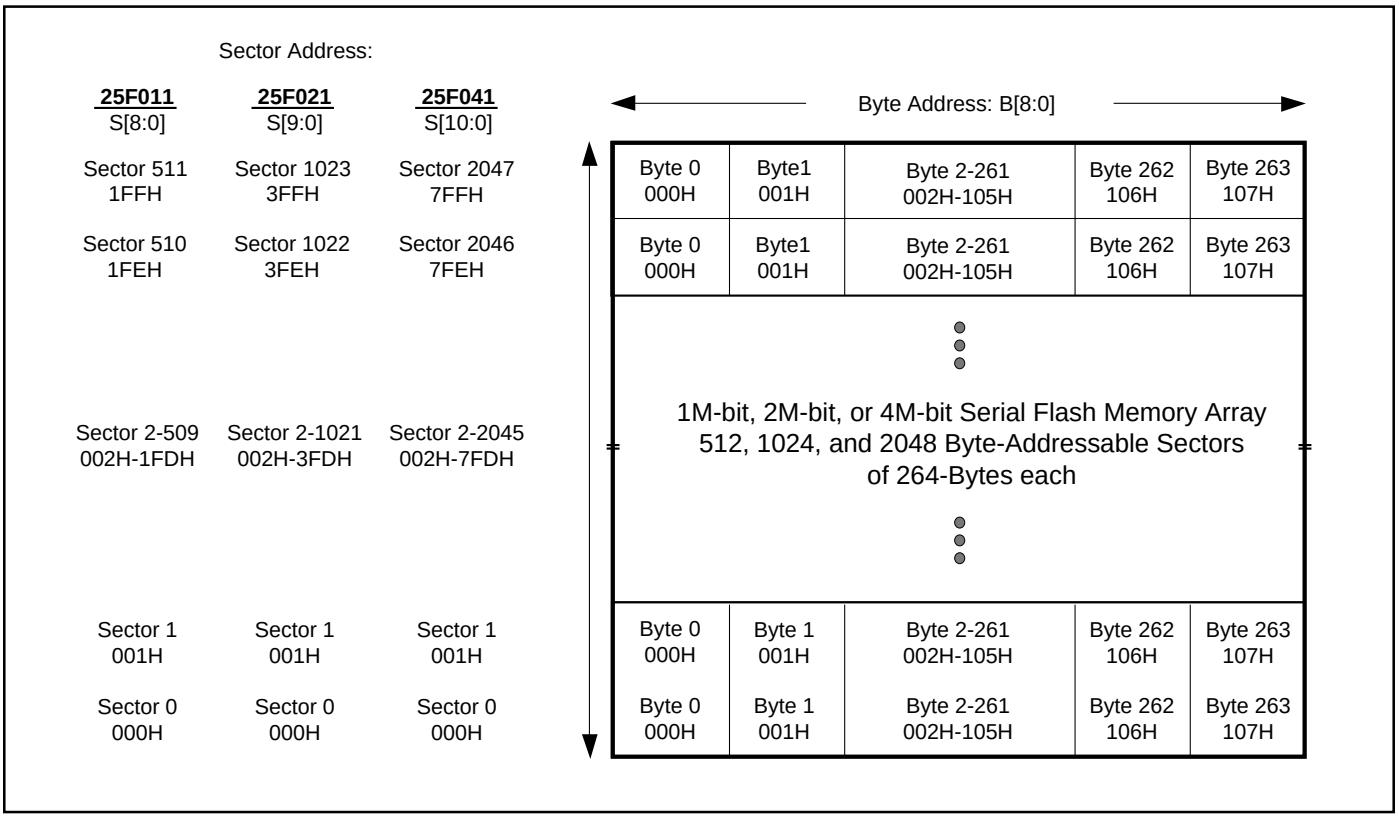


Figure 4. NX25F011B, NX25F021B, and NX25F041B Serial Flash Memory Array

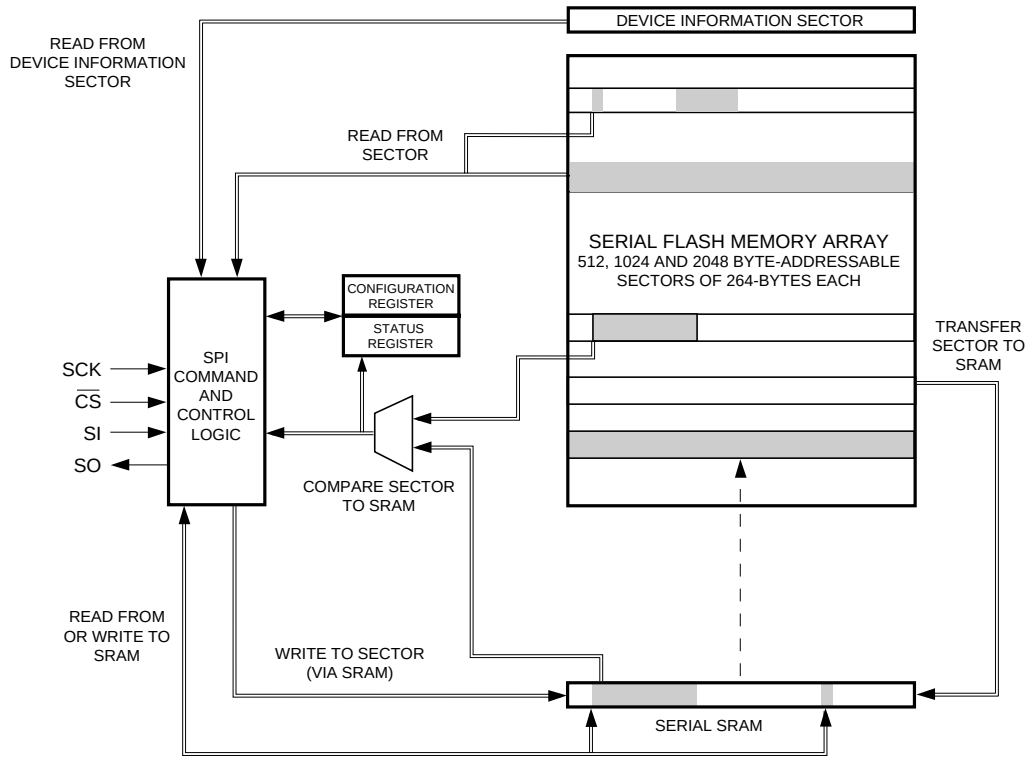
Serial SRAM

One of the most powerful features of the NX25F011B, NX25F021B, and NX25F041B is the integrated Serial SRAM. The main purpose of the Serial SRAM is to serve as the primary buffer for sector data to be written into the Serial Flash memory array. Using the *Write to Sector* command, data is first shifted into the SRAM from the SPI bus. When the command sequence has been completed, the entire 264-bytes is written to the selected sector. See Erase/Write cycle timing (t_{WP}).

The SRAM is fully byte-addressable. Thus, the entire 264-bytes, a single byte, or a sequence of bytes can be read from, or written to the SRAM. This allows the SRAM to be used as a temporary work area for read-modify-write operations prior to a sector write.

The *Transfer Sector to SRAM* command allows the contents of a specified sector of Flash memory to be moved to the SRAM. This can be useful when only a portion of a sector needs to be altered. In this case the sector is first transferred to the SRAM, where modifications are made using the *Write to SRAM* command. Once complete, a *Transfer SRAM to Sector* command is used to update the sector.

The *Compare Sector* command allows the contents of the SRAM to be compared with the specified sector in memory. The result of the compare is set in the status register. This command can be useful when re-writing multi-sector files that have only minor changes from the previous write. If the new data in the SRAM is the same as the previously written data, the sector write can be skipped. Used in this way, the command saves time that would have been used for re-programming. It also extends the endurance of the Flash memory cells.



Note:
1. A single byte, several bytes, or all bytes of a Flash sector, the SRAM, or Program Buffer may be addressed.
2. All double lines represent implied connections or actions.

Figure 5. Command Relationships of the SPI Interface, Serial Flash Memory Array and SRAM

Using the SRAM Independent of Flash Memory
The SRAM can be used independently of Flash memory operations for lookup tables, variable storage, or scratch pad purposes. If the Flash memory needs to be written to while SRAM is being used for a different purpose, the contents can be temporarily stored to a sector and then transferred back again when needed. The SRAM can be especially useful for RAM-limited microcontroller-based systems, eliminating the need for external SRAM and freeing pins for other purposes. It can also make it possible to use small pin-count microcontrollers, since only a few pins are needed for the interface instead of the 20-40 pins required for parallel bus-oriented Flash devices.

Write Endurance
Standard write endurance rating of the memory array allows for 10,000 erase/write cycles per sector or 100,000 erase/write cycles per block. Extended sector endurance to 100,000 cycles is possible using ECC techniques like those provided in the SFK Development Kit. The rating of the non-volatile configuration register EEPROM cells is 1,000 write cycles. This is more than adequate considering the configuration seldom needs to be changed. To minimize writes to the non-volatile configuration register, the configuration register should be read upon power-up to determine if a change is required. If no change is needed, the write non-volatile configuration command can be skipped. This process will extend the life of the non-volatile configuration register and save processing time (Figure 6).

Write Protection

The NX25F011B, NX25F021B, and NX25F041B provide advanced software and hardware write protection features. Software-controlled write protection of the entire array is handled using the *Write Enable and Write Disable* commands. Hardware write protection is possible using the Write Protect pin ($\overline{WP}$). Write-protecting a portion of Flash memory is accommodated by programming a write protect range in the configuration register. For applications needing a portion of the memory to be permanently write-protected or a fixed configuration register value, a onetime programmable write protection feature is supported. Contact *NexFlash* for further information.

Configuration Register

The Configuration Register stores the current configuration of the $\overline{HOLD}$-R/$\overline{B}$ pin, read clock edge, write protect range, and alternate oscillator frequency (Figure 7). The configuration register is accessed using the *Write and Read Configuration Register* commands. The non-volatile configuration register will maintain its setting even when power is removed.

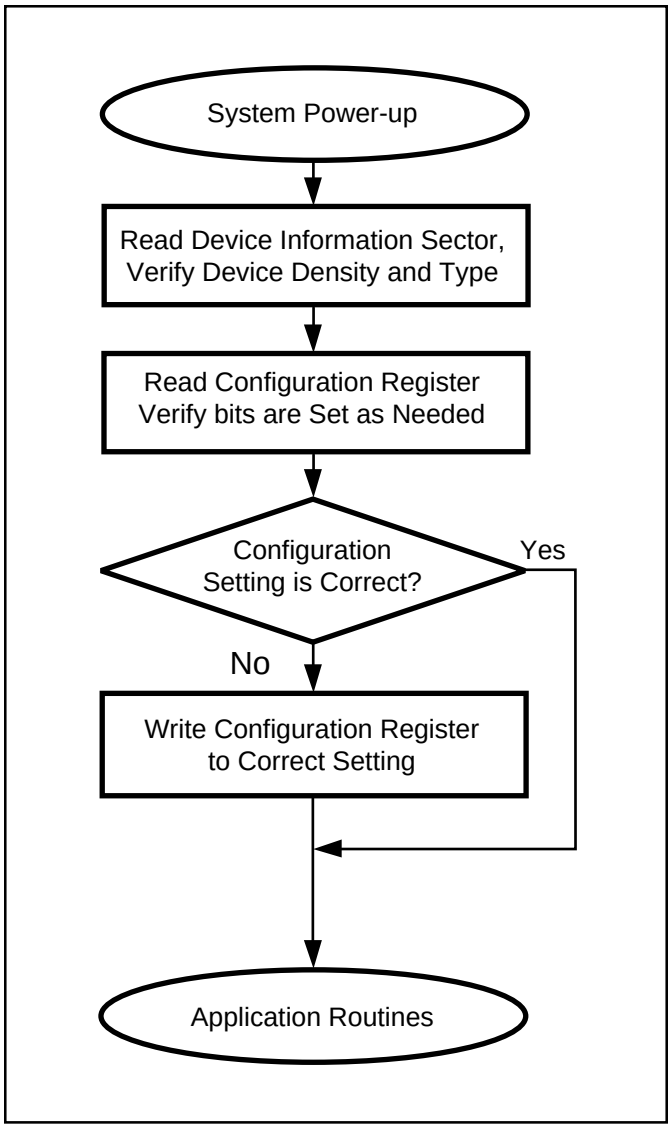


Figure 6. Flow Chart for Checking the Configuration Register upon Power-up

The factory default setting for the non-volatile configuration register is CF8-CF0 is: 0 0000 1001 B (write protect range = none, read uses falling edge of the clock, and pin 1 = no connect). Bits CF15-CF9 are reserved. When writing to the configuration register CF15-CF9 should be 0. When reading, the settings of CF15-CF9 should be ignored.

Alternate Oscillator Frequency, AF

Flash memory devices have charge pump oscillators to generate internal high-voltages used for programming non-volatile memory cells. In some applications, the oscillator frequency of the charge pump may cause noise interference. To solve this problem, an alternate oscillator frequency (AF) can be selected by setting bit CF[8] of the configuration register. The alternate frequency is a non-harmonic frequency of the standard oscillator. The factory default setting is for the standard oscillator frequency, AF equal to 0.

AF=0 Standard Oscillator Frequency is used.
AF=1 Alternate Oscillator Frequency is used.

Write Protect Range and Direction, WR[3:0], WD

The write protect range and direction bits WR[3:0] and WD are located at configuration bits CF[7:4] and CF[3] respectively. The write protect range and direction bits select how the array is protected. They work in conjunction with the $\overline{WP}$ input pin, valid only if $\overline{WP}$ is inactive (high). WR[3:0] can select write protection of all sectors, none of the sectors, or specific sectors grouped in blocks of 32 (~8 KB). The WD bit specifies whether the protected block range starts from the first sector, address 0 (000H), or from the last sector (1FFH for the NX25F011B, 3FFH for the NX25F021B, and 7FF for the NX25F041B). Table 2 lists the write protect sector range for both devices. Once protected, all further writes to sectors within the range will be ignored. The factory default setting is with no write protected sectors, WR=[0,0,0,0] and WD=1.

Read Clock Edge, RCE

The Read Clock Edge bit (RCE) is located at configuration bit location CF[2]. It selects which edge of the clock (SCK) is used while reading data out of the device. Although the SPI protocol specifies that data is written during the rising edge and read on the falling edge of the clock, if required, the output can be driven on the rising edge of the clock by setting the configuration registers RCE bit to a 1. Using the rising edge of clock for data reads may be beneficial to the timing of some high-speed systems. The factory default setting is the falling edge of SCK.

RCE=0 Read data is output on the falling edge of SCK.
RCE=1 Read data is output on the rising edge of SCK.

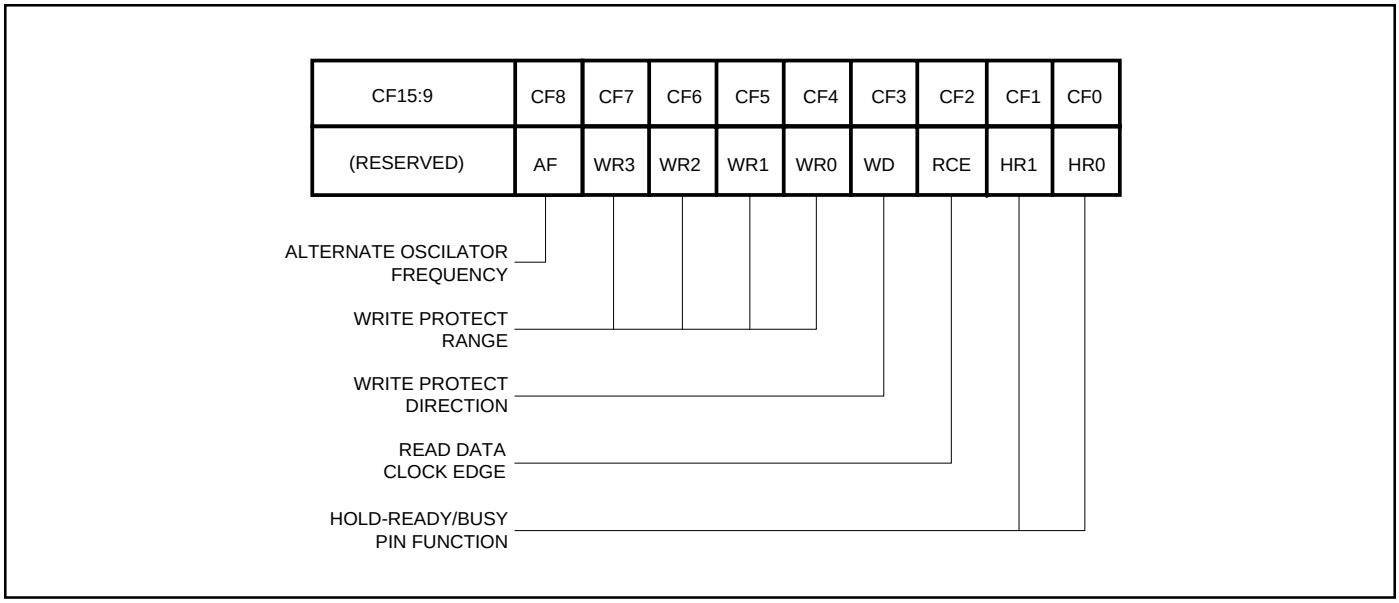


Figure 7. Configuration Register Bit Locations

Table 2. Write Protect Range Sector Selection (Hex)

Write Protect Range Config. Bits				Write Protected Sectors	
WR3	WR2	WR1	WR0	WD=0	WD=1
0	0	0	0	None	None
0	0	0	1	000-01FH	xE0-1FF/3FF/7FFH
0	0	1	0	000-03FH	xC0-1FF/3FF/7FFH
0	0	1	1	000-05FH	xA0-1FF/3FF/7FFH
0	1	0	0	000-07FH	x80-1FF/3FF/7FFH
0	1	0	1	000-09FH	x60-1FF/3FF/7FFH
0	1	1	0	000-0BFH	x40-1FF/3FF/7FFH
0	1	1	1	000-0DFH	x20-1FF/3FF/7FFH
1	0	0	0	000-0FFH	x00-1FF/3FF/7FFH
1	0	0	1	000-11FH	yE0-1FF/3FF/7FFH
1	0	1	0	000-13FH	yC0-1FF/3FF/7FFH
1	0	1	1	000-15FH	yA0-1FF/3FF/7FFH
1	1	0	0	000-17FH	y80-1FF/3FF/7FFH
1	1	0	1	000-19FH	y60-1FF/3FF/7FFH
1	1	1	0	000-1BFH	y40-1FF/3FF/7FFH
1	1	1	1	ALL	ALL

Note:

1. NX25F041B x=7 Y=6, NX25F021B x=3 y=2, and NX25F011B x=1 y=0

$\overline{\text{HOLD}}$-R/$\overline{\text{B}}$, HR[1:0]

The Hold-Ready/Busy ($\overline{\text{HOLD}}$-R/$\overline{\text{B}}$) bits HR1 and HR0 are located at bits CF[1:0] of the configuration register. These two bits select one of four possible functions: No Connect, $\overline{\text{HOLD}}$ input, R/$\overline{\text{B}}$ Output, or R/$\overline{\text{B}}$ Output with open drain. The factory setting for the pin is "No Connect".

HR1	HR0	Pin Configuration
0	0	$\overline{\text{HOLD}}$ input
0	1	No Connect
1	0	R/$\overline{\text{B}}$ Output (Open Drain)
1	1	R/$\overline{\text{B}}$ Output

Configured as a R/$\overline{\text{B}}$ output, the pin can serve as a system interrupt. When R/$\overline{\text{B}}$ is high, the array is ready to be programmed. When R/$\overline{\text{B}}$ is low, it is busy programming. If configured with an open-drain, an external pull-up resistor should be used.

As a $\overline{\text{HOLD}}$ input, the pin can be used in conjunction with the $\overline{\text{CS}}$ and SCK pin to suspend a serial command sequence without resetting the command. This can be useful if a command is in process and a higher priority task on the same SPI bus needs to be attended to. To suspend a command, $\overline{\text{HOLD}}$ must be brought low while $\overline{\text{CS}}$ and SCK are low. With $\overline{\text{HOLD}}$ low, further data on the SI pin is ignored (even while SCK is clocked) and the SO pin goes to a high-impedance state. To resume the command sequence, $\overline{\text{HOLD}}$ must be brought high when $\overline{\text{CS}}$ and SCK are low. See timing diagrams.

Status Register Bit Descriptions

The status register provides status of the Flash array's Ready/Busy condition (R/$\overline{\text{B}}$), transfers between the SRAM and program buffer (TX), Write-Enable/Disable (WE), and Compare Not Equal (CNE). The register can be read using the Read Status Register command (Figure 8).

Ready/Busy Status, BUSY

The BUSY status bit is located at bit ST[7] of the status register. Testing the BUSY bit is one of several ways to check Ready/Busy status of the array. At power-up the BUSY bit is reset to 0.

BUSY=1 The memory array is busy programming.
BUSY=0 The memory array is ready for further use.

SRAM Transfer All or Compare All, TR

The TR status bit is located at bit ST[6] of the status register. The bit provides status primarily for use during the *Transfer All Sector to SRAM* command and *Compare All Sector to SRAM* command. An active state 1 indicates a transfer is in process and the SRAM Array is not available for use. The device will indicate a BUSY state while the TR bit is active. Upon power up the TR bit resets to 0.

TR=1 Transfer or Compare All in Process.
TR=0 Transfer or Compare All not in Process.

Write Enable/Disable, WE

The WE status bit is located at bit ST[4] of the status register. The bit provides write protect status of global *Write Enable and Write Disable* commands. Upon power- up the WE bit resets to 0.

WE=1 Write Enabled, array can be written to.
WE=0 Write Disabled, array can not be written to.

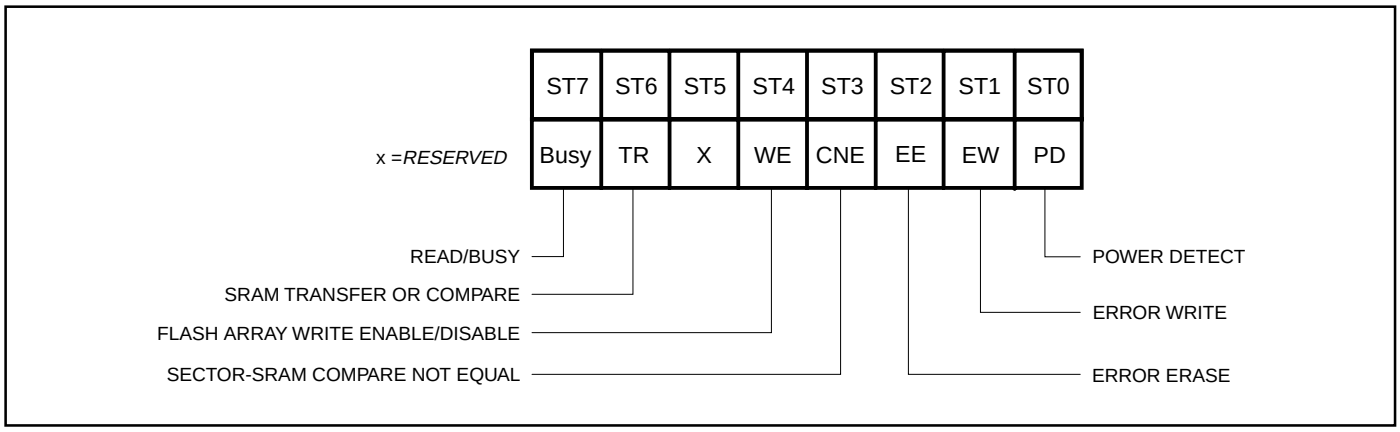


Figure 8. Status Register Bit Locations

Compare Not Equal, CNE
The CNE status bit is located at bit ST[3] of the status register. The bit provides a cumulative comparison result during a *Compare Sector with SRAM* command. The CNE bit is reset to a 0 upon power-up or after a Clear Compare Bit command is executed.

CNE=1 Sector and SRAM contents are not equal.
CNE=0 Sector and SRAM are equal or CNE bit reset.

Error Erase, EE
The Error Erase bit provides status of the last erase operation for the Write Sector through SRAM, Transfer SRAM to Sector, Erase Sector and Erase Block commands. If the Erase operation operates correctly the EE bit will be reset to a 0. If an erase error occurs, the EE bit will be set to a 1 and the related command should reissued. If the error bit continues to get set the application firmware should process an error routine and not attempt to use the selected sector any further.

EE=0 Last erase operation was successful
EE=1 Last erase operation was not successful

Error Write, EW
The Error Write bit provides status of the last write operation for the Write Sector through SRAM, Transfer SRAM to Sector, Write Sector Only commands. If the Write operation operates correctly the EW bit will be reset to a 0. If a write error occurs, the EW bit will be set to a 1 and the related command should reissued. If the error bit continues to get set the application firmware should process an error routine and not attempt to use the selected sector any further.

EW=0 Last write operation was successful
EW=1 Last write operation was not successful

Power Detect, PD
The Power Detect bit works in conjunction with the Set Power Detection and Reset Power Detection Commands and is primarily used for removable media applications. The Set Power Detect Command must be issued before the PD bit can be used for power detection.

PD=0 Power has been removed
PD=1 Power has not been removed

Command Set

The NX25F011B, NX25F021B, and NX25F041B have a powerful command set that is fully controlled through the SPI bus. Command relations are shown in Figure 5 and a list of commands and their associated address, status, clock, and data bytes are shown in Table 3. Detailed clock timing of the *Read Sector* and *Write Sector* command sequences are shown in Figures 10 and 11.

After power up, a device enters an idle state that will maintain until $\overline{CS}$ pin is asserted low. All commands are entered from the SPI serial data input (SI) pin on the rising edge of SCK while $\overline{CS}$ is asserted low. All command, address, and configuration bits are shifted into the device with most-significant-bit-first. Data bits read from the device are shifted out with least significant byte first (i.e., byte-00H, byte-01H,...). The bit order within each byte is most-significant-bit first (i.e.,D7,...D0). All commands are completed by asserting the $\overline{CS}$ pin high.

Note that the entire 264-byte contents of a Flash sector or the SRAM does not have to be accessed all at once. Read, Write, Transfer Clocked, and Compare Clocked commands allow for byte addressing. Thus a single byte, or clocked sequence of bytes, can be accessed at any starting location within the 264-byte boundary as specified by the byte-address field.

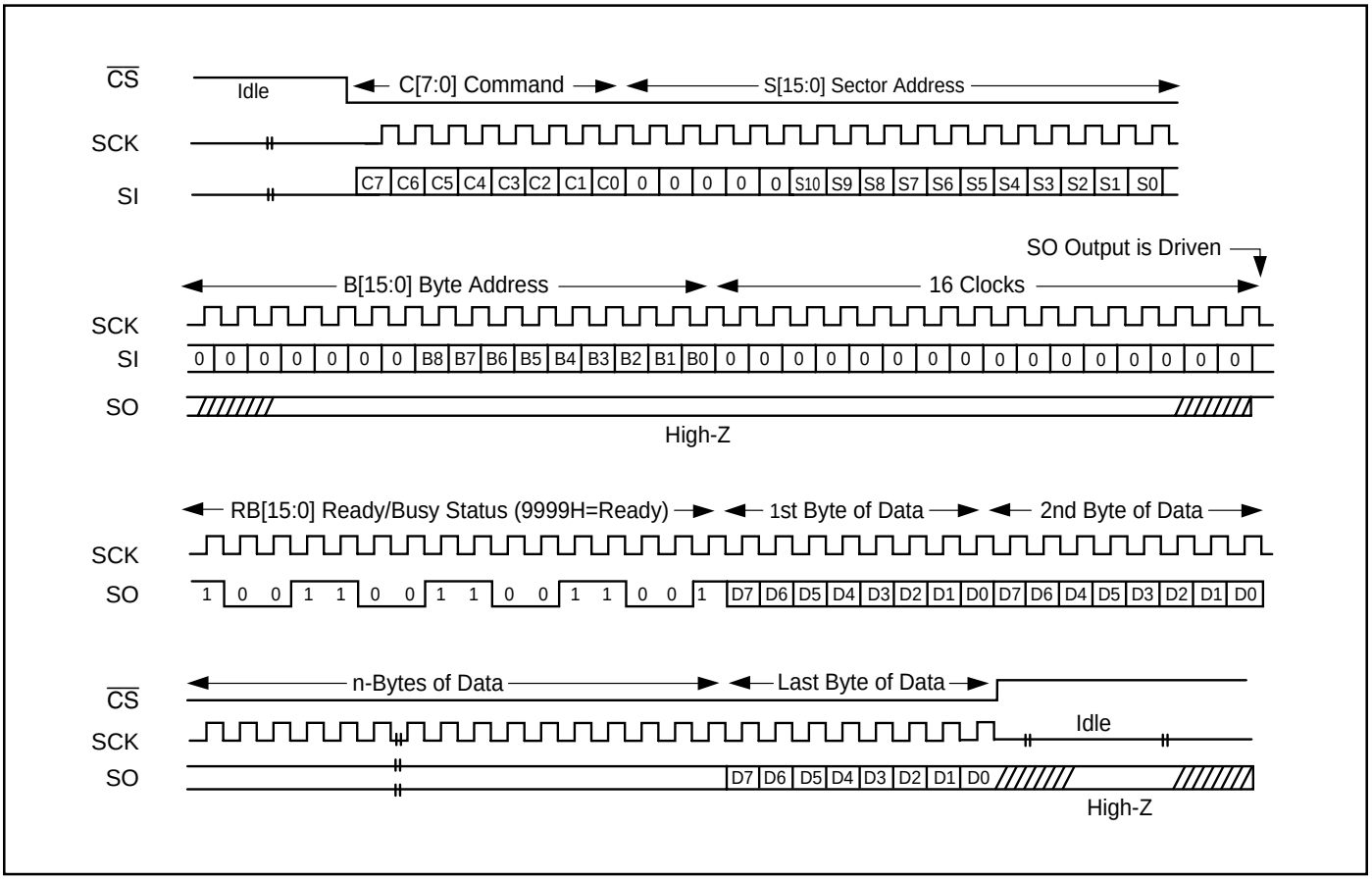


Figure 10. Read from Sector Command Sequence

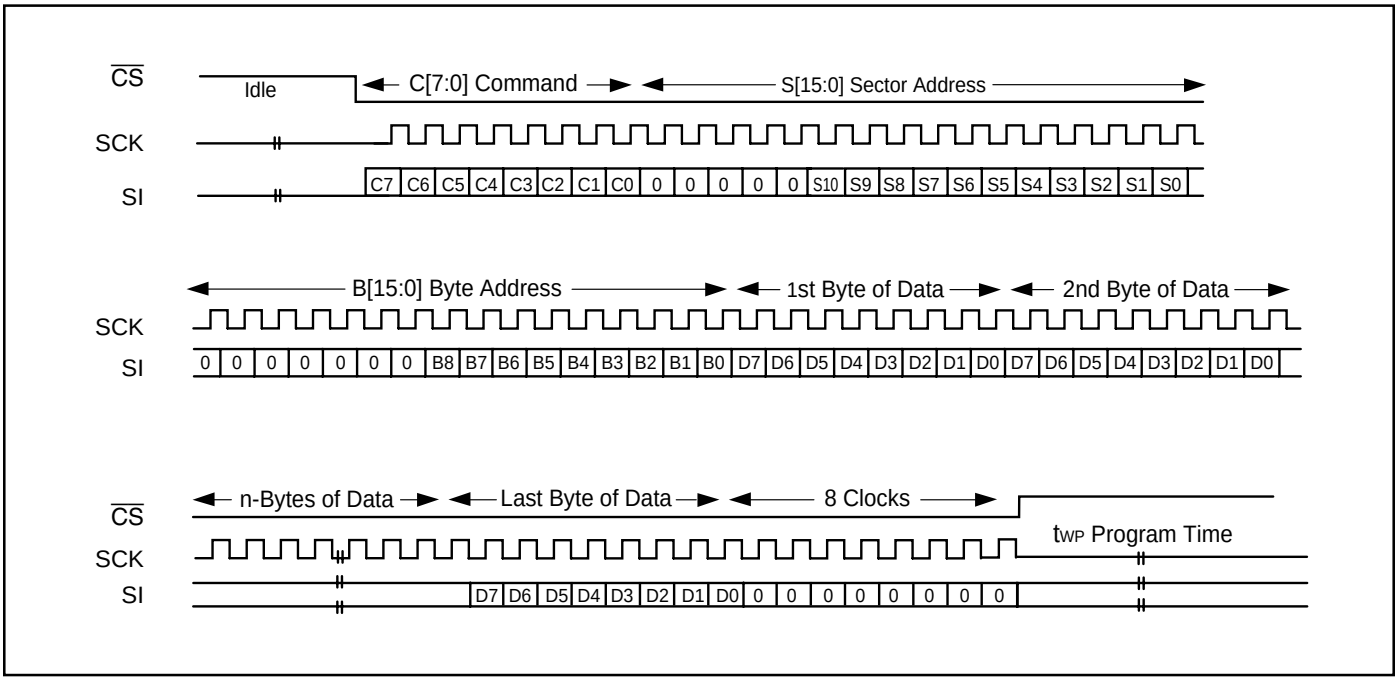


Figure 11. Write to Sector Command Sequence

Command Set for the NX25F011B, NX25F021B and NX25F041B Serial Flash Memory

Command Name	Byte 0	Byte 1-2	Byte 3-4	n- bytes *(Italics indicate device output)*		
Sector Commands						
Read From Sector	52H	Sector address	Byte address	0000H	*Ready/Busy*	*Read Data*
Read From Sector w/AutoInc [3]	50H	Sector address	0000H	0000H	*Ready/Busy*	*Read Data*
Read From Sector Low Freq.	51H	Sector address	Byte address	0000H	*Ready/Busy*	*Read Data*
Read From Sector w/AutoInc Low Freq [3]	5BH	Sector address	0000H	0000H	*Ready/Busy*	*Read Data*
Write Enable [1]	06H	00H				
Write Disable [1]	04H	00H				
Write to Sector (through SRAM) [2]	F3H	Sector address	Byte address	Write Data	00H	
Serial SRAM Commands						
Write to SRAM [2, 3]	72H	Byte address	Write data	00H		
Read from SRAM [1,3]	71H	Byte address	00H	*Read Data*		
Transfer all of SRAM to Sector	F3H	Sector address	0000H			
Transfer all of Sector to SRAM [3]	53H	Sector address	0000H	0000H		
Compare Sector to SRAM [3]	8DH	Sector address	Byte address	0000H		
Configuration and Status Commands						
Read Configuration [1, 3]	8CH	*Configuration*				
Write Non-Volatile Configuration [1] Register	8AH	Configuration	0000H			
Read Status Register [1, 3]	84H	*Status (8 bits)*				
Clear Compare Status [1]	89H					
Set Power Detection Bit [1, 3]	03H					
Reset Power Detection Bit [1, 3]	09H					
Read Device Information Sector	15H	0000H	Byte address	0000H	*Ready/Busy*	*DIS Data*
Special Sector Commands [3, 4]						
Erase Sector	F1H	Sector address	0000H			
Erase Block	F4H	Block address	0000H			
Write-Only to Sector through SRAM	F2H	Sector address	Byte address	Write Data	00H	
Compatibility Commands for 25xxxA Series Devices						
Read from SRAM	81H	0000H	Byte address	0000H	*Read/Busy*	*Read Data*
Write to SRAM	82H	0000H	Byte address	Write data	00H	
Read Configuration Register	8BH	0000H	0000H	0000H	*Ready/Busy*	*Configuration*
Read Status Register	83H	0000H	0000H	0000H	*Ready/Busy*	*Status*
Transfer Sector to SRAM Clocked	54H	Sector address	Byte address	N*00H	00H	
Compare Sector to SRAM Clocked	86H	Sector address	Byte address	0000H	*Ready/Busy*	*Bit compare of data*

Notes:
1. Command may be used when device is busy
2. Command may not be used when device is busy and TR bit=0
3. New “B” series command
4. Warning: Read description of these commands before using to ensure reliable operation.

SERIAL FLASH SECTOR COMMANDS

Read From Sector (52H)

Reading from a sector is accomplished by first bringing $\overline{CS}$ low then shifting in the *Read from Sector* command (52H) followed by its 16-bit "sector-address" field. Although the sector-address field is 16-bits, only bits S[8:0] for the NX25F011B (0-1FFH), S[9:0] for the NX25F021B (0-3FFH), S[10:0] for the NX25F041B (0-7FFH) are used. The uppermost sector address bits are not used but must be clocked using 0 for data. Next a 16-bit "byte-address" field is clocked into the device to designate the starting location within the 264-byte sector. Only B[8:0] of the byte-address field are used; the uppermost bits are not used but must be clocked in (use 0 for data). Only byte-addresses of 0 to 107H (264 bytes) are valid. Following the byte-address field, 16 control clocks are required with data=0.

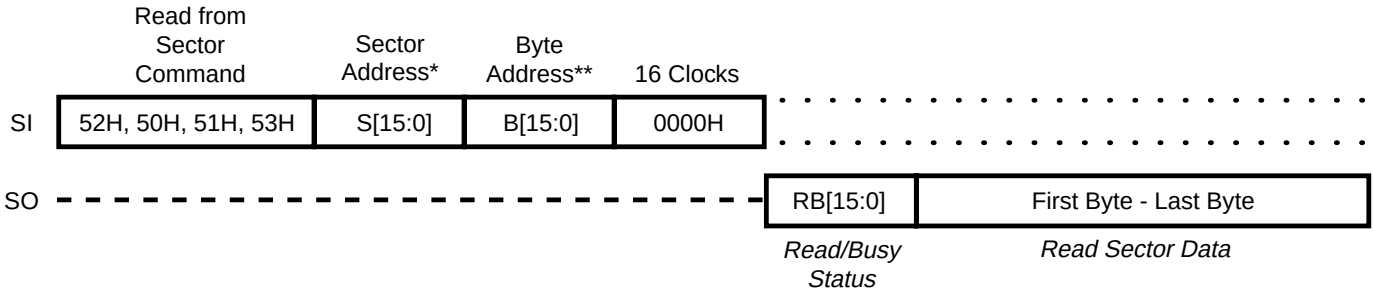
The Serial Data Output (SO) will change from a high-impedance state and begin to drive the output with Ready/Busy status RB[15:0]. If SO uses the rising edge of clock (configuration register RCE=1), the output will be driven after the last control clock. If SO uses the falling edge of clock (RCE=0), the output will be driven on the next falling edge of clock. If the array is not busy, the output status will be 9999H, followed by the sector data on the SO pin. If the array is busy, the status will be 6666H, and the command should be terminated and restarted after a ready state occurs. The data field is shifted out with the least significant byte first (i.e., byte-00H, byte-01H, ...). The bit order within each byte is the most significant bit first (i.e.,D7,...D0). The byte-address is internally incremented to the next higher byte address as the clock continues. When the highest byte-address (107H) is reached, the address counter rolls over to byte-0H and continues to increment. Asserting the $\overline{CS}$ pin high completes (or terminates) the command. Detailed timing for the *Read from Sector* command is shown in Figure 10.

Read From Sector with Auto Increment (50H)

The *Read from sector with Auto Increment* command operates similar to the standard Read from Sector command except that after the last bit of the current sector is clocked the next sequentially addressed sector will be automatically selected for reading without requiring the nine byte command sequence to be issued. This allows the entire device or a large number of sectors to be read out with a single command. **A standard read (52H) command must be issued to properly set the starting sector address prior to the *Read Sector with Auto-increment* command. Contact NexFlash Applications Dept for further information.**

Read From Sector Low Frequency (51H) and Read From Sector Low Frequency with Auto Increment (5BH)

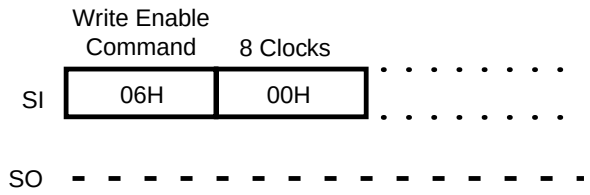
The *Read From Sector at Low Frequency* command (51H) and *Read From Sector Low Frequency with Auto Increment* command (5BH) can reduce power consumption during read operations by 25%-40% when the system clock frequency is 1 MHz or lower. The command sequences are identical to the standard commands.



*The sector address only uses bits [8:0], [9:0] or [10:0] Depending on the density
**The byte address only uses bits [8:0]. Byte address must be 0000h for Auto Increment commands

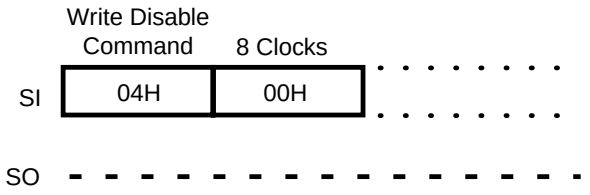
Write Enable (06H)

Upon power-up, the Flash memory array is write- protected until the *Write Enable* command (06H) has been issued. The $\overline{WP}$ pin must be inactive while writing the command for the write enable to be accepted. The status of the device's write protect state can be read in the status register. The *Write Enable* command sequence is completed by asserting $\overline{CS}$ high after eight additional clocks.



Write Disable (04H)

The *Write Disable* command (04H) protects the Flash memory array from being programmed. Once issued, further *Write to Sector* or *Transfer SRAM to Sector* commands will be ignored. The status of the write protect state can be read in the status register. The *Write Disable* command sequence is completed by asserting $\overline{CS}$ high after eight additional clocks.



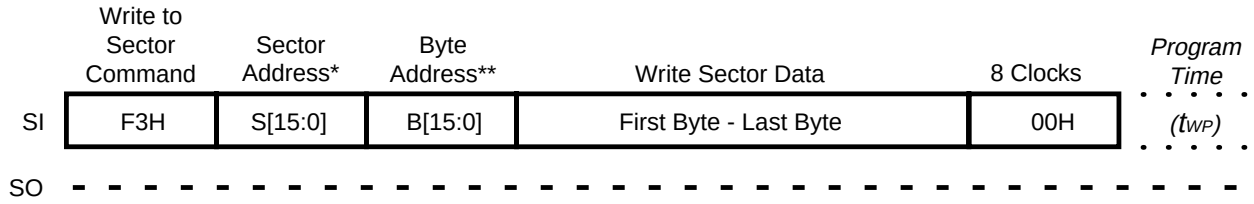
Write to Sector Through SRAM (F3H)

Before writing to a sector in the Flash memory array, all hardware and software write protection must be in an enabled state. This means that the $\overline{WP}$ pin must be in a high state, a *Write Enable* command must have previously been issued, and the sector location that is to be written to must be outside the write protect range set in the configuration register. Additionally, the Ready/Busy status should be checked to confirm that the memory array is available to be written to.

Writing to a sector is accomplished by first bringing $\overline{CS}$ low and shifting in the *Write to Sector* command (F3H) followed by a 16-bit "sector-address" field. Although the sector-address field is 16-bits, only bits S[8:0] for the NX25F011B (0-1FFH), S[9:0] for the NX25F021B (0-3FFH), or S[10:0] for the NX25F041B (0-7FFH) are used. The uppermost sector address bits are not used but must be clocked in (use 0 data). Following the sector address, a 16-bit "byte-address" field is clocked into the device to designate the starting location within the 264-byte sector. Only bits B[8:0] of the byte-address field are used and only values of 0-107H (264 bytes) are valid.

After the byte-address has been loaded, data is shifted into the 264-byte SRAM, which serves as a temporary storage buffer. Existing data in the SRAM will be written over. The byte order of the data shifted into the SRAM is least significant byte first (i.e., byte-00H, byte-01H,...). The bit order within each byte is most significant bit first (i.e., D7,...D0). The byte-address is automatically incremented to the next higher byte address as the clock continues. When the last byte address to be written is reached, the command can be completed with an additional eight control clocks (with data=0) followed by asserting $\overline{CS}$ high. If the clock continues to increment past the highest byte-address (107H), the address counter will roll over to byte 0H.

After the $\overline{CS}$ pin is brought high, the data in the SRAM is transferred to the specified sector in memory array. See t_{WP} timing specifications. During this time the array and SRAM will be "busy" and will ignore further array-related commands until complete. All Ready/Busy status indicators will indicate a busy status. Detailed clock timing for the *Write to Sector* command is shown in Figure 11. The EE and EW bits in the status register must be checked after the write is complete ("ready" state) to confirm proper operation.

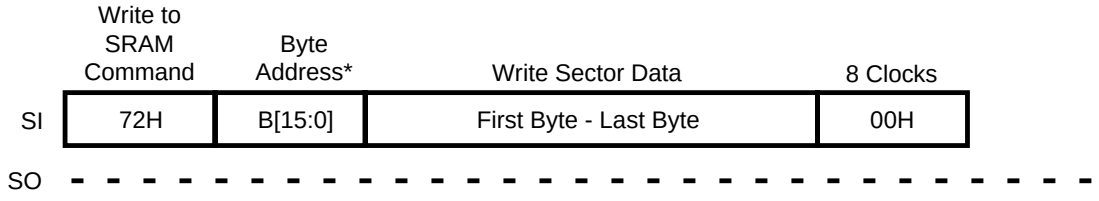


*The sector address only uses bits [8:0], [9:0] or [10:0]
**The byte address only uses bits [8:0]

SERIAL SRAM COMMANDS

Write to SRAM Command (72H)

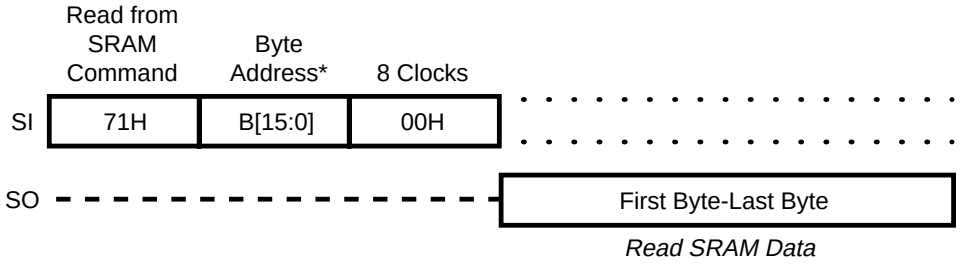
The *Write to SRAM* command (72H) provides access to the 264-Byte SRAM independently of any Flash memory array operation. When $\overline{CS}$ is asserted high to complete the command, the contents of the SRAM will be maintained until overwritten through another command or the power is removed. Using the *Write to SRAM* command, data can be loaded in preparation of writing to a sector in memory and then transferred to a selected sector using the *Transfer SRAM to Sector* command. The TR bit in the status register should be checked first if *Transfer Sector to SRAM* or *Compare Sector to SRAM* commands are used.



*The byte address only uses bits [8:0]

Read from SRAM (71H)

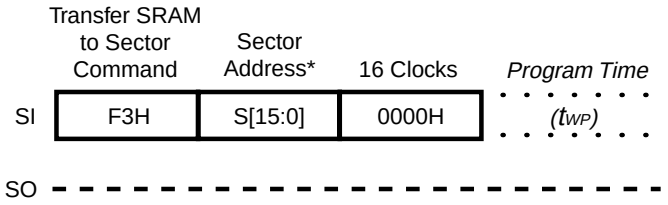
The *Read from SRAM* command (71H) provides access to the 264-Byte SRAM independent of any Flash memory array operations. The TR bit in the status register should be checked first if *Transfer Sector to SRAM* or *Compare Sector to SRAM* commands are used.



*The byte address only uses bits [8:0]

Transfer All of SRAM to Sector (F3H)

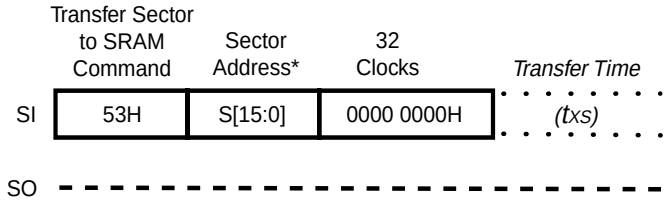
The *Transfer SRAM to Sector* command (F3H) will write the existing contents of the SRAM to the specified sector in memory. The command sequence is identical to that of the *Write to Sector* command except that immediately after the sector address field S[15:0] and 16 control clocks, the $\overline{CS}$ pin is asserted high. This automatically transfers the 264-bytes of SRAM data to the specified sector in the memory array. During this time, the array will be busy. Since the entire 264-bytes are transferred, the byte-address field B[15:0] is not used.



*The sector address only uses bits [8:0], [9:0] or [10:0] Depending on device density

Transfer All of Sector to SRAM (53H)

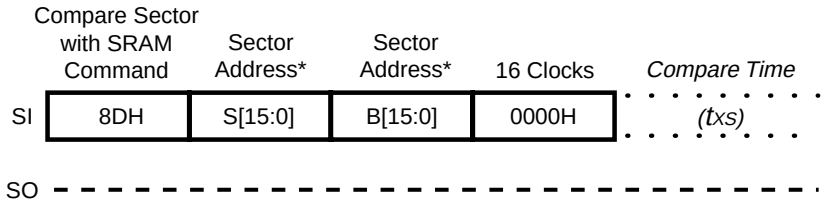
The *Transfer Sector to SRAM* command (53H) allows the contents of a sector to be transferred directly to the SRAM without having to clock or read the sector out of the device and rewrite it into the SRAM. During the transfer, the SO output is in a high-impedance state and the TR bit in the status register will be set to a "1" state. When the last byte address is transferred the TR bit in the status register will be cleared. Note that *the Transfer Sector to SRAM Clocked* command (54H) can also be used if partial transfers are required.



*The sector address only uses bits [8:0], [9:0] or [10:0] Depending on device density

Compare Sector to SRAM (8DH)

The *Compare Sector to SRAM* command (8DH) does a bit-by-bit comparison of the data stored in the addressed sector against data in the SRAM. The TR bit will be 1 during the transfer compare operation. If any of the compared bits are not equal, then the *Compare Not Equal* (CNE) bit in the Status Register is set to a 1. This bit will stay set until a *Clear Compare Status* command has been issued. Note that the *Compare Sector to SRAM Clocked* command can be used if partial compares are required.

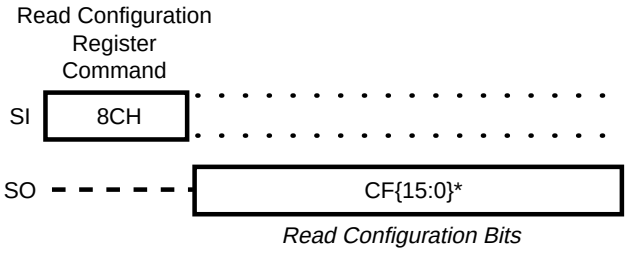


*The sector address only uses bits [8:0], [9:0] or [10:0]
Depending on device density

CONFIGURATION AND STATUS COMMANDS

Read Configuration Register (8CH)

The *Read Configuration Register* command provides access to the configuration register, which stores the current configuration of the $\overline{HOLD}$-R/$\overline{B}$ pin, read clock edge, write protect range, and alternate oscillator frequency (Figure 7). A 16-bit Configuration Data field CF[15:0] provides the contents of the Configuration Register. Although the field is 16-bits long, only bits CF[8:0] are used. All other upper bits are reserved for future features.

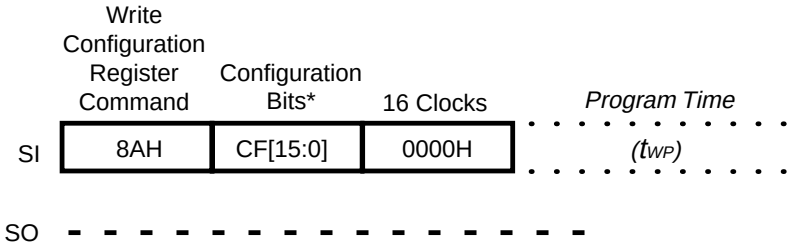


*The CF Register only uses bits [8:0]

Write Non-Volatile Configuration Register (8AH)

The *Write Configuration Register* command provides access to the configuration register which stores the current configuration of the $\overline{HOLD}$-R/$\overline{B}$ pin, read-data clock edge, write protect range, and alternate oscillator frequency. The configuration register is non-volatile. Once set using the *Write Configuration Register* command, the contents will maintain even when power is removed. Because the register's state is stored in non-volatile memory, there is a finite endurance limit to the number of times it can be written to. To limit the number of writes, it is recommended that before writing to the configuration register it should first be read from using the *Read Configuration Register* command. If no change is required, the *Write Configuration Register* command can be skipped. This process will help extend the endurance of the configuration register bits and eliminate additional programming "busy" time.

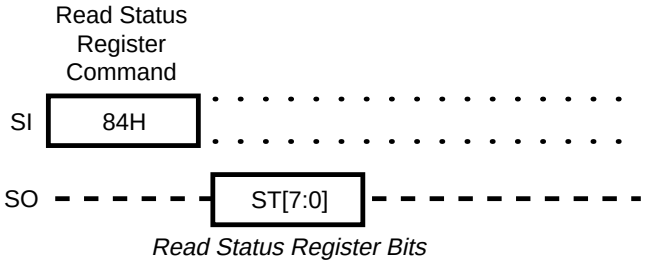
The *Write Configuration Register* command sequence starts with the command byte (8AH) followed by a 16-bit field that specifies configuration register bit settings. Although the field is 16-bits long, only bits CF[8:0] are used. All other upper bits are reserved and must be clocked using 0 for data. After an additional 16 control clocks using 0 for data, the command can be completed by asserting $\overline{CS}$ high. The device will become busy for a short time (t_{WP}) while the non-volatile memory cells of the configuration register are programmed.



*The CF Register only uses bits [8:0]

Read Status Register (84H)

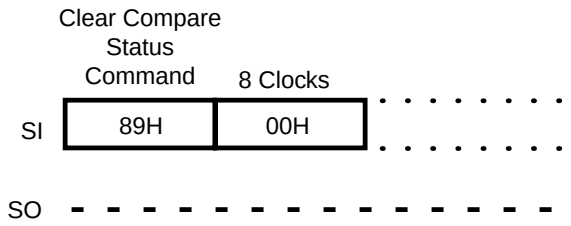
The *Read Status Register* command provides access to the status register and its status flags for Ready/Busy (R/$\overline{B}$), SRAM and program buffer transfer operations (TX), Write Enable/Disable ($\overline{WE}$), and Compare Not Equal (CNE) (Figure 8). An 8-bit Status field ST[7:0] provides the contents of the Status Register.



Read Status Register Bits

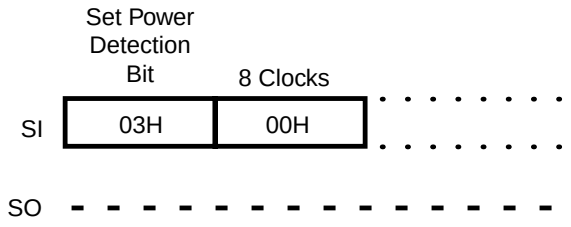
Clear Compare Status (89H)

The *Clear Compare Status* command (89H) works in conjunction with the *Compare Sector to SRAM* command and the Status Register. If any of the compared bits are not equal, then the Compare Not Equal (CNE) bit in the Status Register is set to a 1. The *Clear Compare Status* command must be executed to reset the CNE bit to a 0.



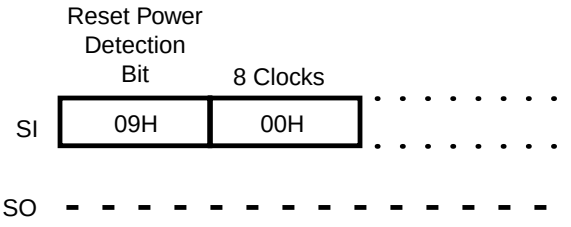
Set Power Detection Bit (03H)

The *Set Power Detection Bit* command (03H) can be used to detect if power has been removed from the device. The command works in conjunction with the Power Detect (PD) status bit. Upon power up the PD bit is cleared to 0. The PD bit can be set to a 1 using the *Set Power Detection Bit* command. Once set, if a power down condition occurs (Vcc voltage < 2V) the PD bit will reset to 0. This function is especially useful for applications using *NexFlash* Serial Flash Modules or other removable media.



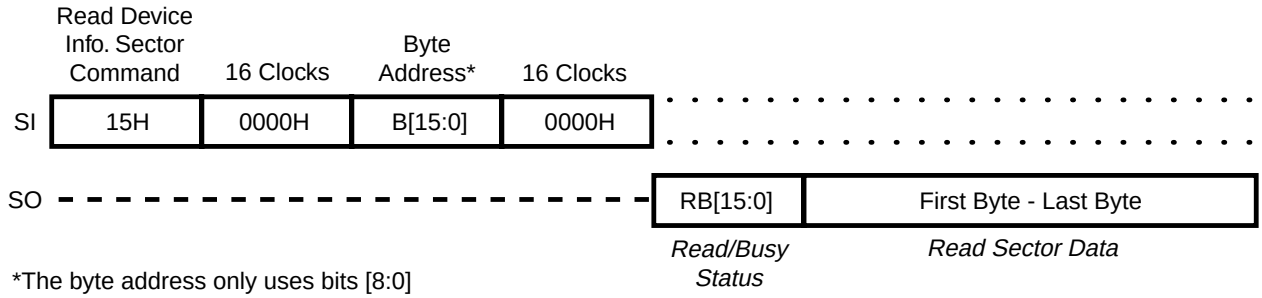
Reset Power Detection Bit (09H)

The *Reset Power Detection Bit* command (09H) can be used to force the Power Detect Status bit in the status register to a 0 state. (see Set Power Detection Bit command (03H).



Read Device Information Sector (15H)

The *Read Device Information* command provides access to a read-only sector that can be used to electronically identify the *NexFlash* Serial Flash device being interfaced to. Information available includes: part number, density, voltage, temperature range, package type, and any special options. This can be extremely useful for systems that need to accommodate optional densities (e.g., both 1M-bit or 2M-bit). In this case the firmware can interrogate the Device Information Sector and determine the density. The Device Information Sector also includes a list of any restricted sectors that might exist in the device. Contact *NexFlash* for more detailed information on the Device Information Sector format.

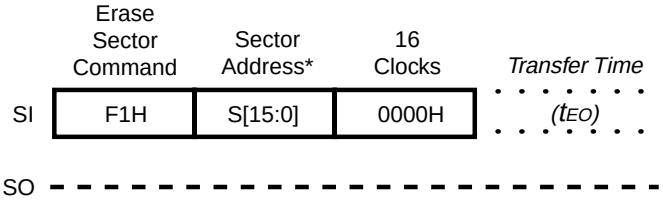


*The byte address only uses bits [8:0]

SPECIAL SECTOR COMMANDS

Erase Sector (F1H)

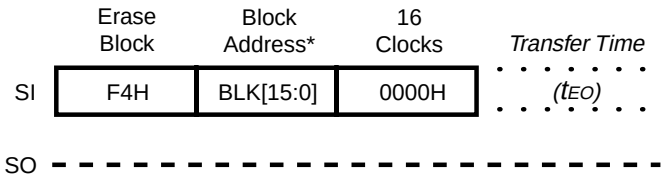
The *Erase Sector* command (F1H) will erase a sector to an “all 1s” state, during this time the array will be "busy." This command can be used in conjunction with the *Write only to Sector through SRAM* command (F2H) to achieve faster program performance in applications that can accommodate pre-erase. (see T_{EO} in AC Characteristics for erase timing). The EE bit in the status register must be checked after the erase is complete ("ready" state) to confirm proper operation.



*The sector address only uses bits [8:0], [9:0] or [10:0] Depending on device density

Erase Block (F4H)

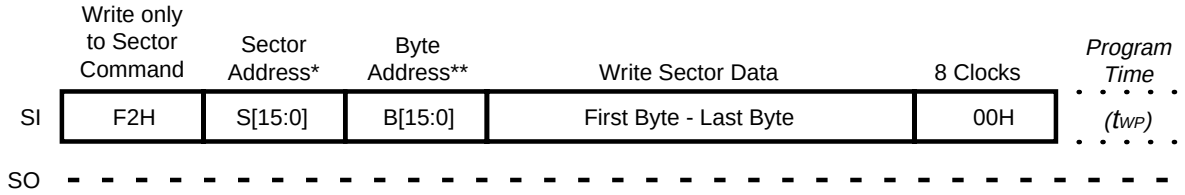
The *Erase Block* command (F4H) will erase a block of 32 sectors to an “all 1s” state, during this time the array will be "busy." This command can be used in conjunction with the *Write only to Sector through SRAM* command (F2H) to achieve faster program performance in applications that can accommodate pre-erase. (see TEO in AC Characteristics for erase and write timing). The EE bit in the status register must be checked after the erase is complete ("ready" state) to confirm proper operation.



*The Block address only uses bits [8:5], [9:5] or [10:5] Depending on device density. Lowest four bit [4:0] must be 0h

Write-only to Sector (F2H)

The *Write-Only to Sector through SRAM* command (F2H) will write a pre-erased sector in about half the time of the standard *Write to Sector through SRAM* command (F3H), during this time the array will be "busy." This command can be used in conjunction with the *Erase Sector* command (F1H) or *Erase Block* command (F4H) to achieve faster program performance in applications that can accommodate pre-erase. (see TWO inAC Characteristics for erase and write timing). The EW bit in the status register must be checked after the erase is complete ("ready" state) to confirm proper operation. **Warning:** to ensure data integrity this command should only be issued after an erase command.

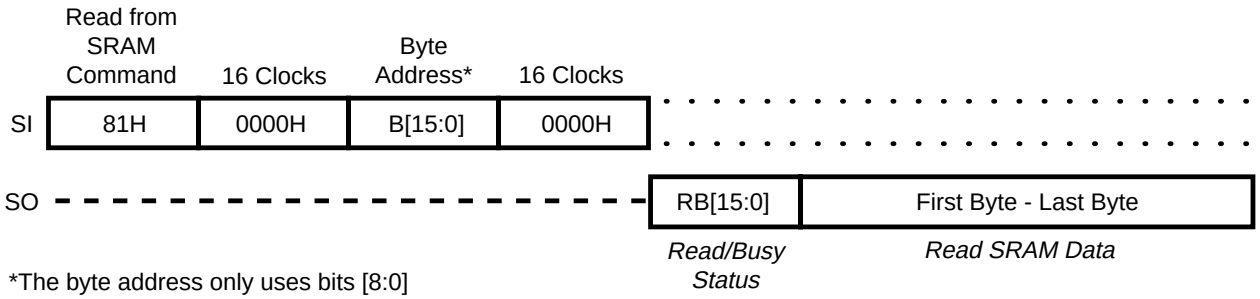


*The sector address only uses bits [8:0], [9:0] or [10:0] Depending on device density
**The byte address only uses bits [8:0]

COMPATIBILITY COMMANDS FOR 25xxxA SERIES DEVICES

Read from SRAM (81H)

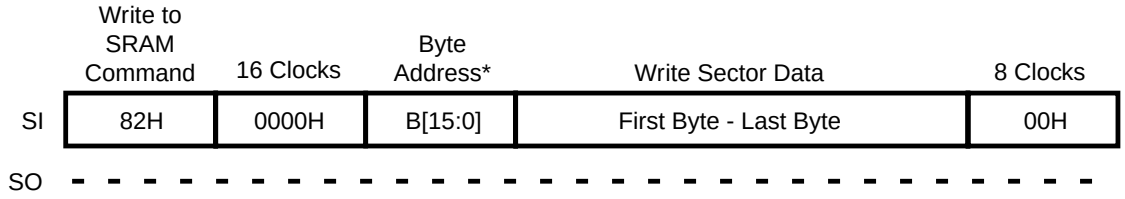
The *Read from SRAM* command (81H) provides access to the 264-Byte SRAM independent of any Flash memory array operations. The command is similar to the *Read from Sector* command except for the sector address field S[15:0] which is replaced with all 0 bits.



*The byte address only uses bits [8:0]

Write to SRAM (82H)

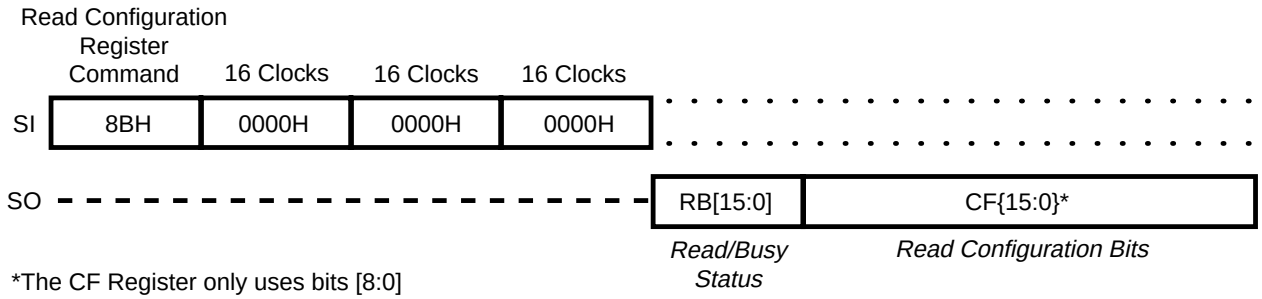
The *Write to SRAM* command (82H) provides access to the 264-Byte SRAM independently of any Flash memory array operation. The command is similar to the *Write to Sector* command sequence except that the sector address field S[15:0] is replaced by all 0 bits. When $\overline{CS}$ is asserted high to complete the command, the contents of the SRAM will be maintained until overwritten through another command or the power is removed. Using the *Write to SRAM* command, data can be loaded in preparation of writing to a sector in memory and then transferred to a selected sector using the *Transfer SRAM to Sector* command.



*The byte address only uses bits [8:0]

Read Configuration Register (8BH)

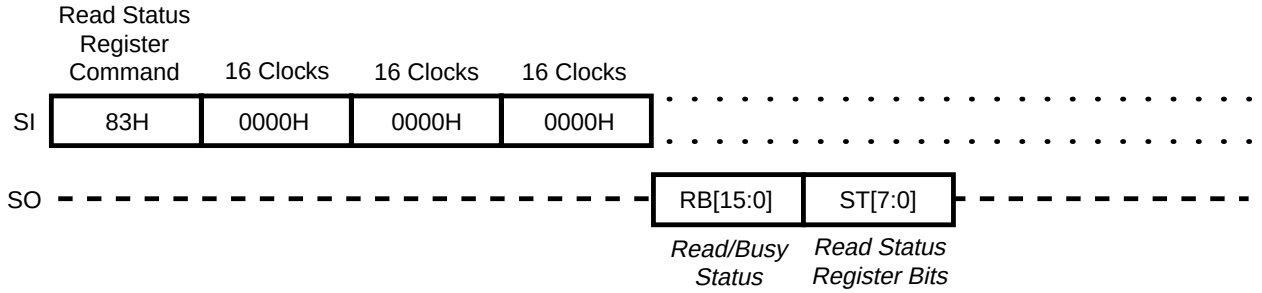
The *Read Configuration Register* command provides access to the configuration register, which stores the current configuration of the $\overline{HOLD}$-R/$\overline{B}$ pin, read clock edge, write protect range, and alternate oscillator frequency (Figure 7). The command sequence is similar to the *Read from Sector* command except that the sector address field S[15:0] and the byte-address field B[15:0] are replaced with all 0 bits. After 16 control clocks and after the Ready/Busy status field has been clocked through, a 16-bit Configuration Data field CF[15:0] provides the contents of the Configuration Register. Although the field is 16-bits long, only bits CF[8:0] are used. All other upper bits are reserved for future features.



*The CF Register only uses bits [8:0]

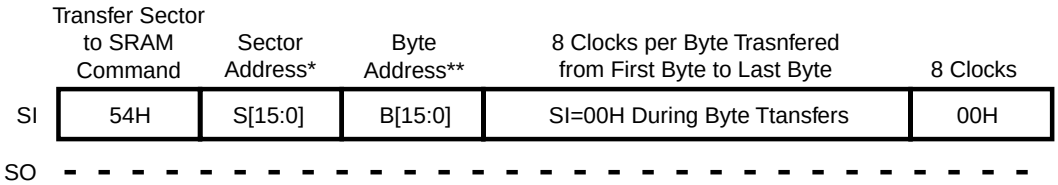
Read Status Register (83H)

The *Read Status Register* command provides access to the status register and its status flags for Ready/Busy (R/$\overline{B}$), SRAM and program buffer transfer operations (TX), Write Enable/Disable ($\overline{WE}$), and Compare Not Equal (CNE) (Figure 8). The command sequence is similar to the *Read From Sector* command except that the sector address field S[15:0] and the byte-address field B[15:0] are replaced by all 0 bits. After 16 clocks and the Ready/Busy status field RB[15:0] has been read, an 8-bit Status field ST[7:0] provides the contents of the Status Register.



Transfer Sector to SRAM Clocked (54H)

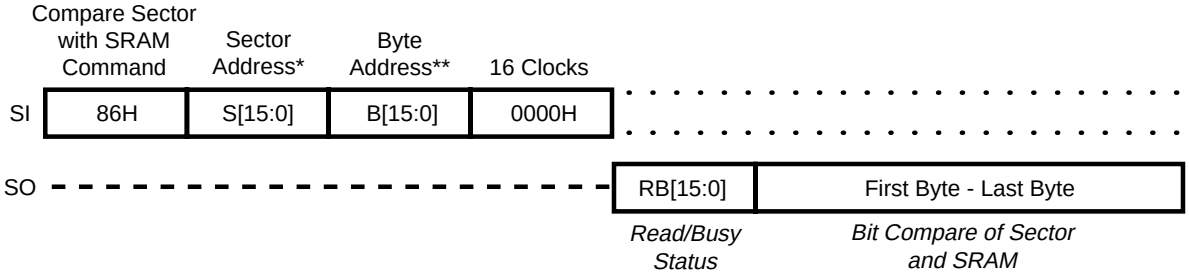
The *Transfer Sector to SRAM Clocked* command (54H) allows the contents of a sector to be transferred directly to the SRAM without having to read the sector out of the device and rewrite it into the SRAM. The command is similar to the *Write to Sector* command except that instead of inputting data from the SI pin, the data is taken from the specified sector and is transferred to the SRAM. Every eight clocks on SCK, a byte from the specified sector to the SRAM will be transferred. Although data on SI is ignored, it is recommended to write data bytes of 00H in order to support the clocking requirements. During the transfer, the SO output is in a high-impedance state. When the last byte address is transferred, the command can be completed by issuing eight more control clocks and asserting $\overline{CS}$ high. If the clock continues to increment past the highest byte-address (107H), the address counter will roll over to byte-0H. This command can also be used to load partial sectors into SRAM



*The sector address only uses bits [8:0], [9:0] or [10:0] Depending on device density
**The byte address only uses bits [8:0]

Compare Sector to SRAM Clocked (86H)

The *Compare Sector to SRAM* command does a bit-by-bit comparison of the data stored in the addressed sector against data in the SRAM. The command is similar to the *Read from Sector* command except that data is not read out of the Serial Output pin (SO). Instead, the SO pin provides a bit-by-bit compare of each sector and SRAM bit. A high (1) per bit will be output if the bit compare is equal. A low (0) per bit will be output if the bit compare is not equal. The compare can start from any location in the 264-byte range as specified by the byte-address field B[15:0]. The byte-address counter is automatically incremented and will wrap around to the first address (0H) if it passes the last address (107H). If any of the compared bits are not equal, then the *Compare Not Equal* (CNE) bit in the Status Register is set to a 1. This bit will stay set until a *Clear Compare Status* command has been issued. This command can also be used to load partial sectors into SRAM



*The sector address only uses bits [8:0], [9:0] or [10:0] Depending on device density
**The byte address only uses bits [8:0]

Sector Format and Tag/Sync Bytes

The first byte of each sector is pre-programmed during manufacturing with a tag/sync value of C9H. Although this byte location of the sector can be changed, it is recommended that it be maintained and incorporated into the application's sector formatting.

The tag/sync values serve two purposes. First, they provide a sync-detect that can help verify if the command sequence was clocked into the device properly. Secondly, they serve as a tag to identify a fully functional (valid) sector. This is especially important if "restricted sector" (-R) devices are ever to be used. Restricted sector devices provide a more cost effective alternative to standard devices with 100% valid sectors. Restricted sector devices have a limited number of sectors that do not meet manufacturing programming criteria over the specified operating range. When such a sector is detected, the first byte is tagged with a pattern other than C9H. In addition to individual sector tagging, all restricted sectors for a given device are listed in the Device Information Sector. For more information see the Device Information Sector Application Note SFAN-02.

High Data Integrity Applications

Data storage applications that use Flash memory or other non-volatile media must take into consideration the possibility of noise or other adverse system conditions that may affect data integrity. For those applications that require higher levels of data integrity it is a recommended practice to use Error Correcting Code (ECC) techniques. The NX-SFK-NXS Serial Flash Development Kit provides a software routine for a 32-bit ECC that can detect up to two bit errors and correct one. The ECC not only minimizes problems caused by system noise but can also extend Flash memory endurance.

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameters	Conditions	Range	Unit
Vcc	Supply Voltage		0 to 7.0	V
V_{IN}, V_{OUT}	Voltage Applied to Any Pin	Relative to Ground	–0.5 to Vcc + 0.5	V
T_{STG}	Storage Temperature		–65 to +150	°C
T_{LEAD}	Lead Temperature	Soldering 10 Seconds	+300	°C

Note:
1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure beyond absolute maximum ratings (listed above) may cause permanent damage.

OPERATING RANGES

Symbol	Parameter	Conditions	Min	Max	Unit
Vcc	Supply Voltage	5.0V	4.5	5.5	V
		3.0V	2.7	3.6	V
T_A	Ambient Temperature, Operating	Commercial	0	+70	°C
		Extended	–20	+70	°C
		Industrial	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (PRELIMINARY) [2]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}	Input Low Voltage			–0.4	—	Vccx0.2	V
V_{IH}	Input High Voltage			Vccx0.6	—	Vcc+0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA	V_{CC} = 4.5V	—	—	0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400 µA	V_{CC} = 4.5V	2.4	—	—	V
V_{OLC}	Output Low Voltage CMOS	V_{CC} = Min, I_{OL} = 10 µA		—	—	0.15	V
V_{OHC}	Output High Voltage CMOS	V_{CC} = Min, I_{OH} = –10 µA		V_{CC}–0.3	—	—	V
I_{IL}	Input Leakage	0 < V_{IN} < Vcc		–10	—	+10	µA
I_{OL}	I/O Leakage	0 < V_{IN} < Vcc		–10	—	+10	µA
I_{CC} (active)	Active Power Supply Current	f_{CLK} @ 8 MHz (1/t_{CP})	V_{CC} = 5V	—	10	15	mA
			V_{CC} = 3V	—	5	10	mA
I_{CCLF} (low frequency)	Active Current Low Frequency. Read	f_{CLK} @1 MHz (1/t_{CP})	V_{CC} = 5V	—	7	10	mA
			V_{CC} = 3V	—	4	7	mA
I_{CCSB} (standby)	Standby Vcc Supply Current	CS = V_{CC}, V_{IN} = Vcc or 0		—	<1	10	µA
C_{IN}	Input Capacitance (1)	T_A = 25°C, V_{CC} = 5V or 3V Frequency = 1 MHz		—	—	10	pF
C_{OUT}	Output Capacitance (1)	T_A = 25°C, V_{CC} = 5V or 3V Frequency = 1 MHz		—	—	10	pF

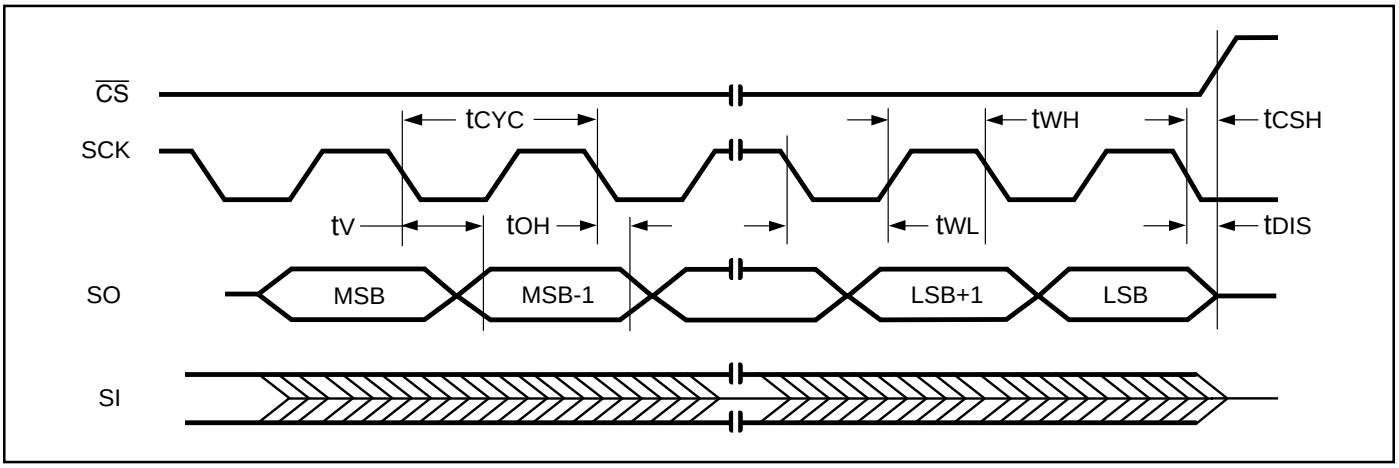
Notes:
1. Tested on a sample basis or specified through design or characterization data.
2. See Preliminary Designation page 31

AC ELECTRICAL CHARACTERISTICS (Preliminary) [4]

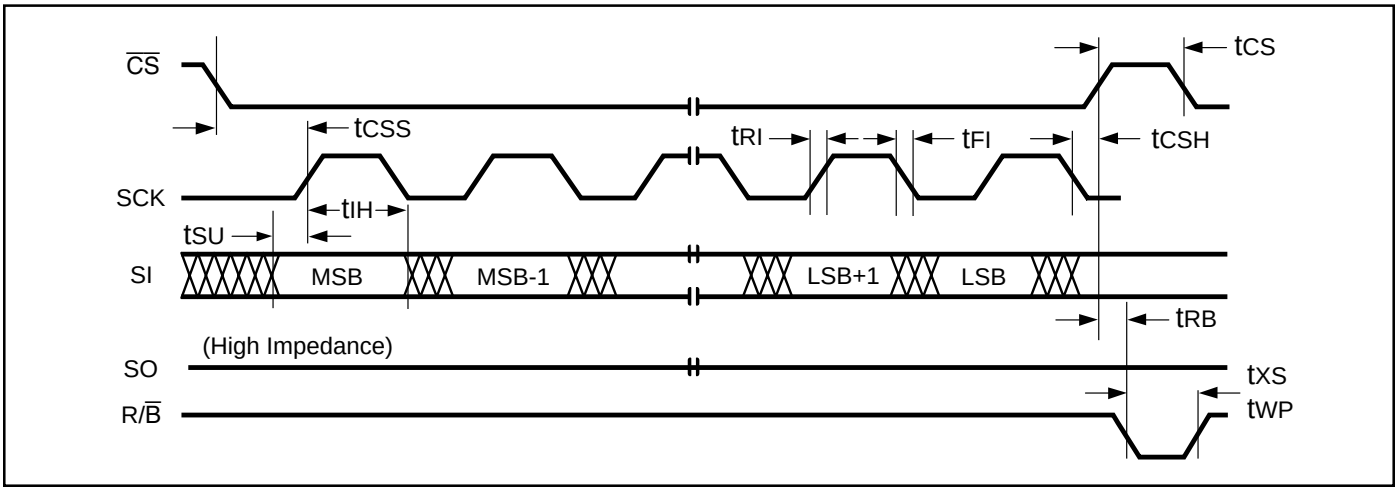
		16 MHz			
Symbol	**Description**	**Min**	**Typ**	**Max**	**Unit**
t_{CYC}	SCK Serial Clock Period [1]	62	—	—	ns
t_{WH} t_{WL}	SCK Serial Clock High or Low Time	24	—	—	ns
t_{RI} t_{FI}	SCK Serial Clock Rise or Fall Time [2]	—	—	5	ns
t_{SU}	Data Input Setup Time to SCLK	25	—	—	ns
t_{IH}	Data Input Hold Time from SCLK	0	—	—	ns
t_{OH}	Data Output Hold Time from SCLK	0	—	—	ns
t_V	Data Output Valid after SCLK [1,3]	—	—	40	ns
t_{CSS}	$\overline{CS}$ Setup Time to Command	100	—	—	ns
t_{CSH}	$\overline{CS}$ Hold Time after Command	100	—	—	ns
t_{WP}	Erase/Write Program Time *(see Write to Sector Command)*	—	5	10	ms
t_{EO}	Erase Only Time *(see Erase Sector/Block Commands)*	—	2	4	ms
t_{WO}	Write Only Time *(see Write Only to Sector Command)*	—	3	6	ms
t_{XS}	Transfer or Compare Sector *(see Transfer/Compare All Command)*	—	100	150	µs
t_{HD}	SCK Setup Time to $\overline{HOLD}$	10	—	—	ns
t_{CD}	SCK Hold Time from $\overline{HOLD}$	30	—	—	ns
t_{CS}	$\overline{CS}$ Deselect Time	160	—	—	ns
t_{RB}	READY / BUSY Valid Time	160	—	—	ns
t_{DIS}	Data Output Disable Time	—	—	60	ns
t_{HZ}	Data Disable/Enable from $\overline{HOLD}$	—	—	60	ns

Notes:
1. To achieve maximum clock performance, the read clock edge will need to be set for rising edge operation in the configuration register (RCE=1).
2. Test points are 10% and 90% points for rise/fall times. All others timings are measured at 50% point.
3. With 30 pF (16 MHz) load SO to GND.
4. See Preliminary Designation page 31

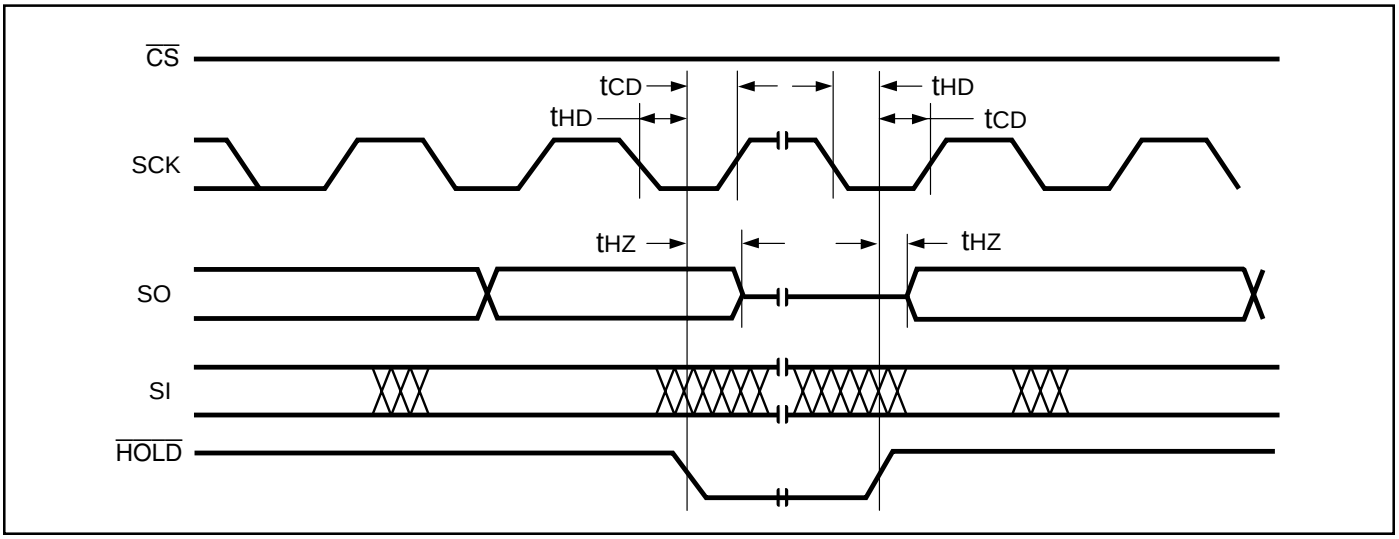
SERIAL OUTPUT TIMING



SERIAL INPUT TIMING

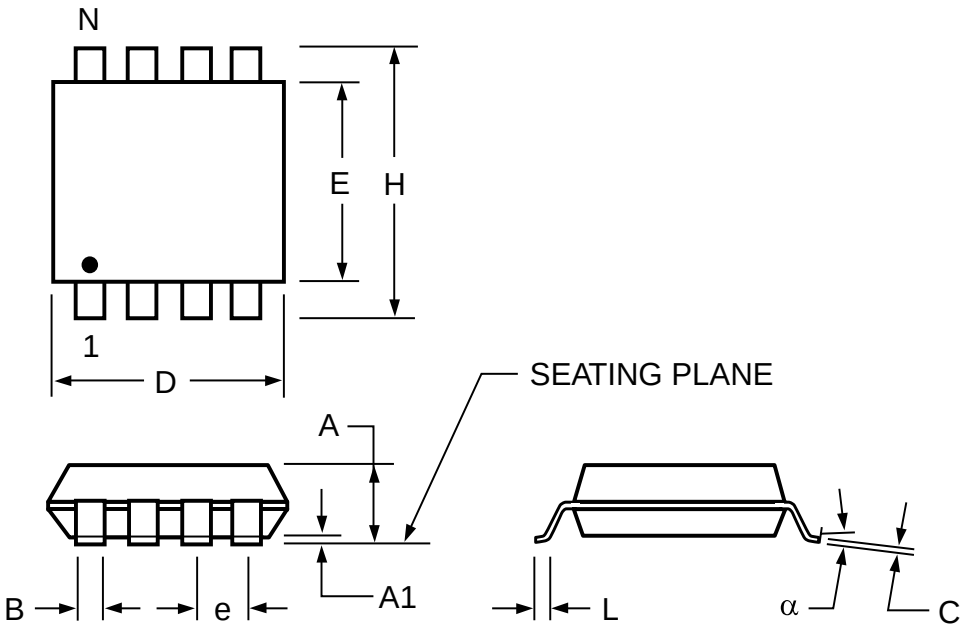


HOLD TIMING



PACKAGING INFORMATION

200-mil Plastic SOIC
Package Code: S

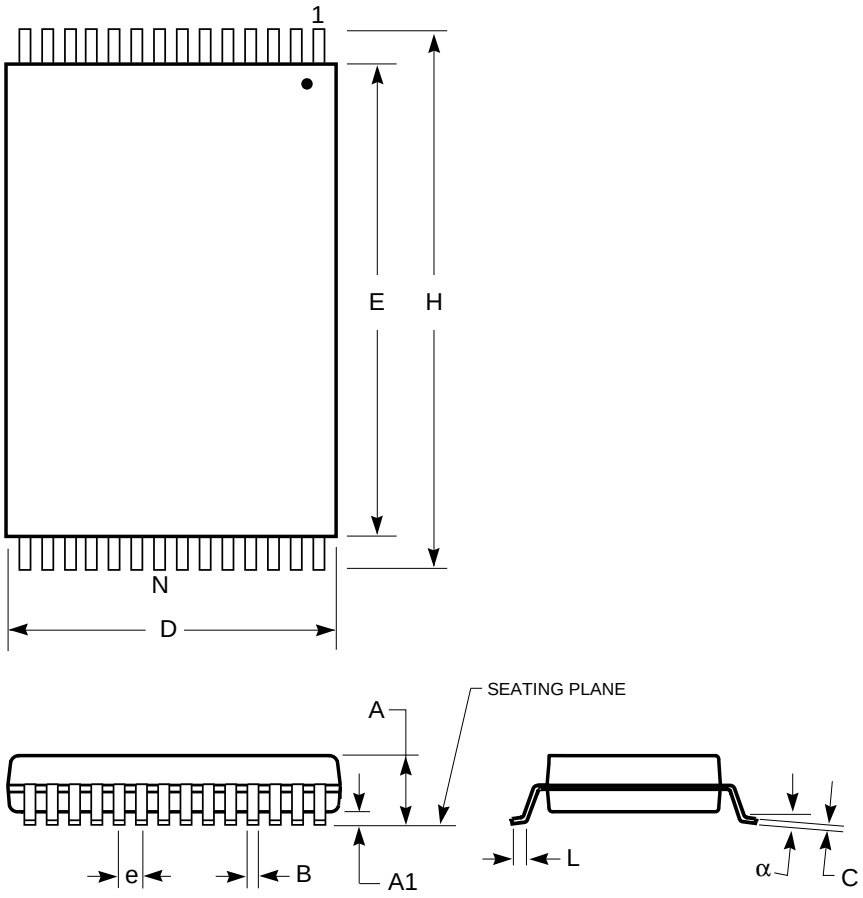


200 mil Plastic SOIC (S)				
	Millimeters		Inches	
Symbol	Min	Max	Min	Max
No. Leads		8		
A	1.780	2.030	0.070	0.080
A1	0.102	0.330	0.004	0.013
B	0.305	0.508	0.012	0.020
C	0.178	0.254	0.007	0.010
D	5.160	5.380	0.203	0.212
E	5.210	5.410	0.205	0.213
e	1.27BSC		0.050 BSC	
H	7.62	8.38	0.300	0.330
L	0.508	0.889	0.020	0.035
α	0^o	8^o	0^o	8^o

Notes:
1. Controlling dimensions: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within .0004 inches at the seating plane.

PACKAGING INFORMATION

Plastic TSOP - 28-pins
Package Code: Type I (V)



Plastic TSOP Type I (V)				
	Millimeters		Inches	
Symbol	Min	Max	Min	Max
No. Leads		28		
A	1.00	1.20	0.039	0.047
A1	0.05	0.20	0.002	0.008
B	0.15	0.25	0.006	0.010
C	0.10	0.20	0.004	0.008
D	7.90	8.10	0.311	0.319
E	11.60	11.80	0.457	0.465
H	13.30	13.50	0.524	0.531
e	0.55 BSC		0.022 BSC	
L	0.50	0.70	0.020	0.028
α	0°	5°	0°	5°

Notes:
1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

PRELIMINARY DESIGNATION

The “Preliminary” designation on an *NexFlash* data sheet indicates that the product is not fully characterized. The specifications are subject to change and are not guaranteed. *NexFlash* or an authorized sales representative should be consulted for current information before using this product.

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(a) the risk of injury or damage has been minimized;

(b) the user assumes all such risks; and

(c) potential liability of *NexFlash* is adequately protected under the circumstances.

ORDERING INFORMATION

Size	Order Part No.	Package
1M-bit	NX25F011B-3V*	SPI, 28-pin, TSOP (Type I) 3V Low Voltage
1M-bit	NX25F011B-3S*	SPI, 8-pin, SOIC 3V Low Voltage
1M-bit	NX25F011B-5V*	SPI, 28-pin, TSOP (Type I) 5V Standard Voltage
1M-bit	NX25F011B-5S*	SPI, 8-pin, SOIC 5V Standard Voltage
2M-bit	NX25F021B-3V*	SPI, 28-pin, TSOP (Type I) 3V Low Voltage
2M-bit	NX25F021B-3S*	SPI, 8-pin, SOIC 3V Low Voltage
2M-bit	NX25F021B-5V*	SPI, 28-pin, TSOP (Type I) 5V Standard Voltage
2M-bit	NX25F021B-5S*	SPI, 8-pin, SOIC 5V Standard Voltage
4M-bit	NX25F041B-3V*	SPI, 28-pin, TSOP (Type I) 3V Low Voltage
4M-bit	NX25F041B-5V*	SPI, 28-pin, TSOP (Type I) 5V Standard Voltage

***Note**: Add -R for Restricted Sector Device (See Serial Flash Application Note SFAN-2 for more information on restricted sector devices).

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