MX•COM, INC.

MX609

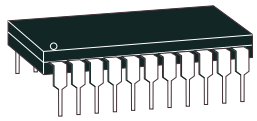
PCN/PCS DELTA MODULATION CODEC

FEATURES

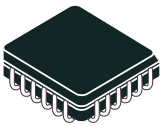
- **Single Chip Full Duplex CVSD CODEC**
- **On-chip Input & Output Filters**
- **Programmable Sampling Clocks**
- **3- or 4-bit Companding Algorithm**
- **Powersave Capabilities**
- **Low Power, Single 5V CMOS**

APPLICATIONS

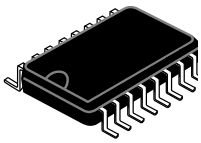
- **Digital PCN/PCS System**
- **Digital Cordless Phones**
- **Digital Delay Lines**
- **Digital Voice Storage**
- **Multiplexers, Switches & Phones**
- **Time Domain Scramblers**



MX609J (CDIP)
MX609P (PDIP)
22 pins



MX609LH
24 pin PLCC



MX609DW
16 pin SOIC

Description

The MX609 is a Continuously Variable Slope Delta Modulation (CVSD) Codec designed for use in cordless telephones. The device is suitable for applications in delta multiplexers, switches and phones. Encoder input and decoder output switched capacitor filters are incorporated on-chip.

Sampling clock rates can be programmed to 16, 32 or 64K bits/second from an internal clock generator or externally injected in the 8 to 64K bits/second range. The internal clocks are derived from an on-chip reference oscillator driven by an externally connected crystal. The sampling clock frequency is output for the synchronization of external circuits.

The encoder has an enable function for use in multiplexer applications. When not enabled the encoder output remains in a high-impedance "tri-state" mode.

Companding circuits may be operated with an externally selectable 3- or 4-bit algorithm. The device may be put in standby mode when Powersave is selected.

The MX609 is a low-power 5V CMOS device. It is available in PDIP, CDIP, PLCC and SOIC packages.

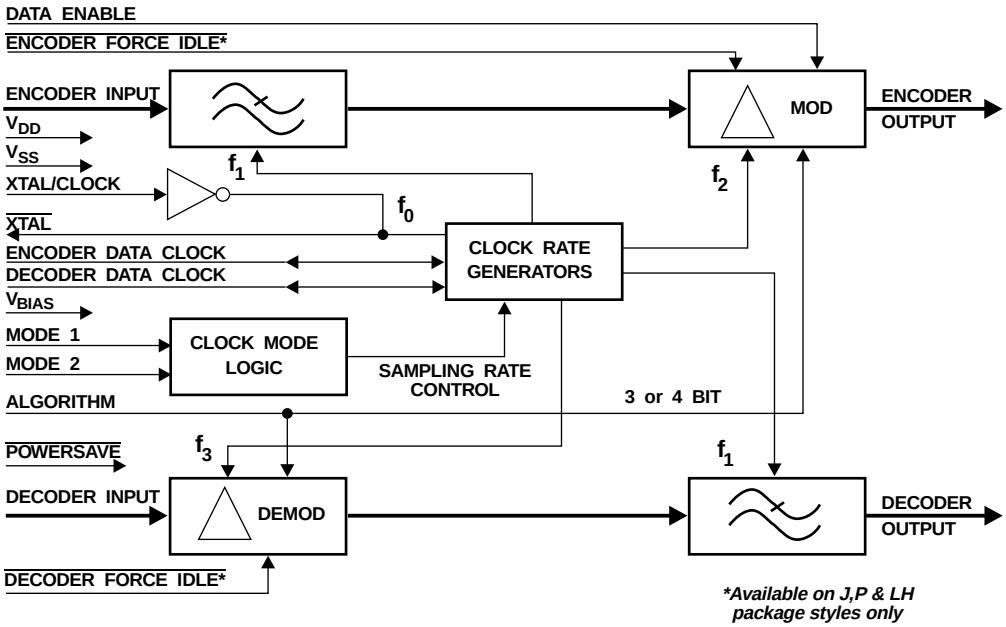


Figure 1 - Internal Block Diagram

PIN FUNCTION CHART

Pin			Function
J/P	LH	DW	
1	1	1	**Xtal/Clock (I/P):** Input to the clock oscillator inverter. A 1.024 MHz Xtal input or externally derived clock is injected here. See Clock Mode pins and Figure 3.
	2		N/C
2	3	2	**Xtal (O/P):** The 1.024 MHz output of the clock oscillator inverter.
3	4		N/C
4	5	3	**Encoder Data Clock:** A logic I/O port. External encode clock input or internal data clock output. Clock frequency is dependent upon clock mode 1,2 inputs and xtal frequency (see Clock Mode pins).
5	6	4	**Encoder Output:** The encoder digital output. This is a three-state output whose condition is set by the Data Enable and Powersave inputs, as shown below: **Data Enable** / **Powersave** / **Encoder Output** 1 / 1 / Enabled 0 / 1 / High Z (open circuit) 1 / 0 / V_{SS}
6	7	--	**Encoder Force Idle:** When this pin is at a logical “0” the encoder is forced to an idle state and the encoder digital output is 0101, a perfect idle pattern. When this pin is a logical “1” the encoder encodes as normal. Internal 1MΩ pullup.
7	8	5	**Data Enable:** Data is made available at the encoder output pin by control of this input. See Encoder Output pin. Internal 1 MΩ pullup.
8	9		N/C
9	10	6	**Bias:** Normally at $V_{DD}/2$ bias, this pin should be externally decoupled by capacitor C_4. Internally pulled to V_{SS} when “Powersave” is a logical “0”.
10	11	7	**Encoder Input:** The analog signal input. Internally biased at $V_{DD}/2$, this input requires an external coupling capacitor. The source impedance should be less than 100Ω. Output channel noise levels will improve with an even lower source impedance. See Figure 3.
11	12	8	**V_{SS}:** Negative Supply
12	13		N/C
13	14	9	**Decoder Output:** The recovered analog signal is output at this pin. It is the buffered output of a lowpass filter and requires external components. During “Powersave” this output is open circuit.
14	15		N/C
15	16	10	**Powersave:** A logic “0” at this pin puts most parts of the codec into a quiescent non-operational state. When at a logical “1”, the codec operates normally. Internal 1 MΩ pullup.
	17		N/C
16	18	--	**Decoder Force Idle:** A logic “0” at this pin gates a 0101... pattern internally to the decoder so that the Decoder Output goes to $V_{DD}/2$. When this pin is a logical “1” the decoder operates as normal. Internal 1MΩ pullup.
17	19	11	**Decoder Input:** The received digital signal input. Internal 1 MΩ pullup.
18	20	12	**Decoder Data Clock:** A logic I/O port. External decode clock input or internal data clock output, dependent upon clock mode 1,2 inputs. See Clock Mode pins.
19	21	13	**Algorithm:** A logic “1” at this pin sets this device for a 3-bit companding algorithm. A logical “0” sets a 4-bit companding algorithm. Internal 1 MΩ pullup.

Pin			Function
J/P	LH	DW	
20 21	22 23	14 15	**Clock Mode 2:** / **Clock Mode 1:** Internal 1 MΩ Pullups.

Clock Mode 1	Clock Mode 2	Facility
0	0	External Clocks
0	1	Internal,64kb/s=f÷16
1	0	Internal,32kb/s=f÷32
1	1	Internal,16kb/s=f÷64

Clock rates refer to f = 1.024MHz Xtal/clock input. During internal operation the data clock frequencies are available at the ports for external circuit synchronization. Independent or common data rate inputs to Encode and Decode data clock ports may be employed in the External Clocks mode.

22	24	16	**V_{DD}:** Positive Supply. A single +5 volt power supply is required.

CODEC INTEGRATION

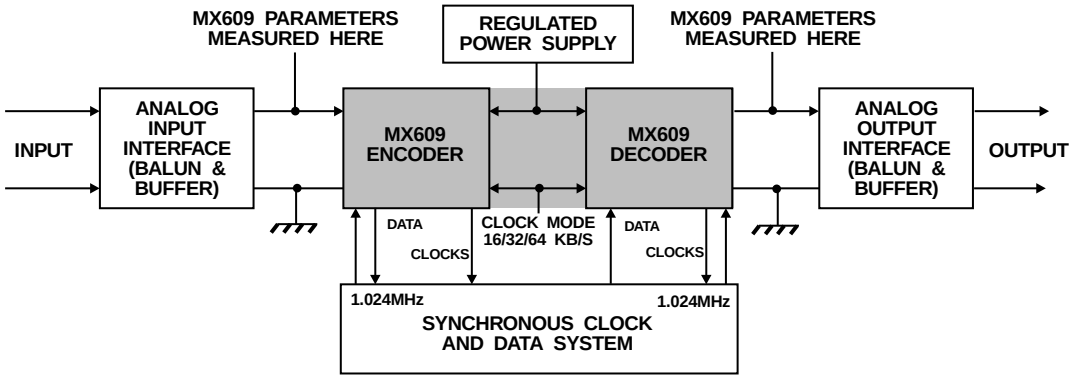
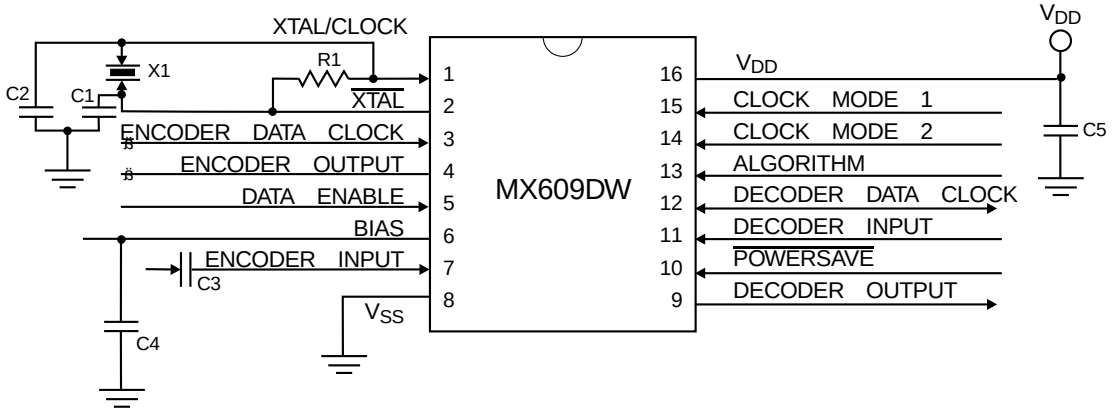


Figure 2 - System Configuration Showing the MX609



Component	Value	Note
R1	1M	Oscillator inverter bias resistor.
C1	33p	Xtal circuit load capacitor.
C2	68p	Xtal circuit load capacitor.
C3	1.0µ	Encoder input coupling capacitor. The drive source impedance to this input should be less than 100Ω. Output idle channel noise levels will improve with an even lower source impedance.
C4	1.0µ	Bias decoupling capacitor.
C5	1.0µ	V_{DD} decoupling capacitor.
X1	1.024MHz	A 1.024 MHz xtal/clock input will yield exactly 16/32/64 kb/s data clock rates. Xtal circuitry shown is in accordance with MX-COM's Xtal Oscillator Application Note (see Appendix).

Tolerances: Resistors = 10%, Capacitors = 20%.

Figure 3 - Recommeded External Components

CODEC TIMING INFORMATION

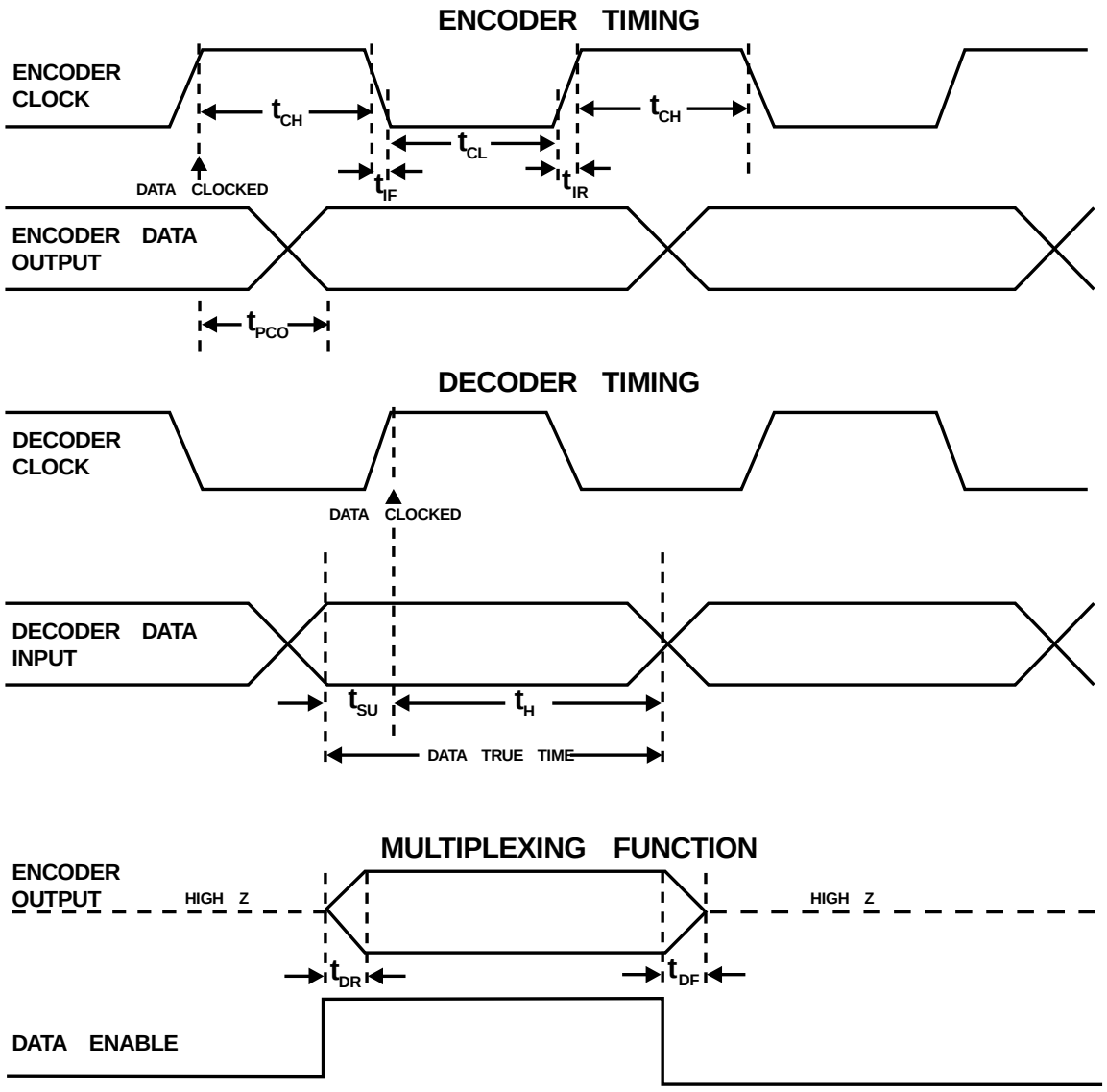


Figure 4 - Codec Timing

Abbreviation	Description	Time
t_{CH}	Clock 1 pulse width	1.0µs min.
t_{CL}	Clock 0 pulse width	1.0µs min.
t_{IR}	Clock rise time	100ns typ.
t_{IF}	Clock fall time	100ns typ.
t_{SU}	Data set-up time	450ns max.
t_H	Data hold time	600ns min.
$t_{SU} + t_H$	Data true time	1.5µs typ.
t_{PCO}	Clock to output delay time	750ns typ.
t_{DR}	Data rise time	100ns typ.
t_{DF}	Data fall time	100ns typ.
	Xtal input frequency	1.024MHz

CODEC PERFORMANCE

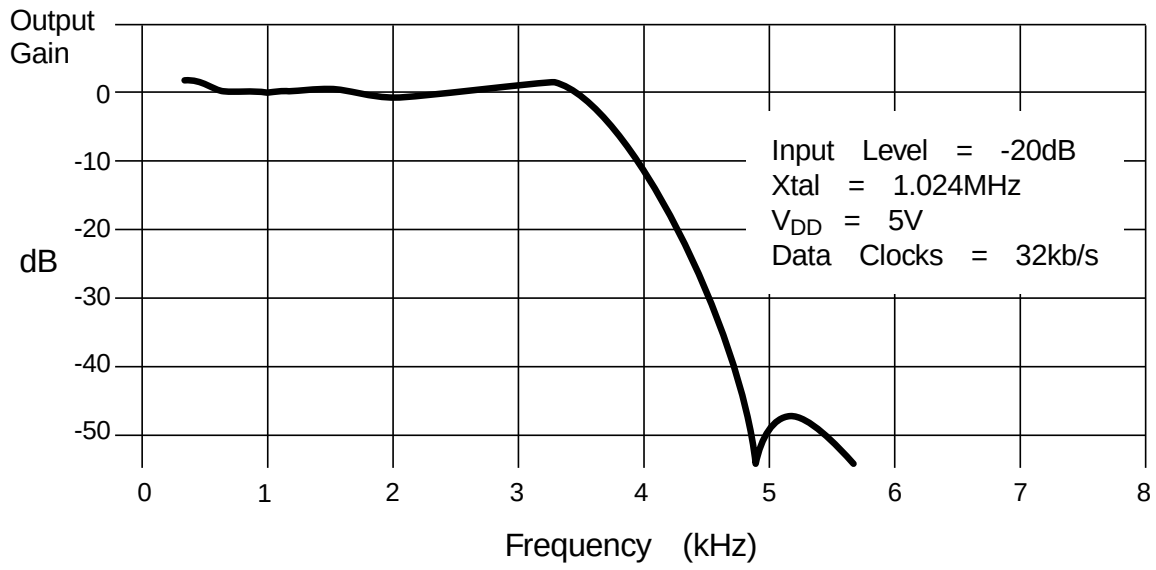


Figure 5 - Typical Codec Frequency Response

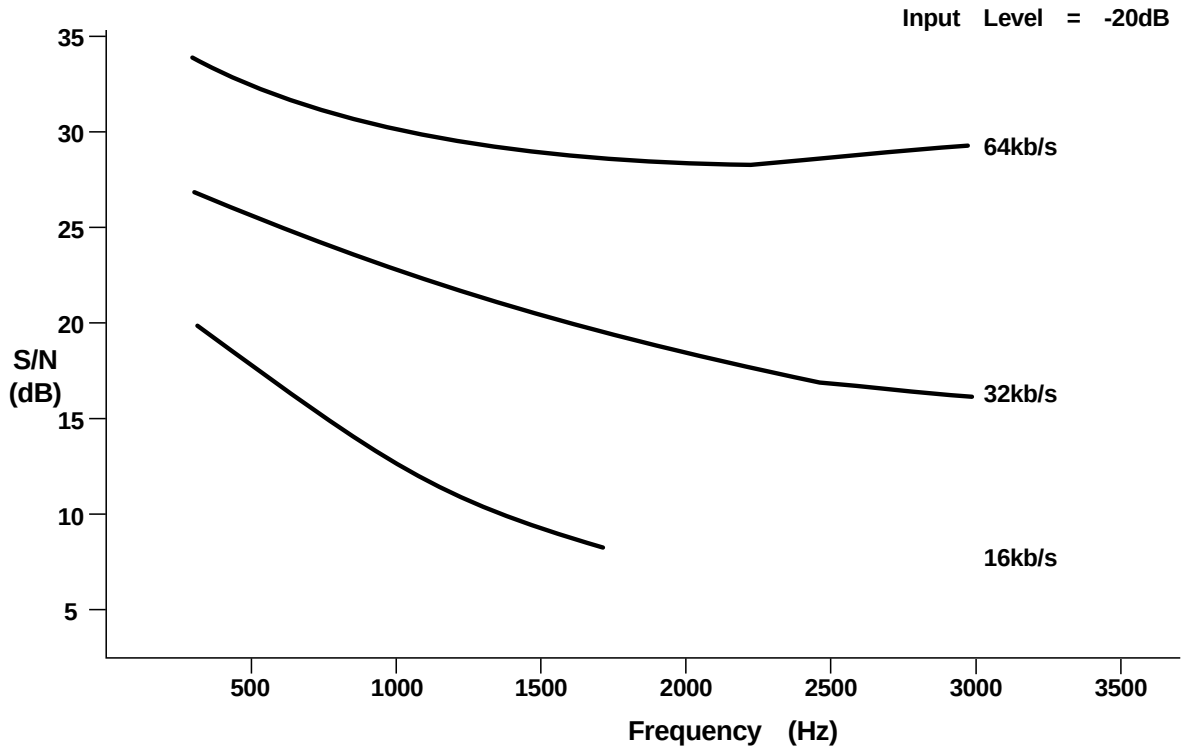


Figure 6 - Typical S/N Ratio with Input Frequency

SPECIFICATIONS

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0V
Input Voltage at any pin (ref V_{ss}=0V)	-0.3 to (V_{DD}+ 0.3V)
Sink/Source Current	
(Supply)	±30mA
(Other Pins)	±20mA
Total Device Dissipation (@ T_{amb}=25°C)	800mW max.
Derating	10 mW/°C
Operating Temperature	-30°C to +70°C
Storage Temperature	-40°C to +85°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

Audio Test Frequency = 820Hz

T_{AMB} = 25°C

Sample Clock Rate = 32 kb/sec

Xtal/Clock f_o = 1.024MHz

Audio level 0dB ref (0 dBm0) = 489mVrms

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage	1	4.5	5.0	5.5	V
Supply Current (Enabled)		-	3.5	-	mA
Supply Current (Powersave)		-	500	-	µA
Input Logic “1”		3.5	-	-	V
Input Logic “0”		-	-	1.5	V
Output Logic “1”		4.0	-	-	V
Output Logic “0”		-	-	1.0	
Digital Input Impedance					
Logic I/O Pins		-	10	-	MΩ
Logic Input Pins, Pullup Resistor	2	300	-	-	kΩ
Digital Output Impedance		-	4	-	kΩ
Analog Input Impedance		-	100	-	kΩ
Analog Output Impedance	6	-	800	-	Ω
Three State Output Leakage		-	±4	-	µA
Insertion Loss	2	-	0	-	dB
Dynamic Values	1				
Encoder:					
Analog Signal Input Levels	6	-30	-	+8	dB
Principal Integrator Frequency		-	275	-	Hz
Encoder Passband		-	3400	-	Hz
Compand Time Constant		-	4	-	ms
Decoder:					
Analog Signal Output Levels	6	-30	0	+8	dB
Decoder Passband	3	-	3400	-	Hz
Encoder Decoder (Full Codec):					
Passband		300	-	3400	Hz
Stopband		6	-	10	KHz
Stopband Attenuation		-	60	-	dB
Passband Gain		-	0	-	dB
Passband Ripple		-3	-	+3	dB
Output Noise (Input Short Circuit)		-	-60	-	dB
Perfect Idle Channel Noise (Encode Forced)	7	-	-63	-	dB
Group Delay Distortion	4				
(1000Hz-2600Hz)		-	-	450	µs
(600Hz-2800Hz)		-	-	750	µs
(500Hz-3000Hz)		-	-	1.5	ms
Xtal/Clock Frequency		500	1024	1500	kHz

NOTES:

1. Dynamic characteristics specified at 5V only.
2. All logic inputs except Encoder and Decoder Data Clocks.
3. With passband gain of ±1dB.
4. Group Delay Distortion for the full codec is relative to the delay with an 820Hz, -20dB signal at the encoder input.
5. Relative Timings are shown in Figure 4.
6. Recommended values.
7. Forced Idle Encode/Decode not available on DW package.

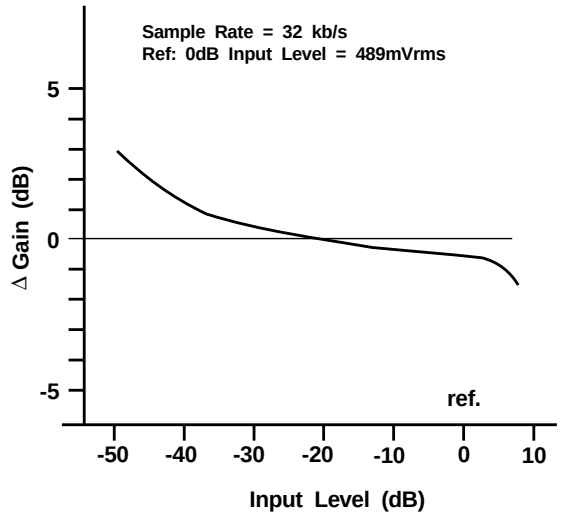


Figure 7 - Typical Variation of Gain with Input Level

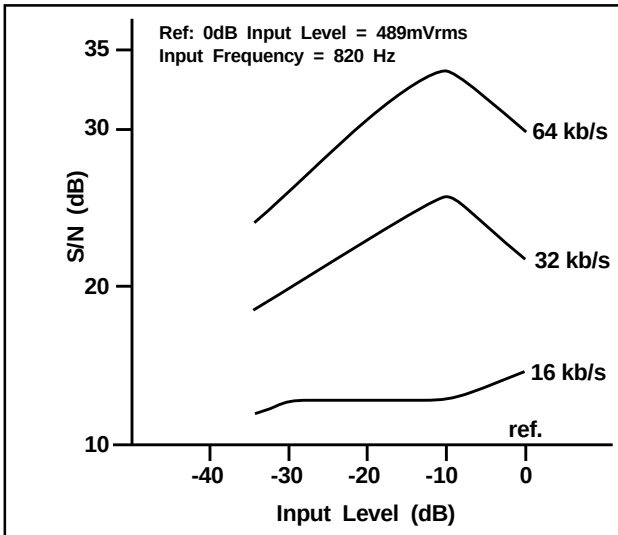
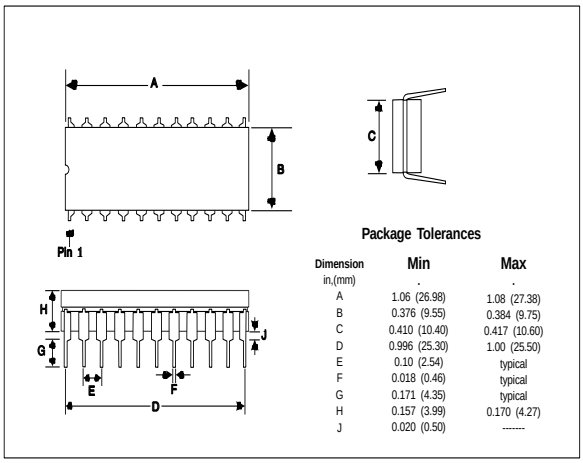


Figure 8 - Typical S/N Ratio with Input Level

Package Outline

The MX609 packages available are shown below. Pin 1 is indicated by an indent spot. Pins number counter-clockwise when viewed from the top.



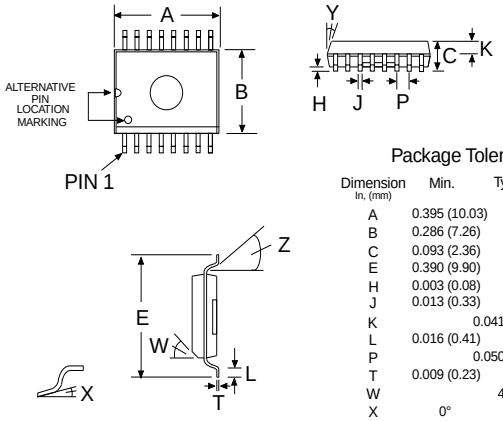
Package Tolerances

Dimension in,(mm)	Min	Max
A	1.06 (26.98)	1.08 (27.38)
B	0.376 (9.55)	0.384 (9.75)
C	0.410 (10.40)	0.417 (10.60)
D	0.996 (25.30)	1.00 (25.50)
E	0.10 (2.54)	typical
F	0.018 (0.46)	typical
G	0.171 (4.35)	typical
H	0.157 (3.99)	0.170 (4.27)
J	0.020 (0.50)	-------

Figure 9 - MX609J 22-pin Ceramic Dual In-Line

Handling Precautions

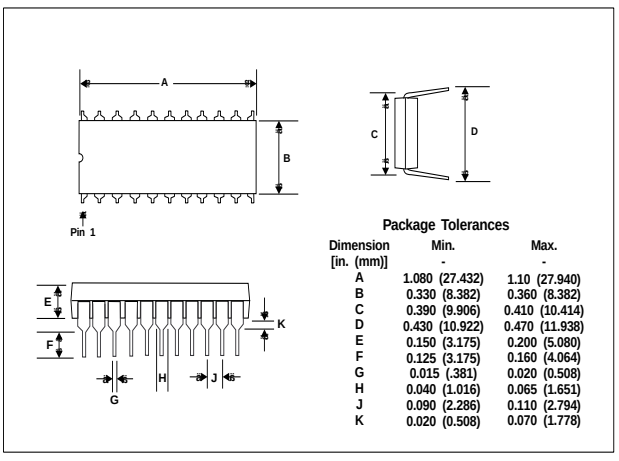
The MX609 is a CMOS LSI circuit which includes input protection. However, precautions should be taken to prevent static discharges which may cause damage.



Package Tolerances

Dimension In, (mm)	Min.	Typ.	Max
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

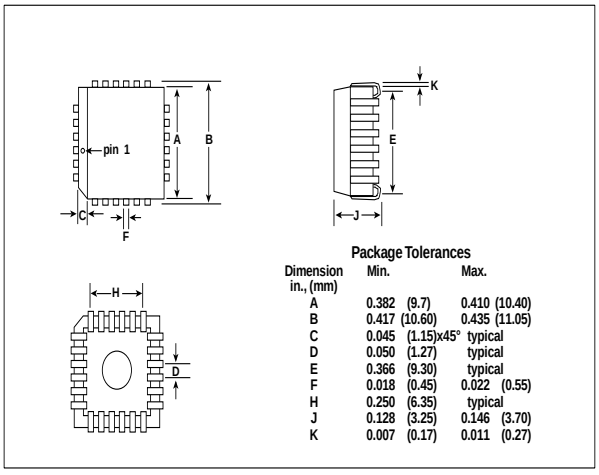
Figure 10 - MX609DW 16-pin Small-Outline IC



Package Tolerances

Dimension [in. (mm)]	Min.	Max.
A	1.080 (27.432)	1.10 (27.940)
B	0.330 (8.382)	0.360 (8.382)
C	0.390 (9.906)	0.410 (10.414)
D	0.430 (10.922)	0.470 (11.938)
E	0.150 (3.175)	0.200 (5.080)
F	0.125 (3.175)	0.160 (4.064)
G	0.015 (.381)	0.020 (0.508)
H	0.040 (1.016)	0.065 (1.651)
J	0.090 (2.286)	0.110 (2.794)
K	0.020 (0.508)	0.070 (1.778)

Figure 11 - MX609P 22-pin Plastic Dual In-Line



Package Tolerances

Dimension in., (mm)	Min.	Max.
A	0.382 (9.7)	0.410 (10.40)
B	0.417 (10.60)	0.435 (11.05)
C	0.045 (1.15)x45°	typical
D	0.050 (1.27)	typical
E	0.366 (9.30)	typical
F	0.018 (0.45)	0.022 (0.55)
H	0.250 (6.35)	typical
J	0.128 (3.25)	0.146 (3.70)
K	0.007 (0.17)	0.011 (0.27)

Figure 12 - MX609LH 24-pin PLCC