MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX609

An Audio Delay circuit based on the MX609 CVSD Codec

1. Introduction

The schematic diagram shown on the following page is an audio delay circuit based on the MX609 CVSD Codec. In addition to the MX609, the circuit uses a Motorola MCM6287 64K x 1 bit RAM, two 4520 counter ICs, and a 4069 inverter chip. It provides up to two seconds of delay. This circuit provides a starting point for a designer who wishes to implement an audio delay circuit. MX-COM makes no guarantee of its performance and assumes no responsibility for its use in any product.

2. Circuit Operation

In the following operational description, a bar over a signal name is used to indicate an active low signal. For example, W is an active low write enable signal. On the MX609P, Clock Mode 1, pin 22, is tied to VDD and Clock Mode 2, pin 21, is tied to ground to set the encode and decoder clocks for a sampling rate of 32 kb/s. The Encoder Force Idle, Powersave, and Decoder Force Idle inputs, pins 6, 15, and 16, respectively, are tied to VDD to set them inactive. The Data Enable input, pin 7, is tied to VDD to make the encoded data available at the Encoder Output, pin 5. Pin 19, the Algorithm select input, is tied to ground to select a four-bit companding algorithm. The other inputs are the same as recommended for "External Component Connections" shown in the MX-COM data book.

The audio signal to be delayed is input to pin 10 of the MX609, the Encoder Input, and is converted to a serial stream of digital data. The serial data are output on pin 5, the Encoder Output, and connected to pin 13, the D input, of the MCM6287 memory chip. The Decoder Data Clock output from pin 18 of the MX609 is connected to pin 1 of the 4069 inverter. The output of the inverter, pin 2, is connected to pin 10 of the MCM6287, the W input, and to pin 3 of the 4069, the input to second inverter. Pin 4, the inverter output, is connected to the enable input of the first 4520 counter.

The enable input is taken from the second inverter to ensure that the 4520 counters increment after the W signal into the 81C71 transitions from low to high. The clock inputs of each of the 4520s, pins 1 and 9, are tied to ground so that only the enable inputs control when the counters increment. The reset inputs, pins 7 and 15, are also tied to ground so that they never reset the counters. The individual four bit counters in the 4520s are cascaded to produce a 16 bit counter. The counter outputs, Q15 - Q0, are connected to the address inputs, A15 - A0, of the MCM6287.

There are switches between Q15 and A15 and between Q14 and A14. The switches allow the number of bits of the counter, and therefore the length of the delay, to be adjusted. When the Decoder Data Clock falls from high to low, the counter, and therefore the address, increments. Since the W input to the memory, pin 17, is the complement of the clock, it rises from low to high, latching the encoded data bit at the D input. The E input to the MCM6287, pin 12, is tied to ground so that the memory is always selected. When W is high and the address is stable, a valid data bit appears at the Q output, pin 17, of the MCM6287. The address of the data bit appearing at Q is one greater than the address of the bit that was just written, so the counter must cycle through its entire range before a data bit that has been written into the memory can be read. Therefore, a data bit output from the MX609 at the Encoder Output pin is delayed by the number of clock periods of the range of the counter. The delay is given by:

$$\text{Delay} = (T \text{ sec/cycle}) * (2N \text{ cycles})$$

Where: T = period of Decoder Data Clock
N = number of bits used in counter

If all 16 bits of the counter are used, and the decoder clock frequency is 32 kHz, then the delay would be:

Delay: = (1/32000) sec/cycle * (216) cycles
= 2.048 seconds

In this example, all locations of the memory are used. If a shorter delay is desired, the switches connecting the counter outputs and address inputs can be opened. If only 14 bits of the counter are used, then the delay is reduced by a factor of four, to 0.512 seconds. The range of delays could be increased even more by adding more switches and by making the sampling clock frequency adjustable. The Q output, pin 9, of the MCM6287 is connected to the Decoder Input, pin 17, of the MX609. The decoder clocks in the serial digital data stream from the memory and converts it to an analog signal which is output at pin 13, the Decoder Output. The Decoder Output is the delayed audio signal.

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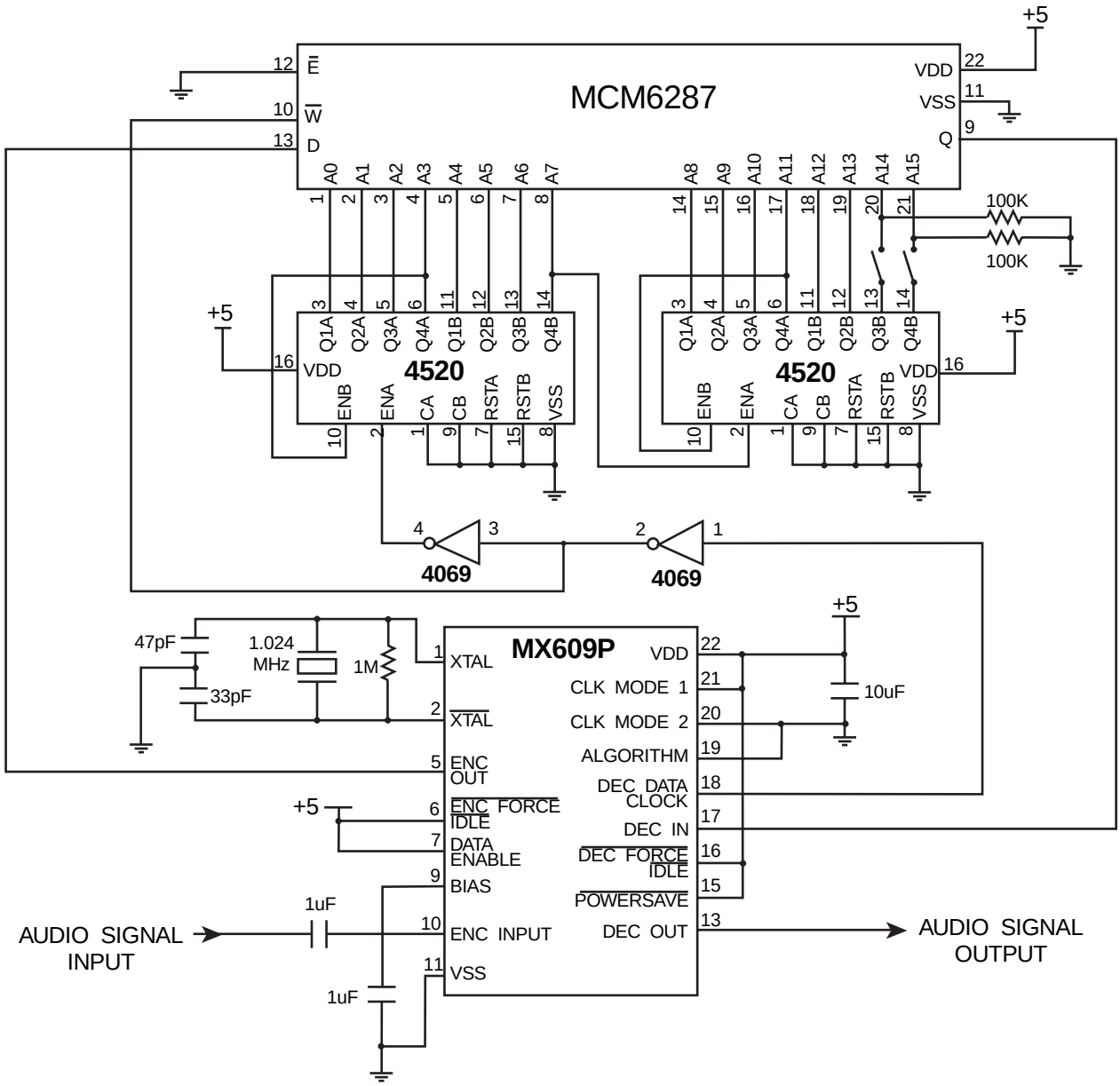

Figure 1: Audio Delay Circuit