MX•COM, INC. MiXed Signal ICs

APPLICATION NOTE

Switched Capacitor Interfacing Anti-Aliasing and Smoothing Filters

1. Introduction

Switched Capacitor Networks (SCNs) are sampled data systems and therefore are governed by the principles of discrete time signal processing. In this context, “discrete time” means the signal is sampled prior to processing. However, the amplitude is continuous – unlike Digital Signal Processing (DSP) systems where both amplitude and time are discrete.

VLSI technology (generally CMOS) has facilitated complete integration of SCNs on a single monolithic chip. Filters utilizing Switched Capacitor techniques (SCFs) are composed of switches, capacitors and opamps. Notice resistors are not mentioned. The resistors normally present in active filters are approximated by switched capacitors. By taking advantage of matching properties of CMOS capacitors, SCFs can be fabricated with low tolerance levels (less than 0.1%) and virtually any order.

The wireless and wireline telecom industries have made extensive use of SCFs. Even with the move towards digital technology and the ensuing popularity of DSP in the communications industry, SCNs are frequently employed where cost and power consumption are critical. SCNs generally have relatively high sampling rates (typically greater than 20 times the bandwidth of the interest). Due to their discrete time nature, aliasing and output smoothing must be addressed. Often a simple single pole filter (R-C network) suffices, but the location of these poles must be carefully thought out during the design process. The world is still analog.

The purpose of this paper is to address the need for anti-aliasing and smoothing filters for SCFs. First, the basics of sampling will be reviewed. The fundamentals of SCNs will follow this, and finally the design of anti-aliasing and smoothing filters for SCFs is addressed.

2. Sampling [3]

Before a continuous signal is processed by a discrete time filter it must first be sampled. Referring to Figure 1, sampling is the process of instantaneously capturing the level of a continuous signal at some predetermined rate. This predetermined rate is the sampling frequency. As the sampling rate increases (Figure 1) the sampled signal begins to approximate the original continuous signal.

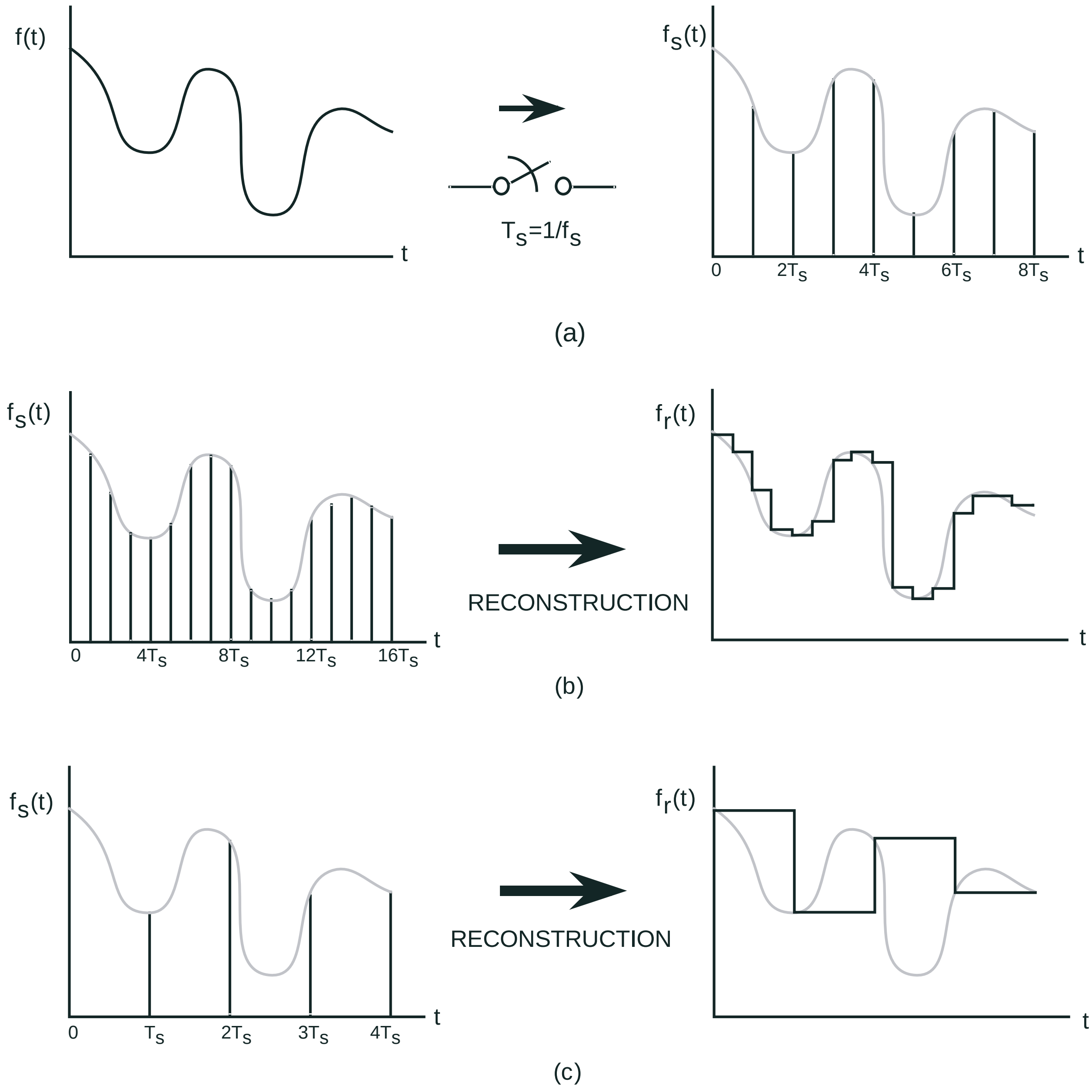

Figure 1: Waveform Sampling:
(a) sampling process, (b) reconstruction with acceptable sampling rate,
(c) reconstruction with unacceptable sampling rate

On the other hand, as the sampling frequency decreases (Figure 1) the samples move further apart in time, yielding a reconstructed signal that does not resemble the original. The limit on how far apart these samples can become without losing information is the basis for Shannon's sampling theorem.

Shannon's original work on sampling and information theory [3] stated the sampling theorem as:

"If a function f(t) contains no frequencies higher than *f* cycles per second it is completely determined by giving its ordinates at a series of points spaced (1/2*f*) seconds apart."

A formal derivation is obtained by convolving the Fourier transform of the continuous signal with the Fourier transform of an infinite sequence of impulse functions.

$$F_S(\omega) = \frac{1}{2\pi}\left[F(\omega) * S(\omega)\right]$$

$$FS(\omega) = \frac{1}{2\pi}\int_{-\infty}^{\infty} F(x)S(\omega - x)dx$$

Where:

$F_S(\omega)$ = sampled signal spectrum
$F(\omega)$ = original signal spectrum
$S(\omega)$ = spectrum for a sequence of impulses
ω = radian frequency ($2\pi f$)

The result of the convolution is the original signal spectrum repeated at multiples of the sampling frequency as shown in Figure 2. Notice that if the sampling frequency is less than twice the bandwidth of the original signal then the replica centered at the sampling frequency will overlap and distort the original. This undesirable phenomenon is aliasing. Aliasing will be avoided if,

$$f_S \geq 2B$$

Where:

f_S = sampling frequency , Hz
B = bandwidth of original signal, Hz

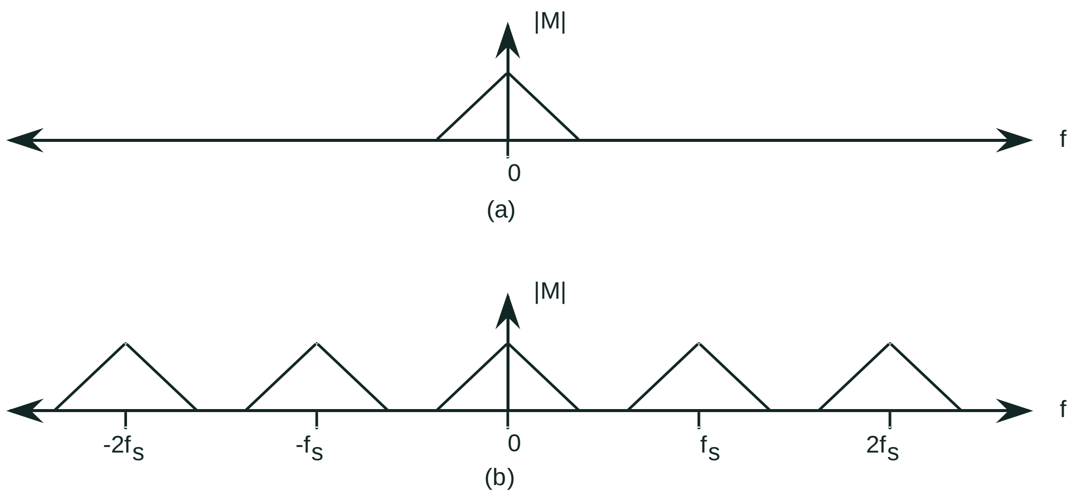

Figure 2: Frequency Spectrum of (a) continuous time signal, (b) sampled signal

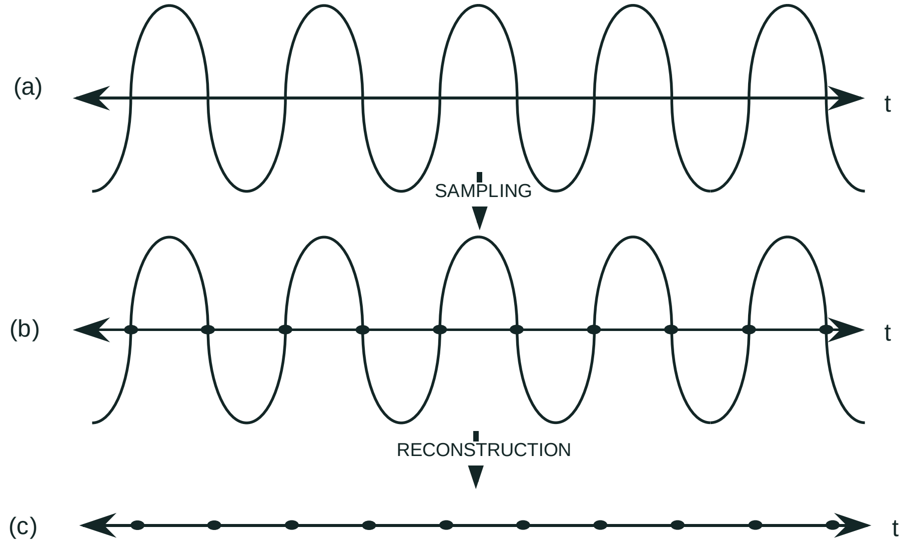

Figure 3: Time domain representation of sampling at f_S = 2B, (a) continuous signal, (b) sampled signal, (c) reconstructed signal

Shannon's sampling theorem is mathematically sound although, in most cases, it is not practical to sample a signal at exactly twice its highest frequency component. Figure 3 shows a sinewave sampled at **2B** samples per second, where **B = 1/T** and **T** is the period of the sinewave. Notice the difference between the reconstructed wave shapes and the original unsampled signal. This type of error is not the result of aliasing, yet it could cause deceptive results. A mathematician might claim that there is no information in a continuous sinewave that never changes amplitude or frequency. This is a fact. However, if a signal is sampled at exactly **2B**, some of the original signal may be lost or distorted.

If the system designer is not concerned with the possibility of losing some of the original signal, and wanted to sample at **2B**, he or she would still be facing the problem of bandlimiting. Bandlimiting is necessary to avoid aliasing. Figure 4 shows the spectrum of a sampled signal. Notice that for f_S **= 2B** the bandlimiting filter must have infinite attenuation at the frequency **B**. A filter that matches this requirement is physically unrealizable.

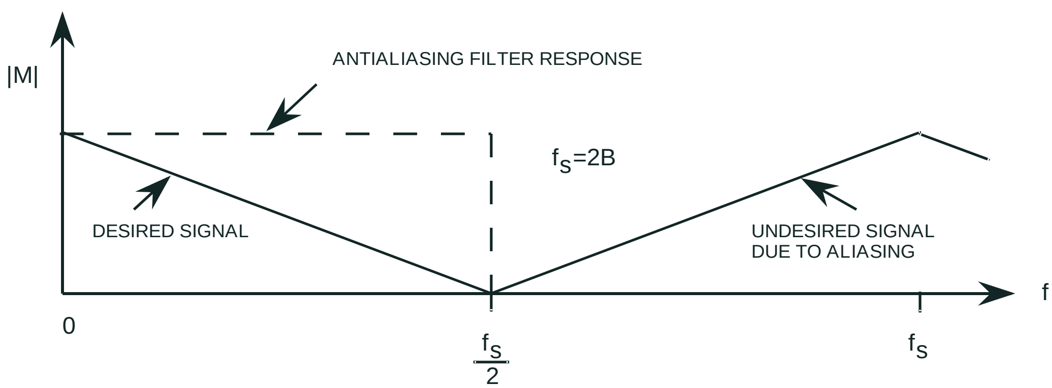

Figure 4: Anti-aliasing filter required for sampling at exactly 2B

3. SCN Concepts [1]

A single pole active filter (inverting integrator) is shown in Figure 5. This circuit is the primary building block for most active filters.

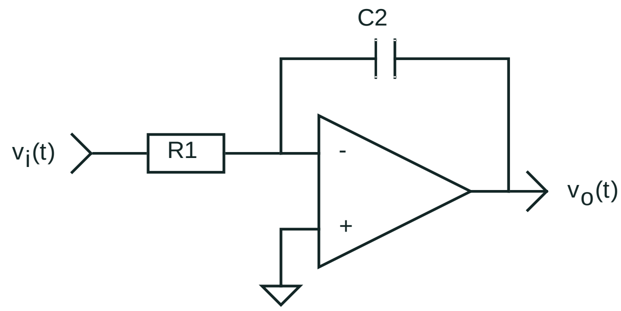

Figure 5: Active R-C Integrator

The output is defined by

$$v_O(t) = -\frac{1}{RC}\int_0^t v_I(\tau)d\tau$$

Hence, the output is an integrated version of the input, scaled by **-1/RC**. The pole frequency is determined by the value of **R** and **C.**

$$fp = \frac{1}{2\pi RC}$$

For a pole frequency of 3000Hz, (5) implies RC=53.05µs. A possible implementation, selecting C2 = 10pF (relatively large capacitor for CMOS technology), requires R=5.305MΩ. A monolithic resistor of this value would consume excessive amounts of silicon and is subject to significant variation with process and temperature. Integrated capacitors are also subject to variation with process and temperature. In addition, capacitor variations are independent of resistor variations.

A more practical realization is shown in Figure 6.

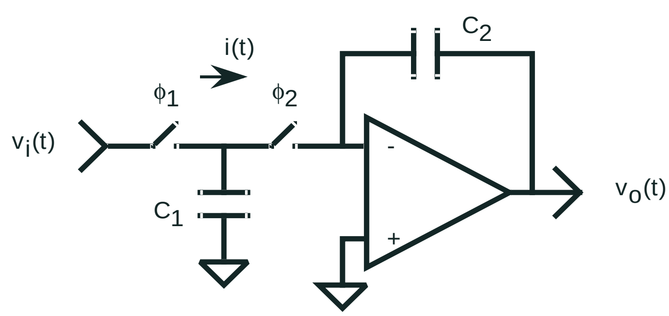

Figure 6: SC Integrator

Notice **R** is replaced by a capacitor and two switches. The function of the resistor is now approximated by transferring charge from $v_i(t)$ to the inverting input of the opamp at intervals determined by clocks $\phi 1$ and $\phi 2$. To ensure complete charge transfer $\phi 1$ and $\phi 2$ must not overlap as shown in Figure 7.

An approximate analysis of Figure 6 reveals the average current through the switches is

$$i = \frac{\Delta q}{T} \quad = \frac{C_1}{T}(v_i - v_1)$$

or

$$i = \frac{1}{R}\,(v_i - v_1)$$

Where:

$$R = \frac{T}{C_1}$$

Looking back at the previous example for a pole frequency of 3000Hz, using T=10µs (f_{clk}=100kHz), yields C_1=1.885 pF. Hence, the integrator can be realized with two capacitors that track with process and temperature. No longer is the absolute value of the capacitors important, only their ratio.

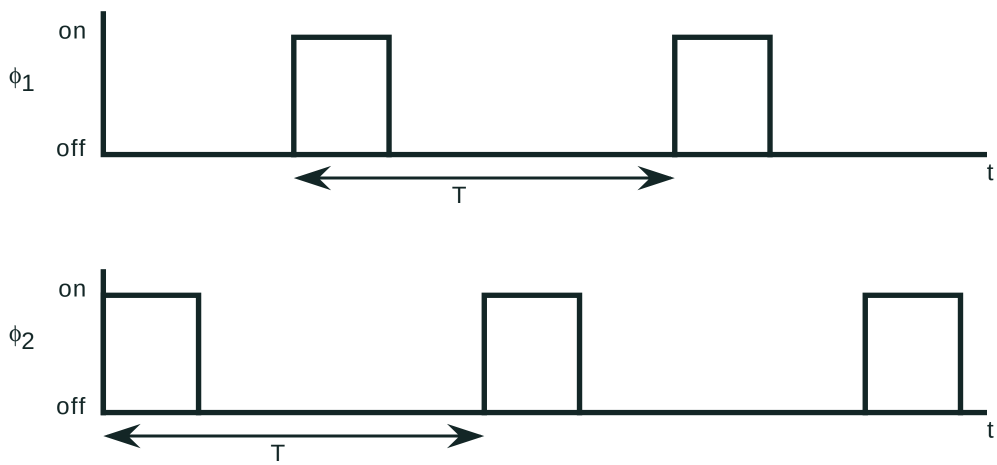

Figure 7: Non-overlapping clocks for SC Integrator

4. Anti-aliasing and Smoothing Filters for SCNs [2]

SCFs approximate active-RC filters by replacing resistors with switched capacitors. As the clock frequency (sampling rate) tends towards infinity the SCF becomes equivalent to the continuous time filter. In other words, higher clock frequency yields a better approximation of the desired response. Also, higher clock frequency lessens the requirements of the anti-aliasing filter (AAF) and smoothing filter (SMF). However, there are upper limits on clock frequency. Although SCFs have been implemented with clock frequencies greater than 1MHz, typical telecom filters (BW less than 10kHz) are clocked at or below 250kHz.

One factor which opposes higher clock frequencies is large capacitor ratios. Referring to the example in section 3.0,

using 1MHz in place of 100kHz, C_1 becomes 0.1885 pf. The ratio between C_1 and C_2 is now 53.05 where it was 5.305. Large capacitor ratios consume more silicon area and are more sensitive to process and temperature variations. Hence, the final sampling rate is a compromise between SCF implementation complexity and SMF/AAF requirements.

SMFs and AAFs can be integrated, but they are subject to the same problems associated with the continuous time RC integrator discussed in section 3.0 and are generally implemented externally. In some cases, where input and output signals are band limited externally, additional circuitry for AAFs and SMFs is not required. A block diagram of a typical SCF system, including AAF and SMF is shown in Figure 8.

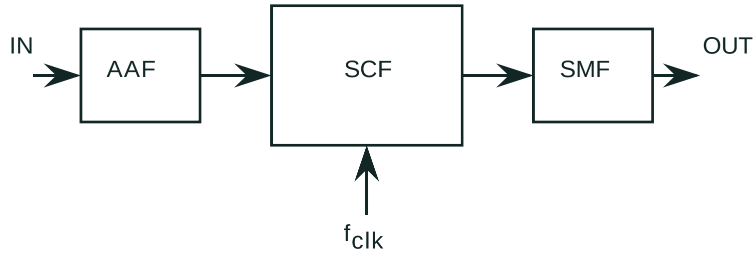

Figure 8: SCF system with AFF and SMF

To determine AAF and SMF requirements the system designer must know the sampling frequency (f_{clk}) and the bandwidth (BW) or cutoff frequency (f_{co}) of the SCF. For discussion purposes, assume f_{clk} =100kHz and f_{co} =5kHz. Recall from section 2.0, if any signal energy is present at the input, with frequency f_S greater than 1/2 f_{clk}, it will be aliased to f_{clk} - f_S. Hence, an input with f_S =99kHz will be aliased to 1kHz. This aliased signal will appear as noise in the passband of the SCF. To eliminate or reduce the effect of this noise the AAF must band limit the input signal to f_{clk} - f_{co} (see Figure 9).

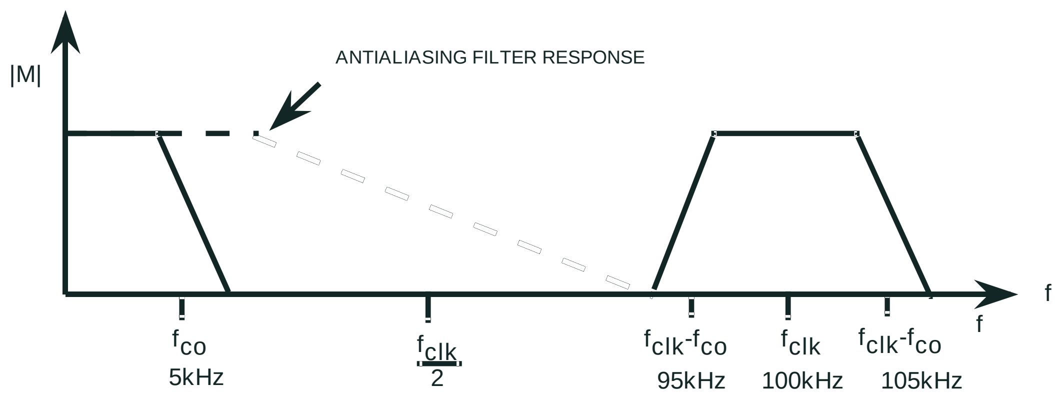

Figure 9: AAF requirements for SCF system

To obtain 20 dB suppression of aliased noise the minimum requirement for the AAF is a first order section (single pole) with it’s cutoff frequency set to 9.5kHz (20 dB/decade/pole). Placing the pole at 9.5kHz minimizes the effect on the SCF passband response. To obtain further suppression more poles are necessary.

The single pole AAF can be implemented with a simple RC at the input to the SCF. The values for can be arrived at by using

$$RC = \frac{1}{2\pi f p}$$

Where:

fp = pole frequency

For the AAF response depicted in Figure 9, RC = 16.75ms. Setting C = 0.1µf yields R = 168Ω. The simple RC network should be used with caution–capacitive loading can cause stability problems. Also, the value of the resistor should be insignificant compared to the SCF input impedance.

A superior solution makes use of an additional opamp forming a damped integrator (see Figure 10). Often this opamp will be available on the SCF chip.

The complete network, including R1, C1, R2 and C2, forms a bandpass filter with a frequency response characteristic as shown in Figure 11.

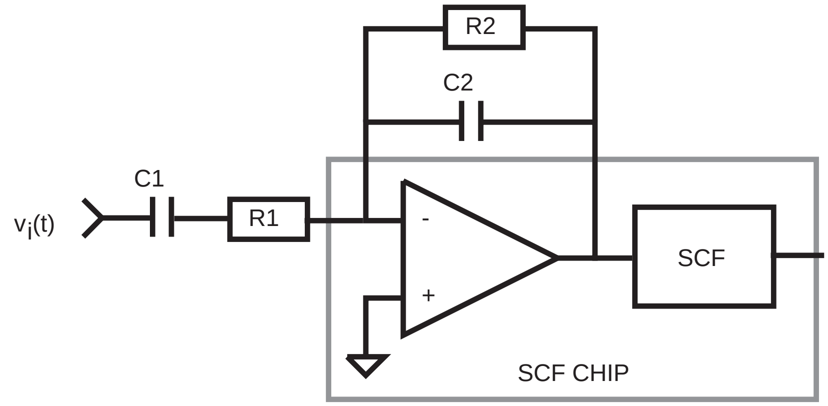

Figure 10: Active RC AAF

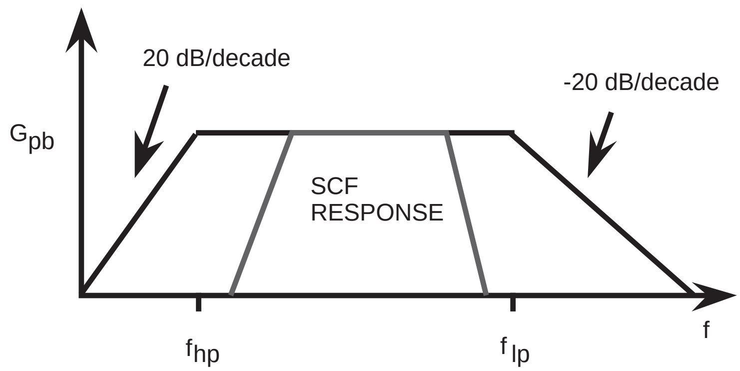

Figure 11: AAF frequency response

The highpass cutoff (f_{hp}) and lowpass cutoff (f_{lp}) are determined by

$$f_{hp} = \frac{1}{2\pi R_1 C_1}$$

and

$$f_{lp} = \frac{1}{2\pi R_2 C_2}$$

The passband gain is set by

$$G_{pb} = \frac{R2}{C2}$$

C_1 is not required if the input signal is biased properly (SCF internal bias = external bias).

To meet the AAF requirements shown in Figure 9 (assuming unity passband gain, f_{lp} = 9.5kHz and f_{hp} = 100 Hz) $\mathbf{R_1} = \mathbf{R_2}$ = 100KΩ, $\mathbf{C_2}$ = 168pf and $\mathbf{C_1}$ = 0.0159µf.

SMF requirements are similar to those of the AAF. The SCF output is a sampled signal and therefore contains replicas of the SCF response at multiples of the sampling frequency. If left unfiltered these replicas appear as high frequency (clock) noise. In some cases this is tolerable. However, in systems where minimum noise is critical the SMF is required.

5. Conclusion

Switched capacitor filters are sampled data systems and hence require anti-aliasing filters at their inputs and smoothing filters at their outputs. The simplest form (and often sufficient) of these filters is the single pole RC network. Other forms such as active RC networks and higher order filters can yield distinct benefits. In any case, application of switched capacitor filters must be viewed at the system level in order to realize optimum performance.

6. REFERENCES

[1] R. Gregorian, K. W. Martin, and G. C. Temes, "Switched-Capacitor Circuit Design," Proceedings of the IEEE, pp. 941-966, August 1983.

[2] L. P. Huelsman and P. E. Allen, Introduction to the Theory and Design of Active Filters, McGraw-Hill, New York, 1980.

[3] A. B. Jerri, "The Shannon Sampling Theorem - Its Various Extensions and Applications: A Tutorial Review," Proceedings of the IEEE, pp. 1565-1596, November 1977.