MIC8030

High-Voltage Display Driver

General Description

The MIC8030 is a CMOS high voltage liquid crystal display driver. Up to 38 segments can be driven from four CMOS level inputs (CLOCK, DATA IN, LOAD and CHIP SELECT). The MIC8030 is rated at 50V. Data is loaded serially into a shift register, and transferred to latches which hold the data until new data is received.

The backplane can be driven from external source, or the internal oscillator can be used. If the internal oscillator is used, the frequency of the backplane will be determined by an external resistor and capacitor. The oscillator need not be used if a DC output is desired.

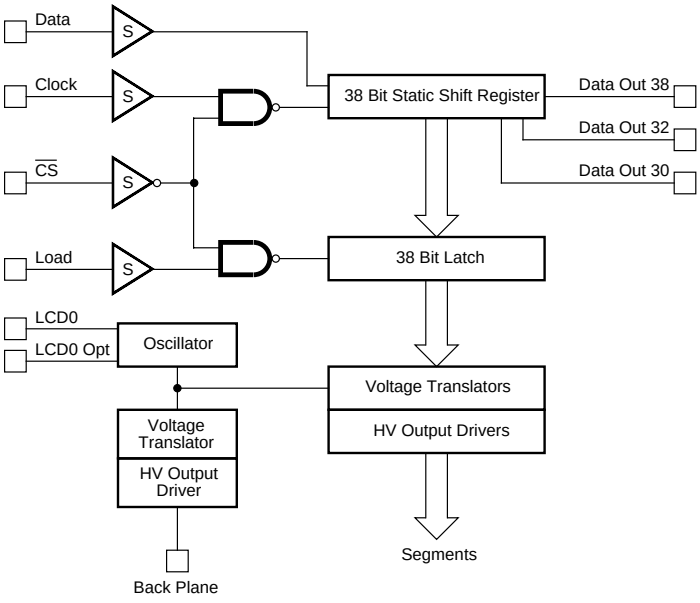
Features

- High Voltage Outputs capable of a driving up to 100 volt outputs from 5 to 15 volt logic
- Drives 30, 32, or 38 segments
- Cascadable
- On chip Oscillator or External Backplane Input
- CMOS construction for wide supply range and low power consumption
- Schmitt Triggers on all inputs
- CMOS, PMOS, and NMOS compatible

Applications

- Dichroic and Standard Liquid Crystal Displays
- Flat Panel Displays
- Print Head Drives
- Vacuum Fluorescent Displays

Functional Diagram

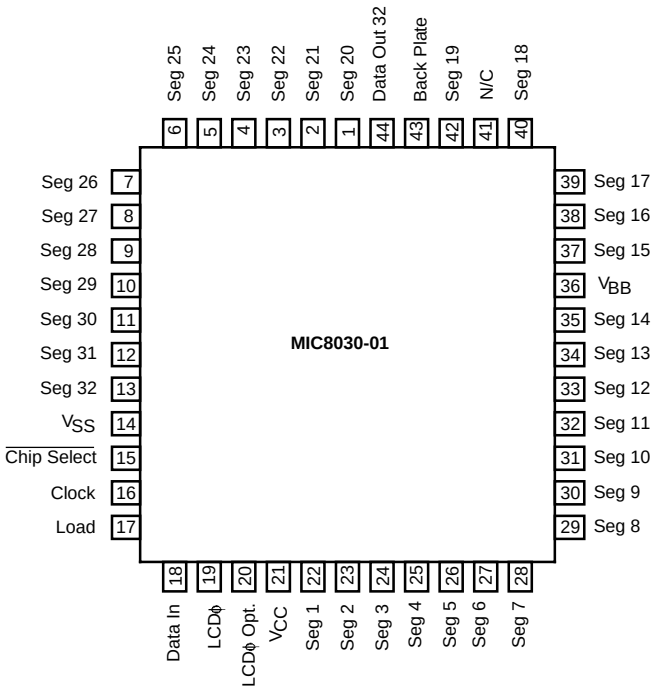


Ordering Information

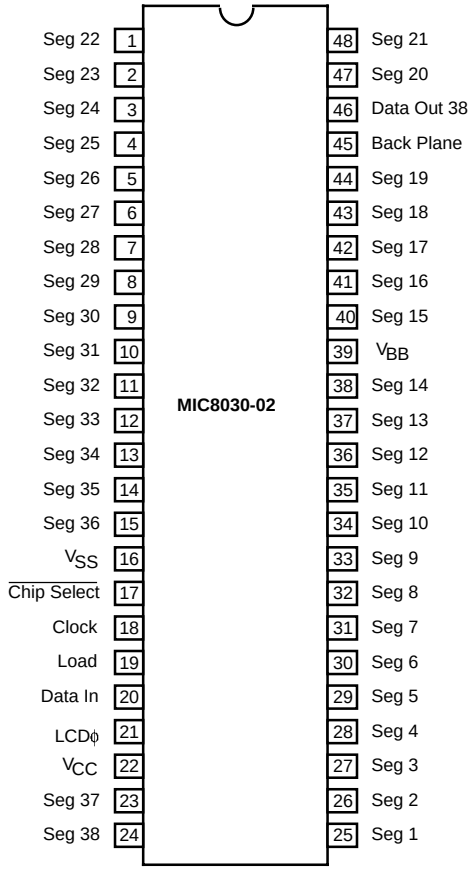
Part Number	Temperature Range	Package
MIC8030-01AEB	–55°C to +125°C	44-lead Cer Quad
MIC8030-01CV	0°C to +70°C	44-pin PLCC
MIC8030-02CN	0°C to +70°C	48-pin Plastic DIP

* AEB indicates units screened to MIL-STD 883, Method 5004, condition B, and burned-in for 1-week.

Pin Configuration 44-Pin Cer Quad - E 44-Pin LCC -L 44-Pin PLCC -V



Pin Configuration 48-Pin Plastic DIP - N



Functional Description

With CHIP SELECT tied low, serial data is clocked into the shift register at each falling edge of the CLOCK input. Pulling LOAD high will cause a parallel loading of the shift register contents into the latches. If load is left high, the latches are transparent.

A logic “1” clocked into the shift register corresponds to that segment being on, and that segment is out of phase with the backplane.

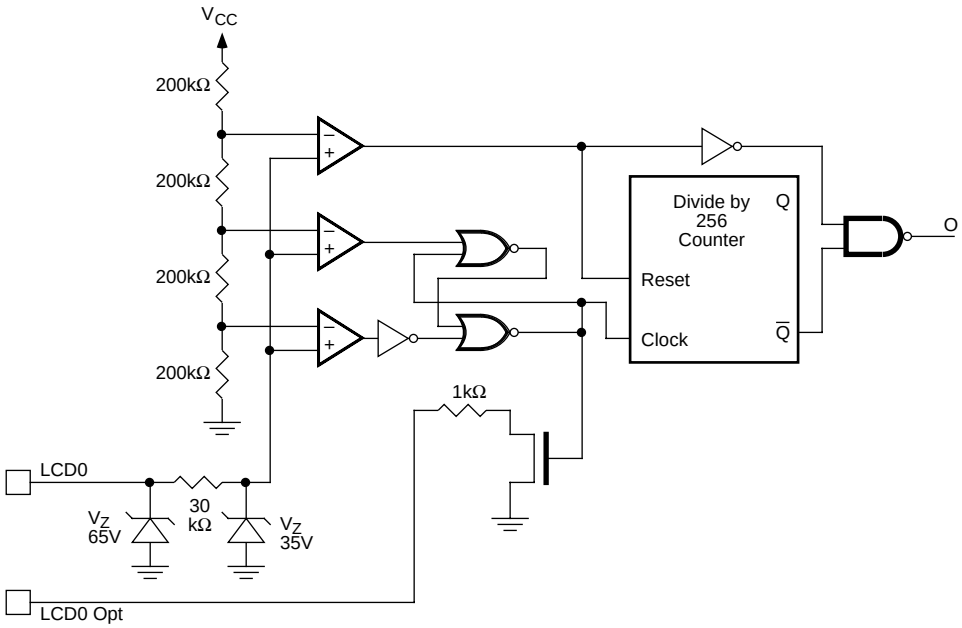
The backplane may be externally driven or the internal oscillator can be used. If LCDϕ is externally driven, the backplane will be in phase with the input; LCDϕ OPT is not connected. The internal oscillator is used by shorting LCDϕ OPT to LCDϕ, connecting a capacitor to ground, and a resistor to V_{CC}. The frequency of the backplane will be 1/256 of the input frequency, and is given as: f = 10/[R(C + .0002)] at V_{DD} = 5V, R in kΩ, C in μF.

Example: R = 150 kΩ, C = 420 pF: f = 108 Hz

For displays with more than 38 segments, two or more MIC8030 may be cascaded by connecting DATA OUT of the previous stage with DATA IN of the next stage; CLOCK, LOAD and CHIP SELECT of all following stages should be tied to the control lines of the first MIC8030/MIC8031. The backplane output of the first stage should be tied to LCDϕ of all following stages, the LCDϕ OPT must be left unconnected on those stages. If the internal oscillator is used, and V_{BB} > 50V then an external 330 kΩ resistor must be used between the BACKPLANE of the first stage and LCDϕ of all following stages.

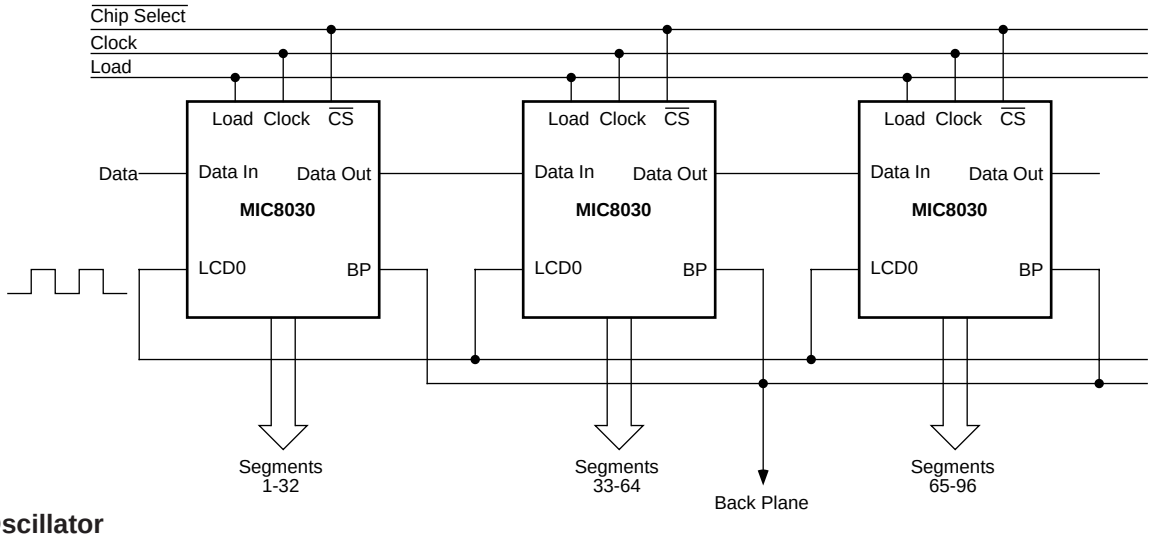
Packaging options available include DATA OUT 30, 32 or 38 with the corresponding number of segments, and the availability of LCDϕ OPT. Types of packages include plastic and ceramic DIPs, surface mount packages, plastic and ceramic Leadless Chip Carriers and custom packaging.

Internal Oscillator Circuit

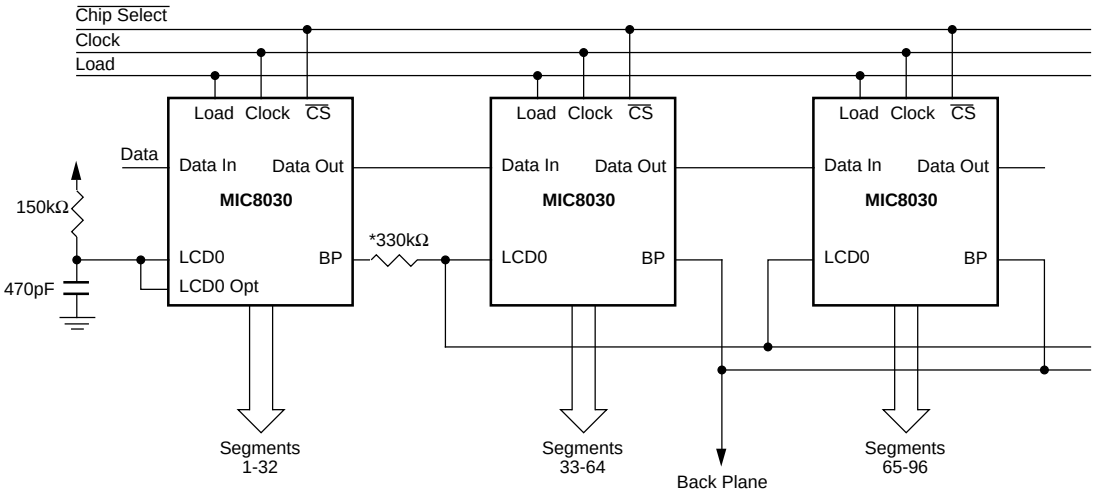


Typical Application

External Oscillator



Internal Oscillator



*Required if using MIC8031 with V_{BB} > 50V.

Absolute Maximum Ratings

V_{CC}	18V
V_{BB} (MIC8030)	75V
Inputs (CLK, DATA IN, LOAD, $\overline{CS}$)	–0.5V to 18V
Inputs (LCD0)	–0.5V to 50V
Storage Temperature	–65°C to +150°C
Operating Temperature	–55°C to +125°C
Maximum Current into and out of any segment	20 mA
Maximum Power Dissipation, any segment	50 mW
Maximum Total power dissipation	600 mW

DC Electrical Characteristics: V_{CC} = 5V, V_{SS} = 0V, V_{BB} = 50V (MIC3830), V_{BB} = 100V (MIC3831), –55°C ≤ T_A ≤ +125°C, unless otherwise noted.

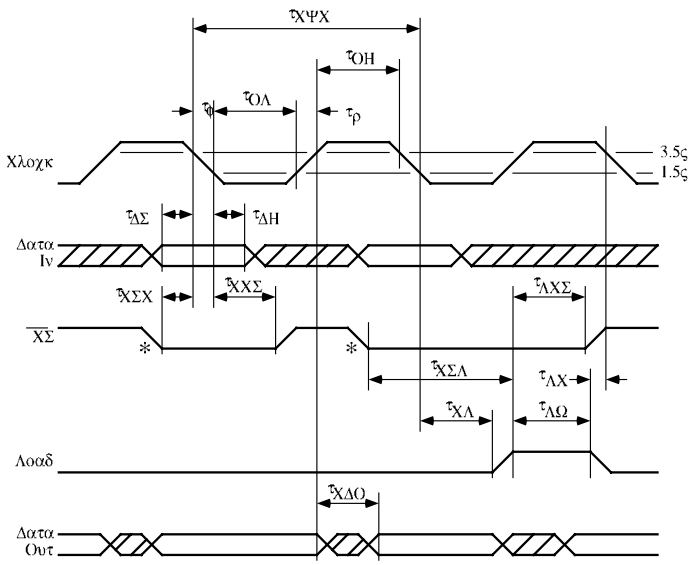
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
POWER SUPPLY						
V_{CC}	Logic Supply Voltage	MIC8030	4.5	5	5.5	V
V_{CC}	Logic Supply Voltage	MIC8031	4.5	5	16.5	V
V_{BB}	Display Supply Voltage	MIC8030	20	35	50	V
V_{BB}	Display Supply Voltage	MIC8031	20	35	100	V
I_{CC}	Supply Current (external oscillator)	Note 1		35	250	µA
	Supply Current (internal oscillator)	Note 1		35	250	
I_{BB}	Display Driver Current	F_{BP} = 100Hz No Loads		7	100	µA
I_{BB}	Display Driver Current	MIC8031, V_{BB} = 100V		20	200	µA
INPUTS (CLK, DATA IN, LOAD, $\overline{CS}$)						
V_{IH}	Input High Level		V_{CC} - 1.5	V_{CC} - 1.8	V_{CC}	V
V_{IL}	Input Low Level		0	2.5	2.0	V
I_L	Input Leakage Current			<1	5	µA
C_I	Input Capacitance	Note 2		5	10	pF
INPUT LCD0						
V_{IH}	LCD0 Input High Level	Externally driven	0.9V_{CC}	V_{CC}	50	V
V_{IL}	LCD0 Input Low Level	Externally driven	–0.5V	0	0.1V_{CC}	V
I_{LCD0}	LCD0 Leakage Current	V_{LCD0} = 15V		2	10	µA
I_{LCD0}	LCD0 Leakage Current	V_{LCD0} = 35V		6	100	µA
I_{LCD0}	LCD0 Leakage Current	V_{LCD0} = 50V			1	mA
CAPACITANCE LOADS (TYPICAL)						
C_{LSEG}	Segment Output	FBP < 100Hz			100	pF
C_{LBP}	Backplane Output	FBP < 100Hz			4000	pF
V_{OAVG}	DC Bias (Average) Any Segment	FBP < 100Hz, Note 2			+25	mV
OUTPUT TO BACKPLANE						
R_{SEG}	Segment Output Impedance	I_L = 100µA		1.4	10	kΩ
R_{BP}	Backplane Output Impedance	I_L = 100µA		170	312	Ω
$R_{DATA\ OUT}$	Data Out Output Impedance	I_L = 100µA		1.8	3	kΩ

Note 1: CMOS input levels. No loads.
Note 2: Guaranteed by design but not tested on a production basis.

AC Electrical Characteristics: V_{CC} = 5V, V_{SS} = 0V, V_{BB} = 50V, –55°C ≤ T_A ≤ +125°C

Symbol	Parameter	Min	Typ	Max	Units
t_{CYC}	Cycle Time	500			ns
t_{OL}, t_{OH}	Clock Pulse Width low/high	250			ns
t_r, t_f	Clock rise/fall			1	µs
t_{DS}	Data In Setup	100			ns
t_{CSC}	$\overline{CS}$ Setup to Clock	100			ns
t_{DH}	Data Hold	10			ns
t_{CCS}	$\overline{CS}$ Hold	220			ns
t_{CL}	Load Pulse Setup	250			ns
t_{LCS}	$\overline{CS}$ Hold (rising load to rising $\overline{CS}$)	200			ns
t_{LW}	Load Pulse Width	300			ns
t_{LC}	Load Pulse Delay (falling load to falling clock)	0			ns
t_{CDO}	Data Out Valid from Clock			220	ns
t_{CSL}	$\overline{CS}$ Setup to LOAD	0			ns
F_{BP}	Backplane Frequency	50	100	2000	Hz

Timing Diagram



* Τηε $\overline{XΣ}$ ηιγη−το−λοω τρανσιτιον ωιλλ γενερατε α χλοχκ πυλσε.

Logic Truth Table

Data In	Clock	Chip Select	Load	$Q_{1(SR)}$	$Q_{N(SR)}$	$Q_{N(DRIVER)}$
X	X	1	X	NC	NC	$Q_{N(L)}$
0	↑	0	0	NC	NC	$Q_{N(L)}$
0	↑	0	1	NC	NC	$Q_{N(L)}$
0	↓	0	0	0	Q_N - 1→Q_N	$Q_{N(L)}$
0	↓	0	1	0	Q_N - 1→Q_N	$Q_{N(SR)}$
1	↑	0	0	NC	NC	$Q_{N(L)}$
1	↑	0	1	NC	NC	$Q_{N(L)}$
1	↓	0	0	1	Q_N - 1→Q_N	$Q_{N(L)}$
1	↓	0	1	1	Q_N - 1→Q_N	$Q_{N(SR)}$

↑ = Rising Edge, ↓ = Falling Edge