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Anti-radioactive design is not implemented in this product.

Dynamic RAM

■ 64M Dynamic RAM (EDO)

Organization (words × bits)	Part number	Access time MAX. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current		Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)			
16M × 4	**μPD4265405**	50 60	4K/64	130 110	0.5	3.3±0.3	• 32-pin SOJ (400 mil) • 32-pin TSOP II (400 mil)	
8M × 8	**μPD4265805**	50 60	4K/64	135 115			• 32-pin SOJ (400 mil) • 32-pin TSOP II (400 mil)	
4M × 16	**μPD4265165**	50 60	4K/64	150 130			• 50-pin TSOP II (400 mil)	Byte read/write

■ 64M Dynamic RAM with Self Refresh (EDO)

Organization (words × bits)	Part number	Access time MAX. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current				Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)	Self refresh (μA)	Long refresh (μA)			
16M × 4	**μPD42S65405**	50 60	4K/128	130 110	0.2	400	500	3.3±0.3	• 32-pin SOJ (400 mil) • 32-pin TSOP II (400 mil)	
8M × 8	**μPD42S65805**	50 60	4K/128	135 115					• 32-pin SOJ (400 mil) • 32-pin TSOP II (400 mil)	
4M × 16	**μPD42S65165**	50 60	4K/128	150 130					• 50-pin TSOP II (400 mil)	Byte read/write

■ 64M Dynamic RAM (Fast Page)

Organization (words × bits)	Part number	Access time MAX. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current		Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)			
16M × 4	**μPD4264400**	50 60	8K/64 *	100 90	0.5	3.3±0.3	• 32-pin SOJ (400 mil) • 32-pin TSOP II (400 mil)	
	μPD4265400	50 60	4K/64	130 110				
8M × 8	**μPD4264800**	50 60	8K/64 *	105 95			• 32-pin SOJ (400 mil) • 32-pin TSOP II (400 mil)	
	μPD4265800	50 60	4K/64	135 115				

*: CBR/Hidden Refresh: 4K/64

Dynamic RAM

■ 64M Synchronous DRAM – PC100 Compliant –

Organization (words × bits × bank)	Part number	Cycle time MIN. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current			Interface level	Supply voltage (V)	Package
				Active (mA) (BL = 1)	Standby (mA)	Self refresh (mA)			
4M × 4 × 4	**μPD4564441**	8 10 10	4K/64	80 80 70	0.5	1	LVTTL	3.3±0.3	• 54-pin TSOP II (400 mil)
	μPD4564441-L					0.4			
2M × 8 × 4	**μPD4564841**	8 10 10		85 85 75		1			
	μPD4564841-L					0.4			
1K × 16 × 4	**μPD4564163**	8 10 10		115 115 90		1			
	μPD4564163-L					0.4			

BL: Burst Length

■ 64M Synchronous DRAM (× 32) – PC100 Compliant –

Organization (words × bits × bank)	Part number	Cycle time MIN. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current			Interface level	Supply voltage (V)	Package
				Active (mA) (BL = 1)	Standby (mA)	Self refresh (mA)			
512K × 32 × 4	**μPD4564323**	8 10	4K/64	180 160	0.5	1	LVTTL	3.3±0.3	• 86-pin TSOP II (400 mil)

BL: Burst Length

■ 16M Synchronous DRAM (Rev. A)

Organization (words × bits × bank)	Part number	Cycle time MIN. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current			Interface level	Supply voltage (V)	Package
				Active (mA) (BL = 1)	Standby (mA)	Self refresh (mA)			
2M × 4 × 2	**μPD4516421A**	8 10 12	2K/32	150 120 100	2	2	LVTTL	3.3±0.3	• 44-pin TSOP II (400 mil)
	μPD4516421A-L					0.25			
1M × 8 × 2	**μPD4516821A**			160 130 110		2			
	μPD4516821A-L					0.25			

BL: Burst Length

■ 16M Synchronous DRAM (Rev. B, P) – PC100 Compliant –

Organization (words × bits × bank)	Part number	Cycle time MIN. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current			Interface level	Supply voltage (V)	Package
				Active (mA) (BL = 1)	Standby (mA)	Self refresh (mA)			
2M × 4 × 2	**μPD4516421A**	8 10 10	2K/32	110 90 90	2	1	LVTTL	3.3±0.3	• 44-pin TSOP II (400 mil)
	μPD4516421A-L					0.25			
1M × 8 × 2	**μPD4516821A**	8 10 10		120 100 100		1			
	μPD4516821A-L					0.25			
512K × 16 × 2	**μPD4516161A**	8 10 10		125 105 105		1			• 50-pin TSOP II (400 mil)
	μPD4516161A-L					0.25			

BL: Burst Length

Dynamic RAM

■ 4M Synchronous DRAM

Organization (words × bits × bank)	Part number	Cycle time MIN. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current			Interface level	Supply voltage (V)	Package
				Active (mA) (BL = 1)	Standby (mA)	Self refresh (mA)			
128K × 16 × 2	**μPD4504161**	10 12	1K/16	140 120	2	2	LVTTL	3.3±0.3	• 50-pin TSOP II (400 mil)

BL: Burst Length

■ 2M Synchronous DRAM

Organization (words × bits × bank)	Part number	Cycle time MIN. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current			Interface level	Supply voltage (V)	Package
				Active (mA) (BL = 1)	Standby (mA)	Self refresh (mA)			
64K × 16 × 2	**μPD4502161**	10 12	512K/8	140 120	2	2	LVTTL	3.3±0.3	• 50-pin TSOP II (400 mil)

BL: Burst Length

■ Rambus™ DRAM

Density (bits)	Organization (words × bits)	Part number	Type	Class	Clock cycle time MIN. (ns)	Supply voltage (V)	Package
18M	2M × 9	**μPD488172**	Concurrent	A60 A53	3.33 (600 MHz) 3.75 (533 MHz)	3.15 to 3.45	• 36/32-pin SHP

Dynamic RAM Module

■ 144-pin 8 Byte SO DIMM (SO DIMM: Small Outline Dual In-line Memory Module)

Organization (words × bits)	Bank	Part number	Access time MAX. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current		Supply voltage (V)	Package	Remarks
					Active (mA)	Standby (mA)			
8M × 64	2	**MC-42S8LFF64S**	50 60	4K/128	1080 920	1.6	3.3±0.3	• 144-pin SOD Socket type (Gold plated)	EDO Self refresh
		MC-42S8LFG64S	50 60	4K/128	648 568	1.6			
4M × 64	1	**MC-42S4LFG64S**	50 60	4K/128	600 520	0.8			

■ 168-pin 8 Byte DIMM (DIMM: Dual In-line Memory Module), Buffered type

Organization (words × bits)	Part number	Access time MAX. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current		Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)			
16M × 72 (ECC)	**MC-4216LFC72**	50 60	4K/64	2350 1990	70	3.3±0.3	• 168-pin DIMM Socket type (Gold plated)	EDO
8M × 72 (ECC)	**MC-428LFC72**	50 60	4K/64	1225 1045	50			
4M × 72 (ECC)	**MC-424LFC72**	50 60	4K/64	850 750	50			

Dynamic RAM Module

■ 200-pin Synchronous DRAM DIMM Registered type

Organization (words × bits)	Part number	Bank Org.	Clock frequency (MHz)	Refresh cycle (cycles/ms)	Maximum supply current		Supply voltage (V)	Package	Remarks
					Active (mA)	Standby (mA)			
16M × 72 (ECC)	**MC-4516DA72**	1	100 83	4K/64	1920	36	3.3+0.3/ –0.15	• 200-pin DIMM Socket type (Gold plated)	
16M × 72 (ECC)	**MC-4516DC72**	2			1470	36			
8M × 72 (ECC)	**MC-458DA72**	1			1245	18			

■ 168-pin Synchronous DRAM DIMM, Unbuffered type

Organization (words × bits)	Part number	Bank Org.	Clock frequency (MHz)	Refresh cycle (cycles/ms)	Maximum supply current		Supply voltage (V)	Package	Remarks
					Active (mA)	Standby (mA)			
16M × 64	**MC-4516CC646**	2	125	4K/64	1200	8	3.3±0.3	• 168-pin DIMM Socket type (Gold plated)	PC100 Compliant
			100		1040				
	MC-4516CC645		100		1040				
16M × 72 (ECC)	**MC-4516CC726**	2	125	4K/64	1350	9			PC100 Compliant
			100		1170				
	MC-4516CC725		100		1170				
8M × 64	**MC-458CB646**	1	125	4K/64	1000	4			PC100 Compliant
			100		840				
	MC-458CB645		100		840				
8M × 72 (ECC)	**MC-458CA726**	1	125	4K/64	1125	4.5			PC100 Compliant
			100		945				
	MC-458CA725		100		945				
4M × 64	**MC-454CB646**	1	125	4K/64	780	2			PC100 Compliant
			100		660				
	MC-454CB645		100		660				
4M × 72 (ECC)	**MC-454AC726**	2	125	2K/32	1332	36			PC100 Compliant
			100		1152				
	MC-454AC725		125		1692				
			100		1422				
			83		1242				

■ 168-pin Synchronous DRAM DIMM, Registered type

Organization (words × bits)	Part number	Bank Org.	Clock frequency (MHz)	Refresh cycle (cycles/ms)	Maximum supply current		Supply voltage (V)	Package	Remarks
					Active (mA)	Standby (mA)			
16M × 72 (ECC)	**MC-4516DA726**	1	100 83	4K/64	2280 2100	36	3.3±0.3	• 168-pin DIMM Socket type (Gold plated)	PC100 Compliant
8M × 72 (ECC)	**MC-458DA726**	1			975 930	18			

Dynamic RAM Module

■ 144-pin Synchronous DRAM SODIMM, Unbuffered type

Organization (words × bits)	Part number	Bank Org.	Clock frequency (MHz)	Refresh cycle (cycles/ms)	Maximum supply current		Supply voltage (V)	Package	Remarks
					Active (mA)	Standby (mA)			
8M × 64	**MC-458CB64S**	1	125 100	4K/64	1000 840	4	3.3±0.3	• 144-pin SODIMM Socket type (Gold plated)	
4M × 64	**MC-454CB64S**	1	125 100		780 660	2			

Static RAM

■ Low Power Static RAM 5 V Operation (4.5 to 5.5 V)

Density (bits)	Organization (words × bits)	Part number	Access time MAX. (ns)	Maximum supply current			Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (μA)	Data retention (μA)			
1M	128K × 8	**μPD431000A** with $\overline{CE1}$, CE2, $\overline{OE}$	70	70	100	50	5.0±0.5	• 32-pin DIP (600 mil) • 32-pin SOP (525 mil) • 32-pin TSOP I (8 × 20 mm) • 32-pin TSOP I (8 × 13.4 mm)	L version
			85		20	10			LL version
256K	32K × 8	**μPD43256B** with $\overline{CS}$, $\overline{OE}$	70	45	50	20		• 28-pin DIP (600 mil) • 28-pin SOP (450 mil) • 28-pin TSOP I (8 × 13.4 mm)	L version
			85		15	7			LL version
		μPD43257B with $\overline{CE1}$, CE2	70	45	50	20		• 28-pin DIP (600 mil) • 28-pin SOP (450 mil)	L version
			85		15	7			LL version

■ Low Power Static RAM Low Voltage (2.2 to 5.5 V) Operation

Density (bits)	Organization (words × bits)	Part number	Access time MAX. (ns)	Maximum supply current			Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (μA)	Data retention (μA)			
256K	32K × 8	**μPD43256B-C25**	250	20*	10*	7	2.2 to 5.5	• 28-pin TSOP I (8 × 13.4 mm)	*: $V_{CC} \leqq 3.3$ V

■ Low Power Static RAM Low Voltage (2.7 to 5.5 V) Operation

Density (bits)	Organization (words × bits)	Part number	Access time MAX. (ns)	Maximum supply current			Supply voltage (V)	Package
				Active (mA)	Standby (μA)	Data retention (μA)		
1M	128K × 8	**μPD431000A-B××** with $\overline{CE1}$, CE2, $\overline{OE}$	100	30	11	10	3.0±0.3	• 32-pin SOP (525 mil) • 32-pin TSOP I (8 × 20 mm) • 32-pin TSOP I (8 × 13.4 mm)
			120	70	20		3.3 < V_{CC} < 4.5	
			150					
			70				5.0±0.5	
256K	32K × 8	**μPD43256B-B××** with $\overline{CS}$, $\overline{OE}$	100	20	10	7	3.0±0.3	• 28-pin SOP (450 mil) • 28-pin TSOP I (8 × 13.4 mm)
			120	45	15		3.3 < V_{CC} < 4.5	
			150					
			85				5.0±0.5	

■ Low Power Static RAM Low Voltage (3.0 to 5.5 V) Operation

Density (bits)	Organization (words × bits)	Part number	Access time MAX. (ns)	Maximum supply current			Supply voltage (V)	Package
				Active (mA)	Standby (μA)	Data retention (μA)		
1M	128K × 8	**μPD431000A-A××**	100	35	13	10	3.3±0.3	• 32-pin SOP (525 mil)
			120	70	20		3.6 < V_{CC} < 4.5	• 32-pin TSOP I (8 × 20 mm)
			70				5.0±0.5	• 32-pin TSOP I (8 × 13.4 mm)
256K	32K × 8	**μPD43256B-A××**	85	45	15	7	3.3±0.3	• 28-pin SOP (450 mil)
			100				3.6 < V_{CC} < 4.5	• 28-pin TSOP I (8 × 13.4 mm)
			120					
			85				5.0±0.5	

Static RAM

■ Low Power Static RAM Extended Temperature (–25 to +85°C) Operation

Density (bits)	Organization (words × bits)	Part number	Access time MAX. (ns)	Maximum supply current			Supply voltage (V)	Package
				Active (mA)	Standby (μA)	Data retention (μA)		
2M	256K × 8	**μPD442000L-C××X**	150	35	2	2	2.2 ≤ V_{CC} ≤ 3.6	• 32-pin TSOP I (8 × 13.4 mm)
		μPD442000L-B××X	70★ 85 100	35	2		2.7 ≤ V_{CC} ≤ 3.6	
1M	128K × 8	**μPD431000A-××X**	70 85 100	70	50	20	5.0±0.5	• 32-pin TSOP I (8 × 20 mm) • 32-pin TSOP I (8 × 13.4 mm)
		μPD431000A-B××X	100 120 150	30	22		3.0±0.3	
				70	50		3.3 < V_{CC} < 4.5	
			70				5.0±0.5	
		μPD431000A-A××X	100 120 150	35	26		3.3±0.3	
				70	50		3.3 < V_{CC} < 4.5	
			70				5.0±0.5	
256K	32K × 8	**μPD43256B-××X**	70 85	45	50	20	5.0±0.5	• 28-pin TSOP I (8 × 13.4 mm)
			100	40				
		μPD43256B-B××X	120 150	25	25		3.0±0.3	
				40	50		3.3 < V_{CC} < 4.5	
			100				5.0±0.5	
		μPD43256B-A××X	100	40	50		3.3±0.3	
			120				3.6 < V_{CC} < 4.5	
			100				5.0±0.5	

★: Under development

Static RAM

■ Fast Static RAM 5 V Operation (4.5 to 5.5 V)

Density (bits)	Organization (words × bits)	Part number	Access time MAX. (ns)	Maximum supply current			Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)	Power down (mA)			
4M	4M × 1	**μPD434001**	20 25	140 130	10	–	5.0±0.5	• 32-pin SOJ (400 mil)	
		μPD434001A	15 17 20	170 160 150					
	1M × 4	**μPD434004**	20 25	150 140					
		μPD434004A	15 17 20	170 160 150					
	512K × 8	**μPD434008**	20 25	190 170				• 36-pin SOJ (400 mil)	
		μPD434008A	12 15 17 20	200 190 180 170					
	256K × 16	**μPD434016A**	12 15 17 20	230 220 210 200				• 44-pin SOJ (400 mil) • 44-pin TSOP II (400 mil)	
1M	128K × 8	**μPD431008**	15 17 20	160 150 140	10	–	5.0±0.5	• 32-pin SOJ (400 mil)	
	128K × 9	**μPD431009**	15 17 20	160 150 140				• 36-pin SOJ (400 mil)	
	64K × 16	**μPD431016**	15 17 20	240 230 220				• 44-pin SOJ (400 mil)	
	64K × 18	**μPD431018**	15 17 20	240 230 220				• 44-pin SOJ (400 mil)	

■ Fast Static RAM Low Voltage (3.0 to 3.6 V) Operation

Density (bits)	Organization (words × bits)	Part number	Access time MAX. (ns)	Maximum supply current			Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)	Power down (mA)			
4M	4M × 1	**μPD434001AL**	15 17 20	150 140 130	5	–	3.3±0.3	• 32-pin SOJ (400 mil) • 32-pin TSOP II (400 mil)	
	1M × 4	**μPD434004AL**	15 17 20	150 140 130				• 32-pin SOJ (400 mil)	
	512K × 8	**μPD434008AL**	15 17 20	170 160 150				• 36-pin SOJ (400 mil)	
	256K × 16	**μPD434016AL**	15 17 20	200 190 180				• 44-pin SOJ (400 mil) • 44-pin TSOP II (400 mil)	

Static RAM

■ Synchronous Static RAM

Density (bits)	Organization (words × bits)	Part number	Clock frequency (MHz)	Maximum supply current			Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)	Power down (mA)			
2M	64K × 32	**μPD432232L**	83 (7 ns) 66 (8 ns)	180	2	2	$3.3^{+0.3}_{-0.2}$ I/O: 2.5 V/3.3 V	• 100-pin TQFP	Pipelined operation
1M	32K × 32	**μPD431232AL**	83 (7 ns) 66 (8 ns) 60 (10 ns)	130	2	1	$3.3^{+0.3}_{-0.2}$ I/O: 3.3 V		Pipelined operation
		μPD431532L	100 (8.5 ns) 100 (9 ns) 83 (10 ns) 66 (12 ns)	200	5	5	3.3±0.165 I/O: 2.5 V/3.3 V		Flow through operation
		μPD431632L	150 (4.6 ns) 133 (5 ns)	200	20	20	3.3±0.165 I/O: 2.5 V/3.3 V		Pipelined operation
	32K × 36	**μPD431536L**	100 (8.5 ns) 100 (9 ns) 83 (10 ns) 66 (12 ns)	200	5	5	$3.3^{+0.3}_{-0.2}$ I/O: 2.5 V/3.3 V		Flow through operation
		μPD431636L	150 (4.6 ns) 133 (5 ns)	200	20	20	$3.3^{+0.3}_{-0.2}$ I/O: 2.5 V/3.3 V		Pipelined operation

■ BiCMOS Synchronous Static RAM

Density (bits)	Organization (words × bits)	Part number	Clock frequency (MHz)	Maximum supply current			Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)	Power down (mA)			
4M	256K × 18	**μPD464318L**	200 (2.6 ns) 167 (3 ns) 154 (3.5 ns)	600	–	–	3.3±0.15	• 119-pin BGA	Single clock RR mode
		μPD464518L	125 (8 ns)	450	150				Single clock RL mode
	128K × 36	**μPD464336L**	200 (2.6 ns) 167 (3 ns) 154 (3.5 ns)	700	–				Single clock RR mode
		μPD464536L	125 (8 ns)	550	150				Single clock RL mode

Mask ROM

■ Mask ROM

Density (bits)	Organization (words × bits)	Part number	Access time MAX. (ns)	Maximum supply current		Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (μA)			
64M	8M × 8 or 4M × 16 (selectable)	**μPD23C64000**	120	70	100	5.0±0.5	• 44-pin SOP (600 mil) • 48-pin TSOP I (12 × 18 mm)	
	4M × 16	**μPD23C64020**	120	70	–		• 42-pin DIP (600 mil)	
32M	4M × 8 or 2M × 16 (selectable)	**μPD23C32000A**	120	70	100		• 44-pin SOP (600 mil) • 48-pin TSOP I (12 × 18 mm) • 44-pin TSOP II (400 mil)	
	2M × 16	**μPD23C32020A**					• 42-pin DIP (600 mil)	
24M	3M × 8 or 1.5M × 16 (selectable)	**μPD23C24000**	120	70	100		• 44-pin SOP (600 mil) • 48-pin TSOP I (12 × 18 mm) • 44-pin TSOP II (400 mil)	
	1.5M × 16	**μPD23C24020**					• 42-pin DIP (600 mil)	
16M	2M × 8 or 1M × 16 (selectable)	**μPD23C16000W**	120	70	100		• 42-pin DIP (600 mil) • 44-pin SOP (600 mil) • 48-pin TSOP I (12 × 18 mm) • 44-pin TSOP II (400 mil)	
		μPD23C16040A	120/35	100				with page access read mode
8M	1M × 8 or 512K × 16 (selectable)	**μPD23C8000X**	120	50	100		• 42-pin DIP (600 mil) • 44-pin SOP (600 mil) • 48-pin TSOP I (12 × 18 mm) • 44-pin TSOP II (400 mil)	
	1M × 8	**μPD23C8001EJ**					• 32-pin DIP (600 mil) • 32-pin SOP (525 mil)	
4M	512K × 8	**μPD23C4001EJ**	120	35	100		• 32-pin DIP (600 mil) • 32-pin SOP (525 mil) • 40-pin TSOP I (10 × 20 mm)	∗: T_A = –20 to 85°C
			300 330 ∗	15 20	25 150	3.3±0.3		
			350 380 ∗	10 15	20 100	3.0±0.3		

Mask ROM

■ Mask ROM (Low Voltage Operation)

Density (bits)	Organization (words × bits)	Part number	Access time MAX. (ns)	Maximum supply current		Supply voltage (V)	Package	Remarks
				Active (mA)	Standby (mA)			
64M	8M × 8 or 4M × 16 (selectable)	μPD23C64000AL★	100	45	30	3.3±0.3	• 44-pin SOP (600 mil) • 48-pin TSOP I (12 × 18 mm)	
			120	40	30	3.0±0.3		
		μPD23C64000L	120	45	30	3.3±0.3		
			140	40	30	3.0±0.3		
		μPD23C64040AL★	120/40	100	30	3.3±0.3		with page access read mode
			150/50	80	30	3.0±0.3		
		μPD23C64040L	120/40	100	30	3.3±0.3		
			150/50	80	30	3.0±0.3		
32M	4M × 8 or 2M × 16 (selectable)	μPD23C32000L	120	40	30	3.3±0.3	• 44-pin SOP (600 mil) • 48-pin TSOP I (12 × 18 mm) • 48-pin TSOP II (400 mil)	
			150	35	30	3.0±0.3		
		μPD23C32040L	140/40	60	30	3.3±0.3		with page access read mode
	2M × 16 or 1M × 32 (selectable)	μPD23C32082L	100/30	80	30	3.3±0.3	• 70-pin SSOP (500 mil) • 70-pin TSOP II (400 mil)	
16M	2M × 8 or 1M × 16 (selectable)	μPD2316000L	120	35	30	3.3±0.3	• 42-pin DIP (600 mil) • 44-pin SOP (600 mil) • 48-pin TSOP I (12 × 18 mm) • 44-pin TSOP II (400 mil)	
			140	30	30	3.0±0.3		
	2M × 8 or 1M × 16 (selectable)	μPD23C16000LW	170	25	25	3.3±0.3		
			200	20	20	3.0±0.3		
8M	1M × 8 or 512K × 16 (selectable)	μPD23C8000L	120	35	30	3.0±0.3		
			140	30	30	3.0±0.3		
	1M × 8 or 512K × 16 (selectable)	μPD23C8000LX	170	25	25	3.3±0.3		
			200	20	20	3.0±0.3		

★: Under development

COMBO Memory

■ COMBO Memory

Density (bits)	Organization (words × bits)	Part number	Access time MAX. (ns)	Maximum supply current		Supply voltage (V)	Package	Remarks
				Active (mA) ROM/RAM	Standby (μA)			
ROM: 2M RAM: 1M	ROM: 256K × 8 RAM: 128K × 8	**μPD26401**	500	3.5/3.5	5	1.8 to 2.2	• 32-pin TSOP I (8 × 13.4 mm)	
			375	5.5/5.5	7.5	2.2 to 2.7		
			250	7.5/7.5	10	2.7 to 3.3		
		μPD26411	500	4.0/4.0	5	1.8 to 2.2	• 32-pin TSOP I (8 × 20 mm)	
			375	6.0/6.0	7.5	2.2 to 2.7		
			250	10/10	10	2.7 to 3.3		

Flash MEMORY

■ Flash MEMORY

Density (bits)	Organization (words × bits)	Part number	Access time MAX. (ns)	Maximum supply current		Supply voltage		Package	Remarks
				Active (mA)	Standby (mA)	V_{CC} (V)	V_{PP} (V)		
8M	1024K × 8	**μPD29F008L**	120 150	35	5	2.7 to 3.6	–	• 40-pin TSOP I (10 × 20 mm)	Under development
	1024K × 8 or 512K × 16 (selectable)	**μPD29F800L**	120 150	35		2.7 to 3.6		• 44-pin SOP (600 mil) • 48-pin TSOP I (12 × 20 mm)	

MCP (Flash Memory + SRAM)

■ MCP (Flash Memory + SRAM)

Density (bits)	Organization (words × bits)	Part number	Boot code sector architecture	Access time MAX. (ns)	Supply voltage (V)	Multi-chip package (MCP)	Remarks
Flash: 16M SRAM: 2M	Flash: 1M × 16 SRAM: 256K × 8	**MC-22102**	Top sector	100	2.7 to 3.6	• 48-pin BGA (10 × 14 mm)	Under development
		MC-22103	Bottom sector				
Flash: 8M SRAM: 2M	Flash: 1M × 8 SRAM: 256K × 8	**MC-22000**	Top sector			• 48-pin BGA (10 × 11 mm)	
		MC-22001	Bottom sector				
Flash: 8M SRAM: 2M	Flash: 512K × 16 SRAM: 256K × 8	**MC-22002**	Top sector				
		MC-22003	Bottom sector				
Flash: 8M SRAM: 1M	Flash: 1M × 8 SRAM: 128K × 8	**MC-22004**	Top sector				
		MC-22005	Bottom sector				

Other

■ Synchronous Graphics RAM

Density (bits)	Organization	Part number	Cycle time MIN. (ns)	Refresh cycle (cycles/ ms)	Maximum supply current (mA)			Interface	Supply voltage (V)	Package	Function
					Active Normal/ Burst (C.L=3)	Standby power down mode	Self refresh				
16M	256K words × 2 banks × 32 bits	**μPD4811650**	8 (125 MHz) 10 (100 MHz) 12 (83 MHz)	2K/32	220/375 205/300 180/250	3	2	LVTTL	3.3±0.3	• 100-pin Thin-QFP (14 × 20 mm)	Sychronous Interface Write-per-bit (Old Mask) 8 column Block Write
		μPD4811652	8 (125 MHz) 10 (100 MHz)		220/375 205/300			LVTTL SSTL_3			
8M	128K words × 2 banks × 32 bits	**μPD481850**	10 (100 MHz) 12 (83 MHz)	1K/16	105/200 90/170	6 6	6 6	LVTTL		• 100-pin QFP (14 × 20 mm)	

■ Field/Line Buffer

Density (bits)	Organization (words × bits)	Part number	Read/Write cycle time MIN. (ns)	Data hold period (ms)	Maximum supply current active (mA)	Supply voltage (V)	Package	Remarks
2M	256 × 8	**μPD42280**	30/30 60/60	–	90 60	5.0±0.5	• 28-pin SOP • 28-pin ZIP	Field buffer FIFO structure
80K	10096 × 8 5048 × 16	**μPD485506**	25/25 35/35	–	140	5.0±0.5	• 44-pin TSOP II	FAX, PPC Line buffer FIFO structure
40K	5048 × 8	**μPD485505**	25/25 35/35	–	80		• 24-pin SOP	

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