High-frequency switching IC powers portable telephone

Switched-capacitor voltage converters provide convenient sources of negative voltage for battery-operated systems, but the switching frequency poses a problem for portable telephones and radios. Appearing as sidebands about the carrier frequency, the switching energy is difficult to filter unless its frequency is relatively high.

IC1 in **Figure 1**, for example, is a switched-capacitor voltage converter that normally operates at 4kHz. By connecting its BOOST pin to V+, you can raise this frequency to 32kHz or so, moving the interference above the frequency band of interest for most audio applications. For radio applications, the switching frequencies must be even higher.

IC1's OSC pin lets you override the internal oscillator with external frequencies as high as 500kHz. The arrangement shown drives the IC with a 375kHz square wave of 50% duty cycle. HC logic gates provide the required rail-to-rail amplitude, and an internal divide-by-two stage lowers the frequency of this drive signal before applying it to the internal switches. The resulting sidebands, about 190kHz from the carrier, are easily removed by filtering.

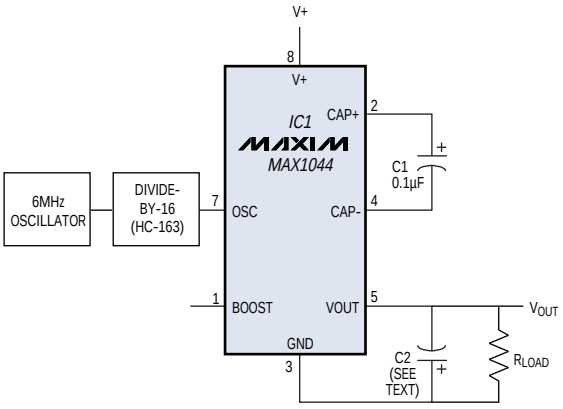

Figure 1. Driving this switching converter at an unusually high rate (375kHz) produces high-frequency switching noise that is easy to filter.

The following data illustrates the effects of load resistance and output capacitance (C2) on output voltage, ripple amplitude, and supply current (for IC1):

OUTPUT CAPACITANCE	LOAD RESISTANCE	1 mΩ	100 kΩ	10 kΩ	1 kΩ
C2 = 0.1µF	$-V_{OUT}$ (V)	4.95	4.92	4.88	4.56
	I+ (mA)	2.29	2.34	2.78	6.60
	M_{RIPPLE} (mV_{p-p})	60	60	70	200
C2 = 1µF	$-V_{OUT}$ (V)	4.93	4.92	4.88	4.61
	I+ (mA)	2.43	2.46	2.90	6.77
	M_{RIPPLE} (mV_{p-p})*	20	20	20	60
C2 = 10µF	$-V_{OUT}$ (V)	4.94	4.93	4.90	4.62
	I+ (mA)	2.37	2.41	2.85	6.63
	M_{RIPPLE} (mV_{p-p})**	10	10	10	30

* Plus 100mV, 0.1µs spikes
** Plus 60mV, 0.1µs spikes

Larger output capacitors obviously improve the load regulation and ripple voltage. Adding a 0.1µF ceramic capacitor in parallel with C2 can lower the fast spike amplitudes (for C2 values of 1µF and 10µF) to about 20mV. If practical, adding a linear regulator at the output can further reduce the variation of output voltage with load current.

When IC1 generates the negative supply for a data converter, you can minimize the effect of switching noise by synchronizing IC1 to the system clock or the data converter's clock. As an alternative, you can turn off the chip during each data conversion (using the BOOST pin), provided that C2 can support the negative output voltage during those intervals.

(Circle 3)