DESIGN SHOWCASE

μP-Supervisor Chip Controls Programmable Filter

Certain dual-section filter ICs have a common 7-bit port for programming the two cutoff frequencies (f_C). If both sections require the same f_C , you can strap an appropriate code to the port pins, but other applications require a different f_C for each section. In such cases, a microprocessor is the obvious tool for sequentially programming the two filter sections, but lacking a μP , you can do the job with the circuit of **Figure 1**.

 IC_2 is a continuous, dual-lowpass filter containing identical 2nd-order sections A and B. To program desired f_C values, obtain corresponding codes from the data sheet and connect each pin of A0-A6 and B0-B6 to 5V ("1") or GND ("0") accordingly. (The latches internal to inputs D0-D6 remain "transparent" because inputs \overline{WR} and \overline{CS} are wired low.)

Latch IC₃ also remains transparent because pin 11 is wired high. The latch outputs (1Q-7Q) are three-stated when the Output Control $(\overline{OC}, \text{ pin } 1)$ is driven high. When \overline{OC} is high, therefore, A0-A6 data drives the filter port (D0-D6). When \overline{OC} is low, B0-B6 data appears at the latch outputs and overrides A0-A6.

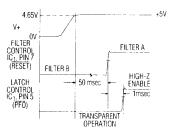


Figure 2. Timing relationships for the Figure 1 circuit.

The μP -supervisory chip IC_1 , though normally used to monitor supply voltage and software execution in a μP system, generates directly usable signals for controlling IC_2 and IC_3 : \overline{RESET} (pin 7), which remains low for 50msec after power-up, directs the input port of IC_2 first to filter section A, then to section B. \overline{PFO} (Power Fail Output, pin 5), which goes high a few milliseconds after \overline{RESET} , provides a properly timed control signal for three-stating the latch outputs of IC_3 (**Figure 2**).

The circuit as shown requires $\pm 5V$ supplies. To operate on $\pm 2.5V$ or on 5V alone, connect IC₁'s GND pin to the lower supply rail and drive IC₂'s pin 12 through a resistive divider (see the MAX270 data sheet, Figure 3).

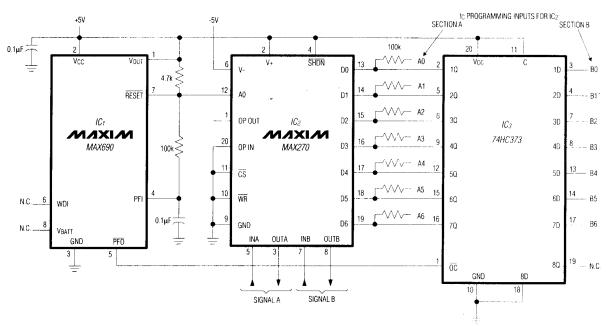


Figure 1. A µP-supervisory chip (IC1) directs the sequential loading of fC data into the dual, programmable lowpass filter IC2. The circuit reloads this fC data following each power-up.