DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4557B
LSI
1-to-64 bit variable length shift register

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

1-to-64 BIT VARIABLE LENGTH SHIFT REGISTER

The HEF4557B is a static clocked serial shift register whose length may be programmed to be any number of bits between 1 and 64. The number of bits selected is equal to the sum of the subscripts of the enabled length control inputs (L_1, L_2, L_4, L_8, L_{16} and L_{32}) plus one. Serial data may be selected from the D_A or D_B data inputs with the $A/\overline{B}$ select input. This feature is useful for recirculation purposes. Information on D_A or D_B is shifted into the first register position and all the data in the register is shifted one position to the right on the LOW to HIGH transition of CP_0 while $\overline{CP}_1$ is LOW or on the HIGH to LOW transition of $\overline{CP}_1$ while CP_0 is HIGH. A HIGH on master reset (MR) resets the register and forces O to LOW and $\overline{O}$ to HIGH, independent of the other inputs.

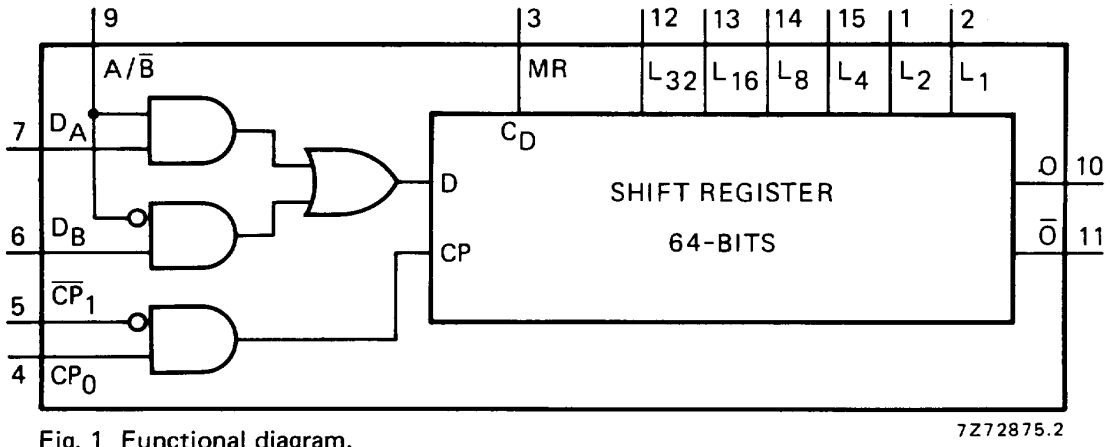

Fig. 1 Functional diagram.

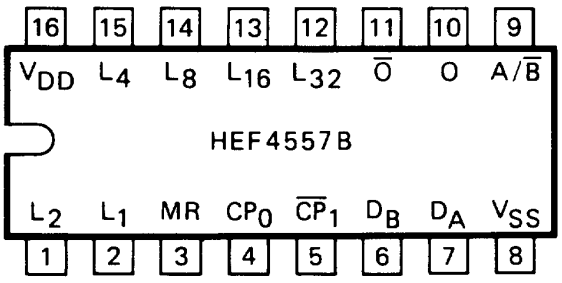

Fig. 2 Pinning diagram.

PINNING

D_A, D_B	data inputs
$A/\overline{B}$	select data input
CP_0	clock input
$\overline{CP}_1$	clock enable input
MR	asynchronous master reset
L_1 to L_{32}	bit-length control inputs
O, $\overline{O}$	buffered outputs

HEF4557BP(N): 16-lead DIL; plastic (SOT38-1)
HEF4557BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4557BT(D): 16-lead SO; plastic (SOT109-1)
( ): Package Designator North America

FAMILY DATA

I_{DD} LIMITS category LSI

see Family Specifications

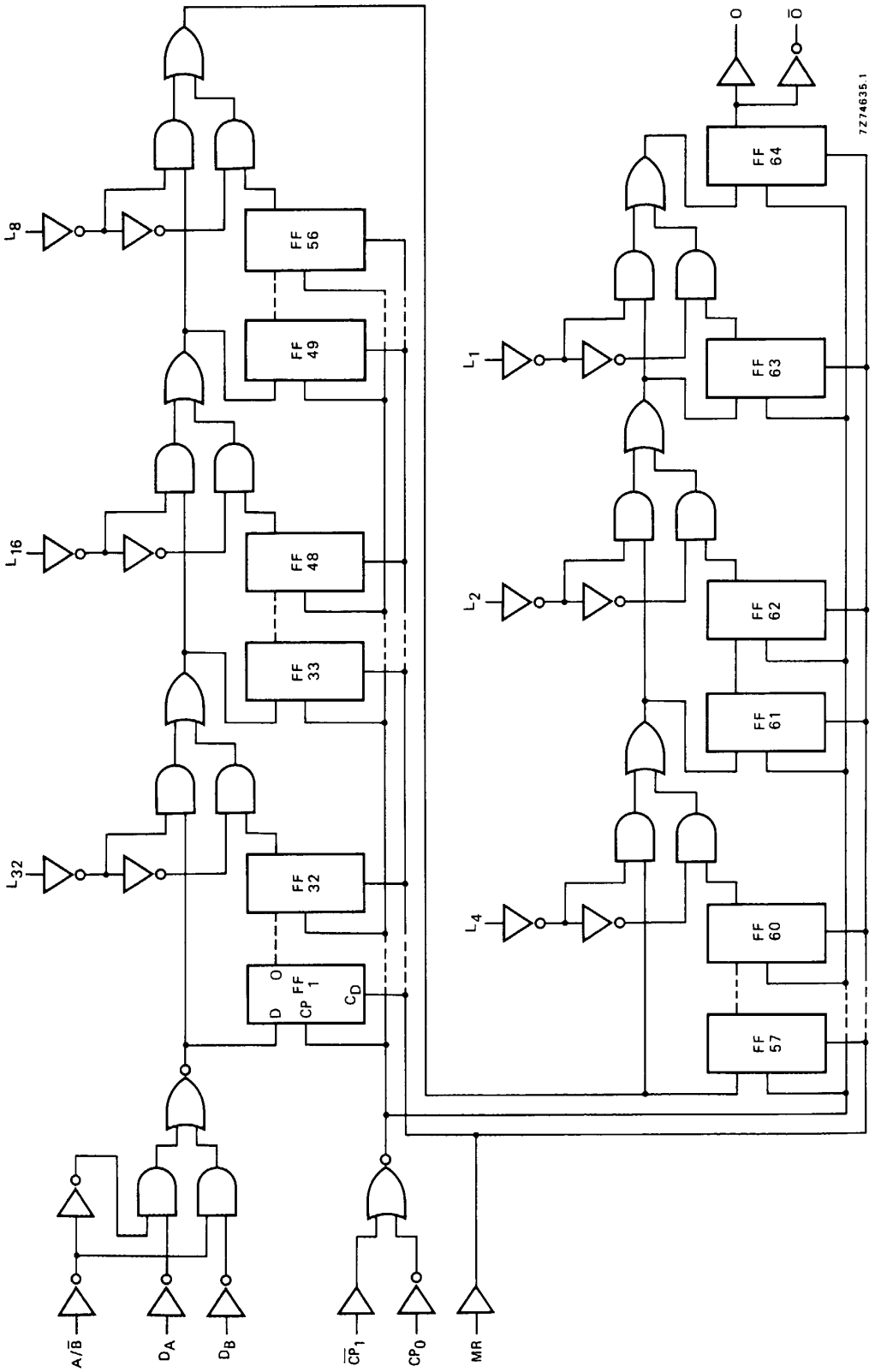

Fig. 3 Logic diagram.

FUNCTION TABLE

inputs						output
MR	A/$\overline{B}$	D_A	D_B	CP_0	$\overline{CP}_1$	O *
L	L	D_1	D_2	∫	L	D_2
L	H	D_1	D_2	∫	L	D_1
L	L	D_1	D_2	H	⌞	D_2
L	H	D_1	D_2	H	⌞	D_1
H	X	X	X	X	X	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition
⌞ = negative-going transition
D_n = either HIGH or LOW

* The moment D_n appears at O depends on the bit-length shown in the table below.

BIT-LENGTH SELECT FUNCTION TABLE

L_{32}	L_{16}	L_8	L_4	L_2	L_1	register length
L	L	L	L	L	L	1-bit
L	L	L	L	L	H	2-bits
L	L	L	L	H	L	3-bits
L	L	L	L	H	H	4-bits
L	L	L	H	L	L	5-bits
L	L	L	H	L	H	6-bits
L	L	L	H	H	L	7-bits
L	L	L	H	H	H	8-bits
↓	↓	↓	↓	↓	↓	↓
L	H	H	H	H	H	32-bits
H	L	L	L	L	L	33-bits
H	L	L	L	L	H	34-bits
↓	↓	↓	↓	↓	↓	↓
H	H	H	H	L	L	61-bits
H	H	H	H	L	H	62-bits
H	H	H	H	H	L	63-bits
H	H	H	H	H	H	64-bits

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$3\,500\,f_i + \Sigma(f_oC_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_oC_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$15\,000\,f_i + \Sigma(f_oC_L) \times V_{DD}^2$	
	15	$37\,000\,f_i + \Sigma(f_oC_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
CP_0, $\overline{CP_1}$ → O, $\overline{O}$	5		240	480	ns	213 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	90	180	ns	79 ns + (0,23 ns/pF) C_L
	15		65	130	ns	57 ns + (0,16 ns/pF) C_L
	5		240	480	ns	213 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	90	180	ns	79 ns + (0,23 ns/pF) C_L
	15		65	130	ns	57 ns + (0,16 ns/pF) C_L
MR → O	5		170	340	ns	143 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	80	160	ns	69 ns + (0,23 ns/pF) C_L
	15		60	120	ns	52 ns + (0,16 ns/pF) C_L
MR → $\overline{O}$	5		140	280	ns	113 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	70	140	ns	59 ns + (0,23 ns/pF) C_L
	15		55	110	ns	47 ns + (0,16 ns/pF) C_L
Output transition times	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

Interpolation table (see note next page)

length control inputs						minimum number of bits selected	set-up, hold, recovery times
L_1	L_2	L_4	L_8	L_{16}	L_{32}		
L	L	L	L	L	L	1	specified
H	L	L	L	L	L	2	⋮
X	H	L	L	L	L	3	⋮
X	X	H	L	L	L	5	six equal steps
X	X	X	H	L	L	9	⋮
X	X	X	X	H	L	17	⋮
X	X	X	X	X	H	33	specified

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns; see also waveforms Fig. 4

	V_{DD} V	symbol	min.	typ.		
Minimum clock pulse width; LOW for CP_0 or HIGH for $\overline{CP}_1$	5	t_{WCPL} or t_{WCPH}	180	90	ns	
	10		60	30	ns	
	15		40	20	ns	
Minimum reset pulse width; HIGH	5	t_{WMRH}	150	75	ns	
	10		70	35	ns	
	15		50	25	ns	
Set-up times D_A, D_B, $A/\overline{B}$ → CP_0, $\overline{CP}_1$ L_1 to L_{32} = LOW	5	t_{su}	360	180	ns	see note
	10		140	70	ns	
	15		90	45	ns	
L_{32} = HIGH	5	t_{su}	40	-20	ns	
	10		35	-10	ns	
	15		30	-5	ns	
Hold times D_A, D_B, $A/\overline{B}$ → CP_0, $\overline{CP}_1$ L1 to L32 = LOW	5	t_{hold}	-40	-110	ns	
	10		-10	-45	ns	
	15		0	-30	ns	
L_{32} = HIGH	5	t_{hold}	90	30	ns	
	10		60	20	ns	
	15		50	15	ns	
Recovery times for MR L_1 to L_{32} = LOW	5	t_{RMR}	500	250	ns	
	10		250	125	ns	
	15		150	75	ns	
L_{32} = HIGH	5	t_{RMR}	110	50	ns	
	10		70	30	ns	
	15		60	25	ns	
Minimum clock pulse frequency	5	f_{max}	2,5	5	MHz	
	10		7	14	MHz	
	15		10	20	MHz	

Note

The set-up, hold and recovery times vary with the minimum number of bits selected. For other values as specified one may interpolate as shown in the table (see previous page).

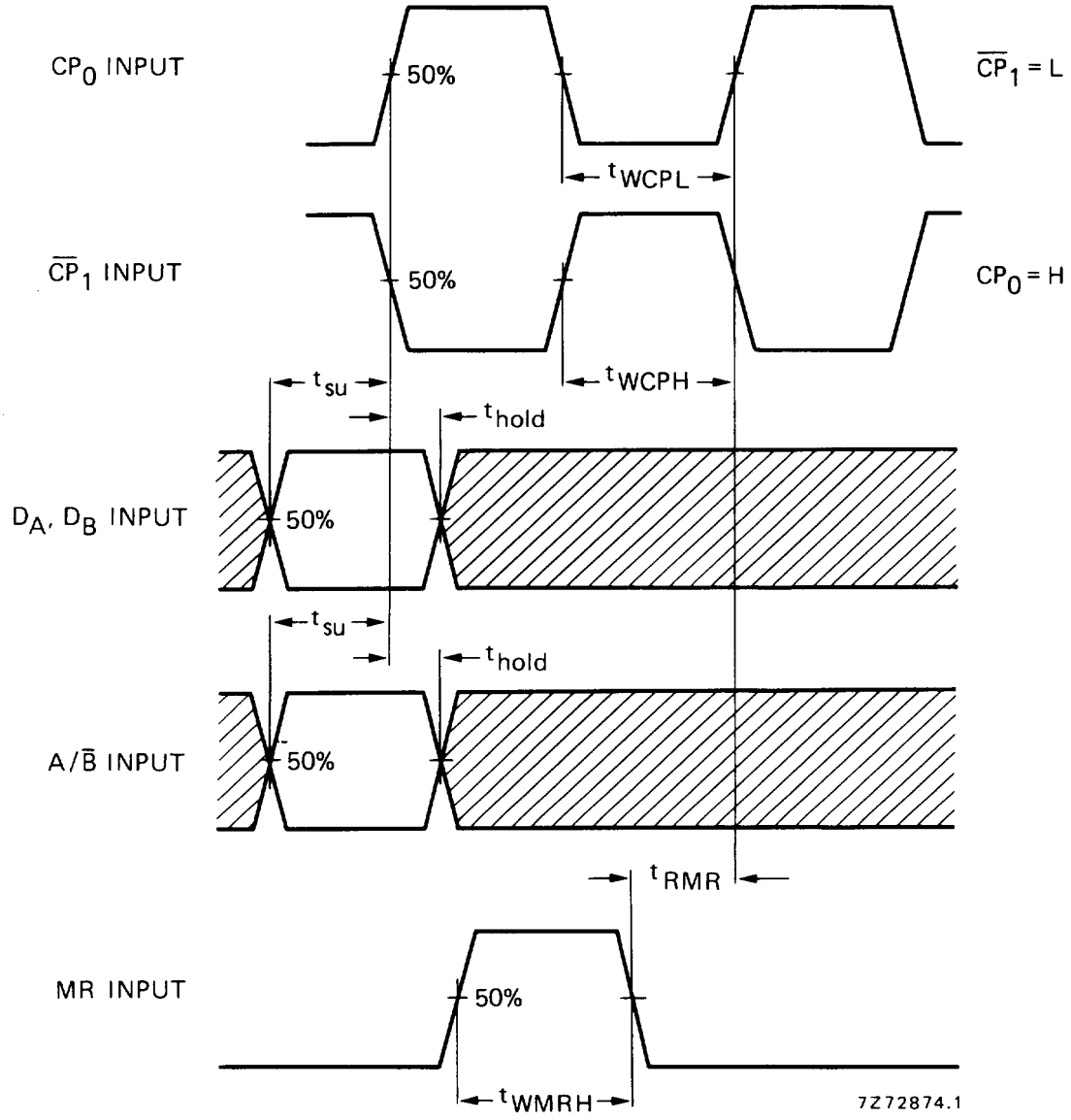

Fig. 4 Waveforms showing recovery time for MR and minimum CP_0, $\overline{CP}_1$ and MR pulse widths, set-up and hold times for D_A, D_B and $A/\overline{B}$ to CP_0 and $\overline{CP}_1$. Set-up and hold times are shown as positive values but may be specified as negative values.