DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4094B
MSI
8-stage shift-and-store bus register

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

8-STAGE SHIFT-AND-STORE BUS REGISTER

The HEF4094B is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs O_0 to O_7. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive-going clock transitions. The data in each shift register stage is transferred to the storage register when the strobe (STR) input is HIGH. Data in the storage register appears at the outputs whenever the output enable (EO) signal is HIGH.

Two serial outputs (O_S and O'_S) are available for cascading a number of HEF4094B devices. Data is available at O_S on positive-going clock edges to allow high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information is available at O'_S on the next negative-going clock edge and provides cascading HEF4094B devices when the clock rise time is slow.

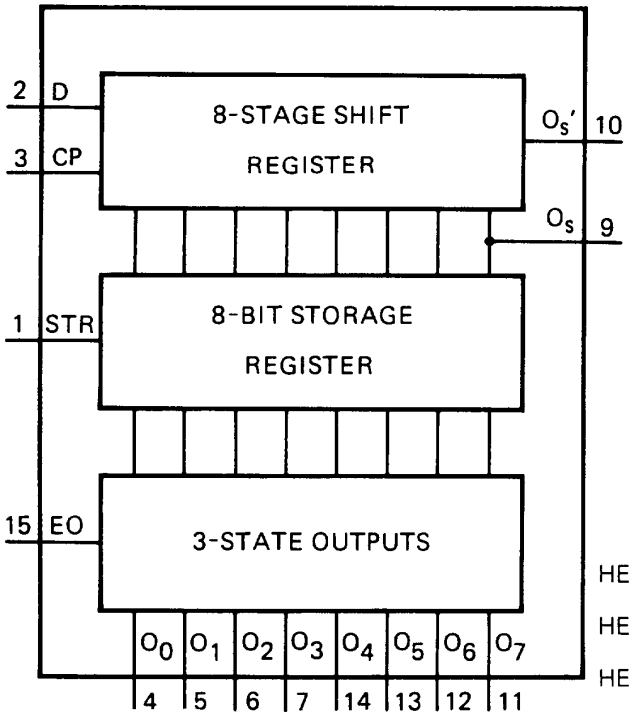

Fig. 1 Functional diagram.

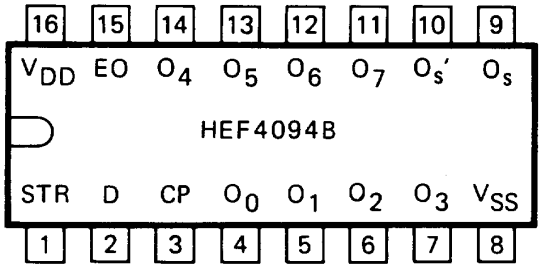

Fig. 2 Pinning diagram.

HEF4094BP(N): 16-lead DIL; plastic (SOT38-1)
HEF4094BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4094BT(D): 16-lead SO; plastic (SOT109-1)
( ): Package Designator North America

PINNING

D	data input	EO	output enable input
CP	clock input	O_S, O'_S	serial outputs
STR	strobe input	O_0 to O_7	parallel outputs

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

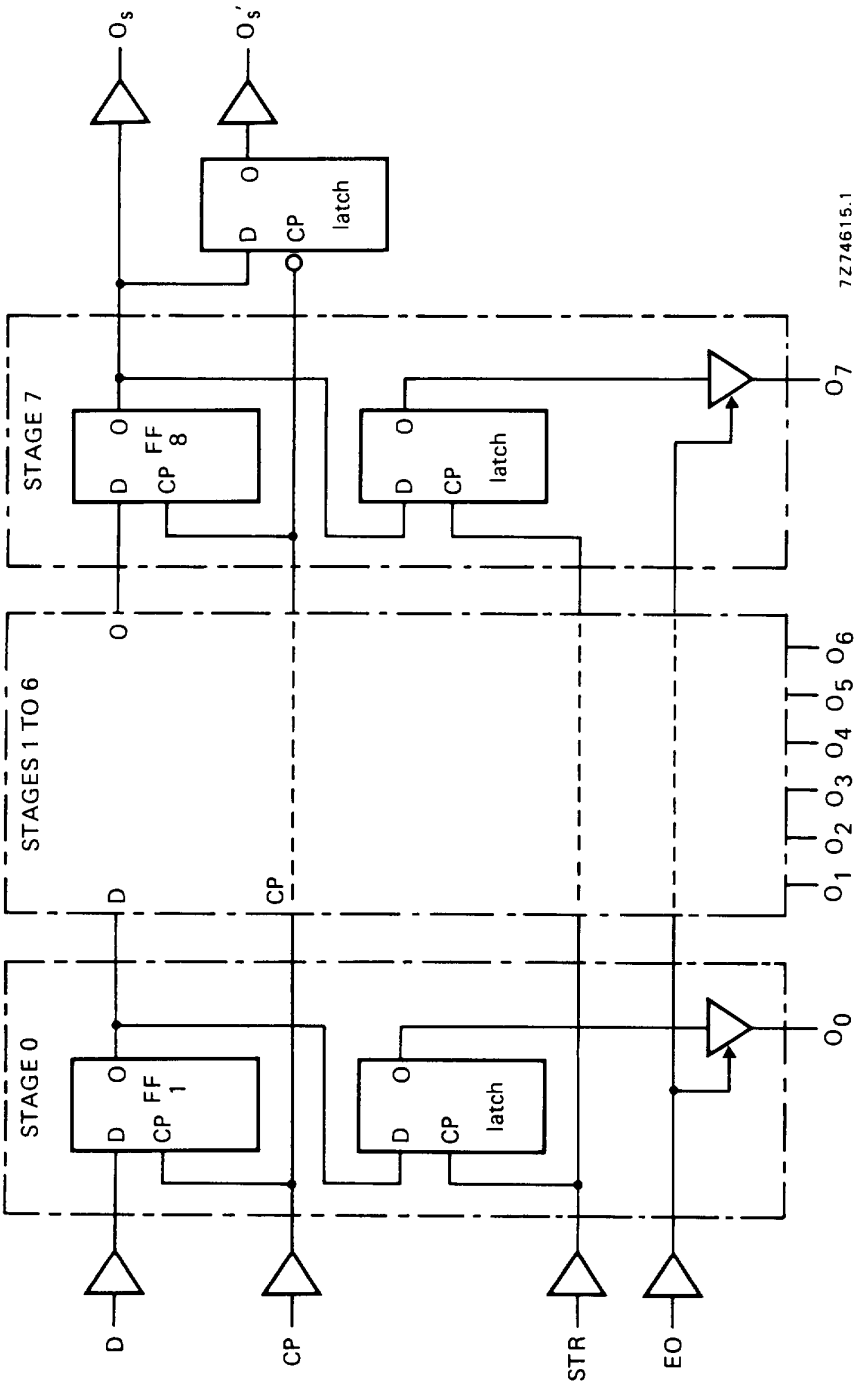

Fig. 3a Logic diagram.

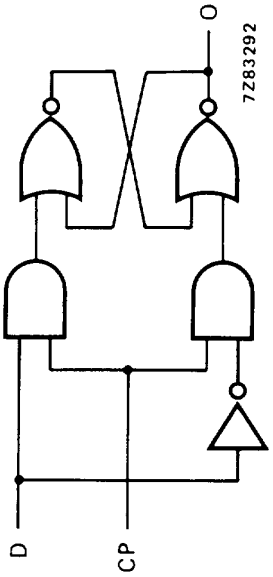

Fig. 3b One D-latch.

FUNCTION TABLE

inputs				parallel outputs		serial outputs	
CP	EO	STR	D	O_0	O_n	O_s	O'_s
∫	L	X	X	Z	Z	O'_6	nc
⌞	L	X	X	Z	Z	nc	O_7
∫	H	L	X	nc	nc	O'_6	nc
∫	H	H	L	L	O_{n-1}	O'_6	nc
∫	H	H	H	H	O_{n-1}	O'_6	nc
⌞	H	H	H	nc	nc	nc	O_7

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition
⌞ = negative-going transition
Z = high impedance off state
nc = no change
O'_6 = the information in the seventh shift register stage

At the positive clock edge the information in the 7th register stage is transferred to the 8th register stage and the O_s output.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$2100\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_oC_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$9700\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	
	15	$26\,000\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
CP → O_s	5		135	270	ns	108 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	65	130	ns	54 ns + (0,23 ns/pF) C_L
	15		50	100	ns	42 ns + (0,16 ns/pF) C_L
	5		105	210	ns	78 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	50	100	ns	39 ns + (0,23 ns/pF) C_L
	15		40	80	ns	32 ns + (0,16 ns/pF) C_L
CP → O'_s	5		105	210	ns	78 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	50	100	ns	39 ns + (0,23 ns/pF) C_L
	15		40	80	ns	32 ns + (0,16 ns/pF) C_L
	5		105	210	ns	78 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	50	100	ns	39 ns + (0,23 ns/pF) C_L
	15		40	80	ns	32 ns + (0,16 ns/pF) C_L
CP → O_n	5		165	330	ns	138 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	75	150	ns	64 ns + (0,23 ns/pF) C_L
	15		55	110	ns	47 ns + (0,16 ns/pF) C_L
	5		150	300	ns	123 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	70	140	ns	59 ns + (0,23 ns/pF) C_L
	15		55	110	ns	47 ns + (0,16 ns/pF) C_L
STR → O_n	5		110	220	ns	83 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	50	100	ns	39 ns + (0,23 ns/pF) C_L
	15		35	70	ns	27 ns + (0,16 ns/pF) C_L
	5		100	200	ns	73 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	45	90	ns	34 ns + (0,23 ns/pF) C_L
	15		35	70	ns	27 ns + (0,16 ns/pF) C_L
Output transition times						
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

A.C. CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		
3-state propagation delays							
Output enable times	5			40	80	ns	
EO → O_n	10	t_{PZH}		25	50	ns	
HIGH	15			20	40	ns	
	5			40	80	ns	
LOW	10	t_{PZL}		25	50	ns	
	15			20	40	ns	
Output disable times	5			75	150	ns	
EO → O_n	10	t_{PHZ}		40	80	ns	
HIGH	15			30	60	ns	
	5			80	160	ns	
LOW	10	t_{PLZ}		40	80	ns	
	15			30	60	ns	
Minimum clock	5		60	30		ns	
pulse width	10	t_{WCPL}	30	15		ns	
LOW	15		24	12		ns	
Minimum strobe	5		40	20		ns	
pulse width	10	t_{WSTRH}	30	15		ns	
HIGH	15		24	12		ns	
Set-up times	5		60	30		ns	
D → CP	10	t_{su}	20	10		ns	
	15		15	5		ns	
Hold times	5		5	–15		ns	
D → CP	10	t_{hold}	20	5		ns	
	15		20	5		ns	
Maximum clock	5		5	10		MHz	
pulse frequency	10	f_{max}	11	22		MHz	
	15		14	28		MHz	

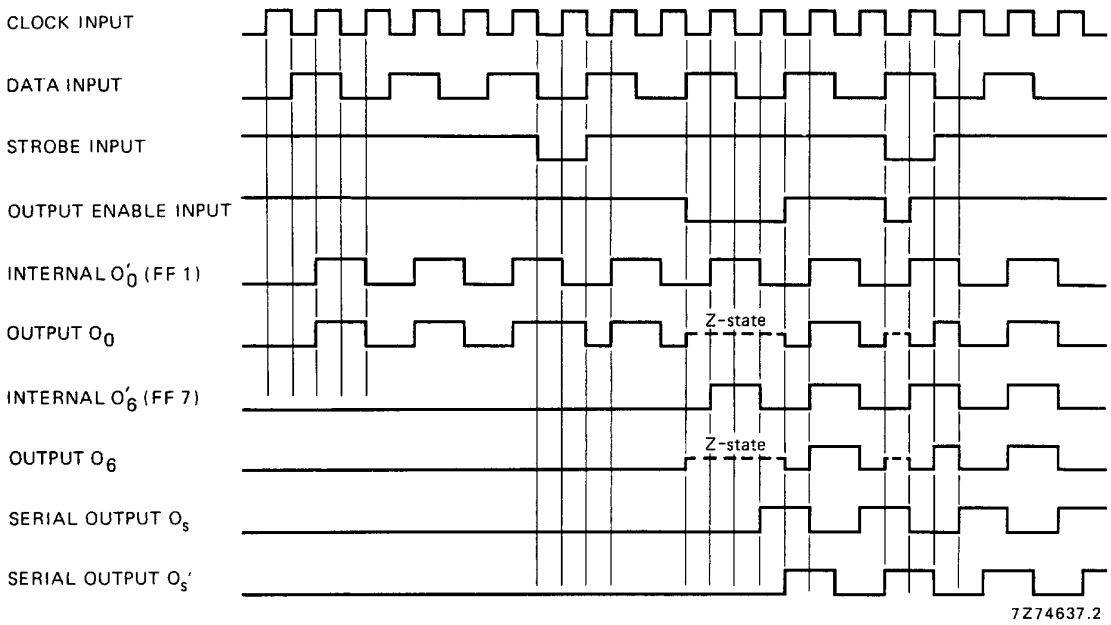

Fig. 4 Timing diagram.

APPLICATION INFORMATION

Some examples of applications for the HEF4094B are:

- Serial-to-parallel data conversion
- Remote control holding register

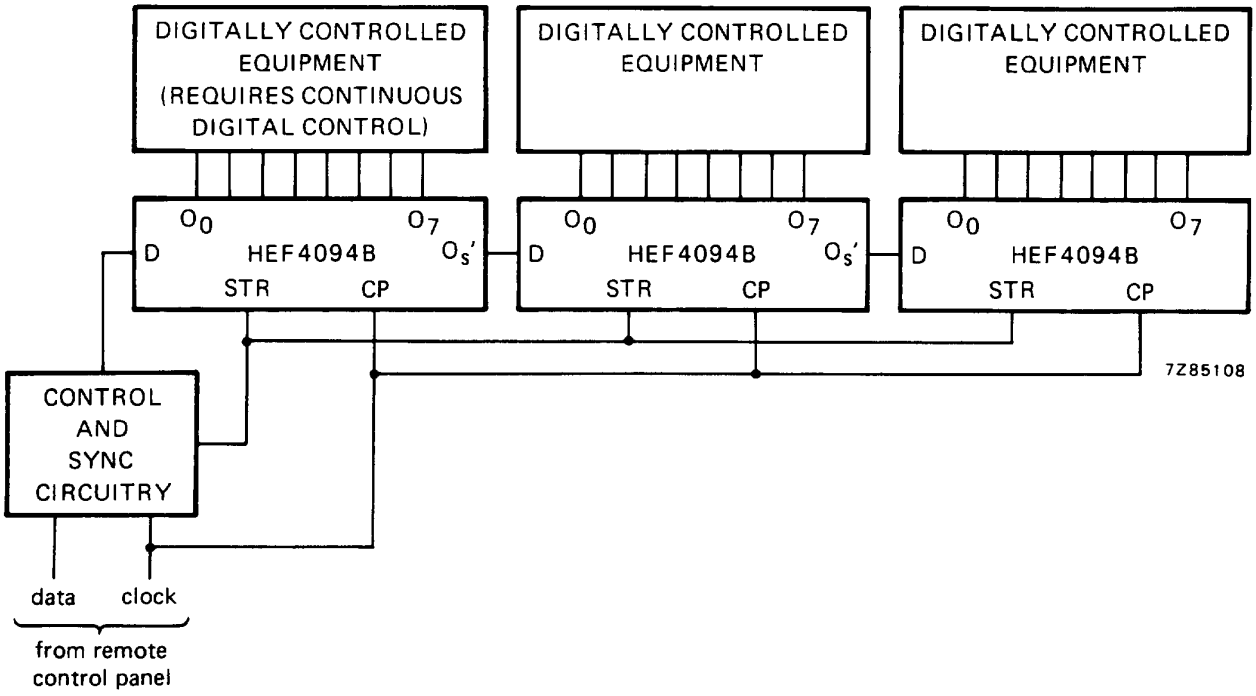

Fig. 5 Remote control holding register.