Features

- **Low Voltage and Standard Voltage Operation**
  - **5.0 (V_{CC} = 4.5V to 5.5V)**
  - **2.7 (V_{CC} = 2.7V to 5.5V)**
  - **1.8 (V_{CC} = 1.8V to 3.6V)**
- **Internally Organized 65,536 x 8**
- **2-Wire Serial Interface**
- **Schmitt Triggers, Filtered Inputs for Noise Suppression**
- **Bidirectional Data Transfer Protocol**
- **1 MHz (5V), 400 kHz (2.7V) and 100 kHz (1.8V) Compatibility**
- **Write Protect Pin for Hardware and Software Data Protection**
- **128-Byte Page Write Mode (Partial Page Writes Allowed)**
- **Self-Timed Write Cycle (5 ms typical)**
- **High Reliability**
  - **Endurance: 100,000 Write Cycles**
  - **Data Retention: 40 Years**
  - **ESD Protection: > 4000V**
- **Automotive Grade and Extended Temperature Devices Available**
- **8-Pin PDIP and 20-Pin JEDEC SOIC and 8-Pin LAP Packages**

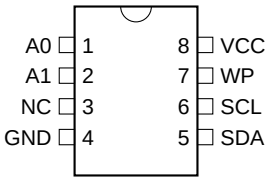
Description

The AT24C512 provides 524,288 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 65,536 words of 8 bits each. The device's cascadable feature allows up to 4 devices to share a common 2-wire bus. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The devices are available in space-saving 8-pin PDIP, 20-pin JEDEC SOIC, and 8-pin Leadless Array (LAP) packages. In addition, the entire family is available in 5.0V (4.5V to 5.5V), 2.7V (2.7V to 5.5V) and 1.8V (1.8V to 3.6V) versions.

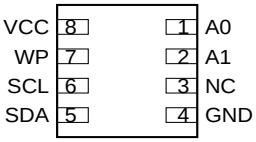
Pin Configurations

Pin Name	Function
A_0 to A_1	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
NC	No Connect

8-Pin PDIP

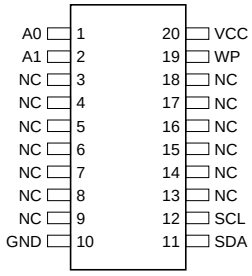


8-Pin Leadless Array



Bottom View

20-Pin SOIC



2-Wire Serial EEPROM

512K (65,536 x 8)

AT24C512 Preliminary

Rev. 1116A–07/98

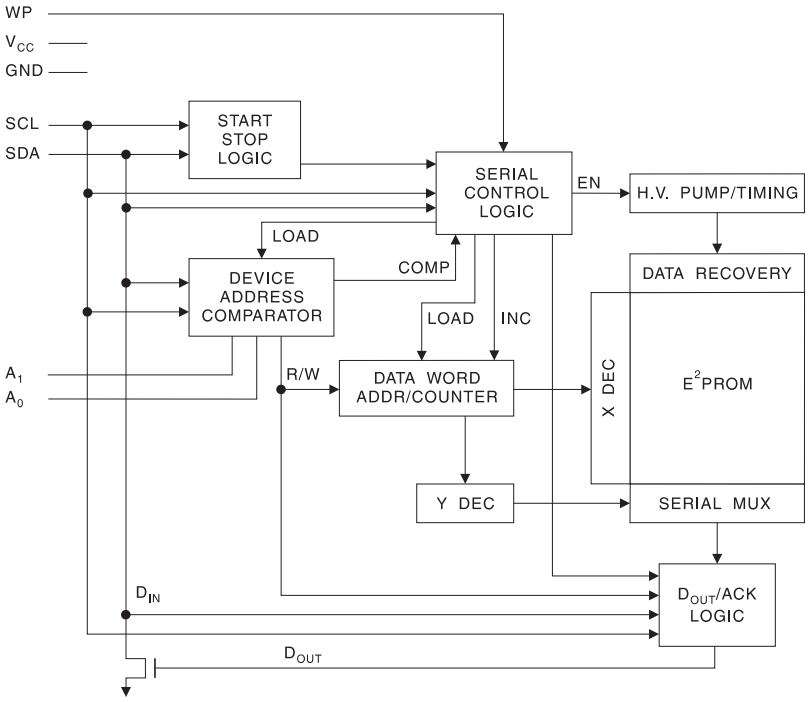
Note: Please contact Atmel Corporation for more information on this product.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

DEVICE/PAGE ADDRESSES (A1, A0): The A1 and A0 pins are device address inputs that are hardwired or left not connected for hardware compatibility with AT24C512. When the pins are hardwired, as many as four 512K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section). When the pins are not hardwired, the default A_1 and A_0 are zero.

WRITE PROTECT (WP): The write protect input, when tied to GND, allows normal write operations. When WP is tied high to V_{CC}, all write operations to the memory are inhibited. If left unconnected, WP is internally pulled down to GND. Switching WP to V_{CC} prior to a write operation creates a software write protect function.

Memory Organization

AT24C512, 512K SERIAL EEPROM: The 512K is internally organized as 512 pages of 128-bytes each. Random word addressing requires a 16-bit data word address.