DATA SHEET

74LV165

8-bit parallel-in/serial-out shift register

Product specification
Supersedes data of 1997 Feb 12
IC24 Data Handbook

1997 May 15

Philips
Semiconductors

PHILIPS

8-bit parallel-in/serial-out shift register 74LV165

FEATURES

- Wide operating voltage: 1.0 to 5.5 V
- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Asynchronous 8-bit parallel load
- Synchronous serial input
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV165 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT165.

The 74LV165 is an 8-bit parallel-load or serial-in shift register with complementary serial outputs (Q_7 and $\overline{Q}_7$) available from the last stage. When the parallel load ($\overline{PL}$) input is LOW, parallel data from the D_0 to D_7 inputs are loaded into the register asynchronously. When $\overline{PL}$ is HIGH, data enters the register serially at the D_S input and shifts one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$, etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by tying the Q_7 output to the D_S input of the succeeding stage.

The clock input is a gated-OR structure which allows one input to be used as an active LOW clock enable ($\overline{CE}$) input. The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of input $\overline{CE}$ should only take place while CP HIGH for predictable operation. Either the CP or the $\overline{CE}$ should be HIGH before the LOW-to-HIGH transition of $\overline{PL}$ to prevent shifting the data when $\overline{PL}$ is activated.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay $\overline{CE}$, CP to Q_7, $\overline{Q}_7$ $\overline{PL}$ to Q_7, $\overline{Q}_7$ D_7 to Q_7, $\overline{Q}_7$	C_L = 15 pF; V_{CC} = 3.3 V	 18 18 14	ns
f_{max}	Maximum clock frequency		78	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per package	V_{CC} = 3.3 V V_I = GND to V_{CC}[1]	35	pF

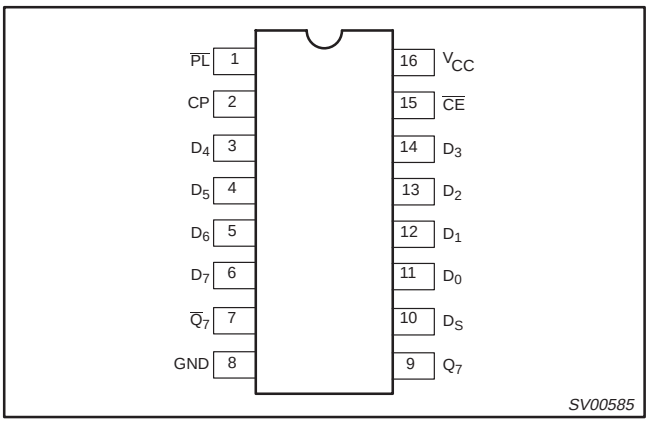
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	–40°C to +125°C	74LV165 N	74LV165 N	SOT38-4
16-Pin Plastic SO	–40°C to +125°C	74LV165 D	74LV165 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +125°C	74LV165 DB	74LV165 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV165 PW	74LV165PW DH	SOT403-1

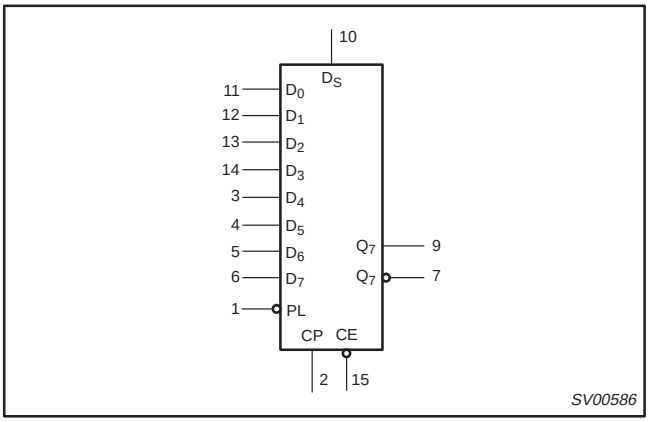
PIN CONFIGURATION



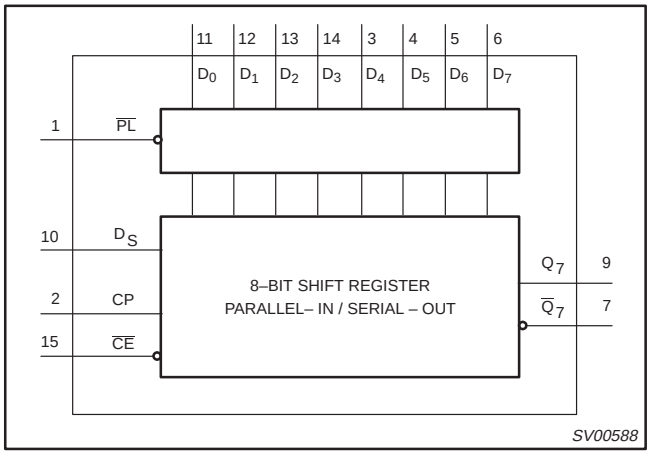
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{PL}$	Asynchronous parallel load input (active LOW)
2	CP	Clock input (LOW to HIGH, edge-triggered)
7	$\overline{Q}_7$	Complementary output from the last stage
8	GND	Ground (0 V)
9	Q_7	Serial output from last stage
10	D_S	Serial data input
11, 12, 13, 14, 3, 4, 5, 6	D_0 to D_7	Parallel data inputs
15	$\overline{CE}$	Clock enable input (active LOW)
16	V_{CC}	Positive supply voltage

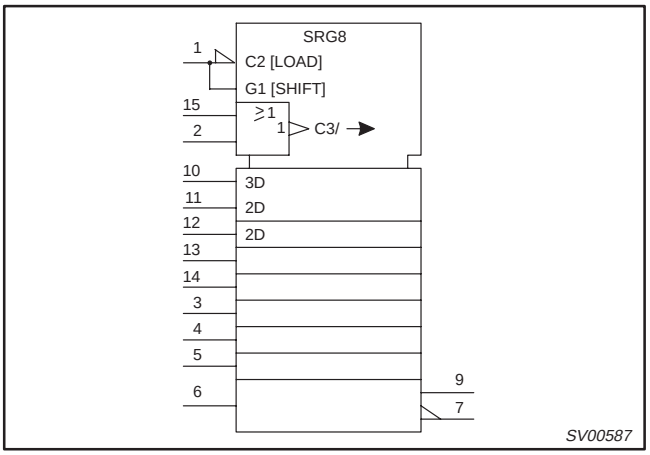
LOGIC SYMBOL



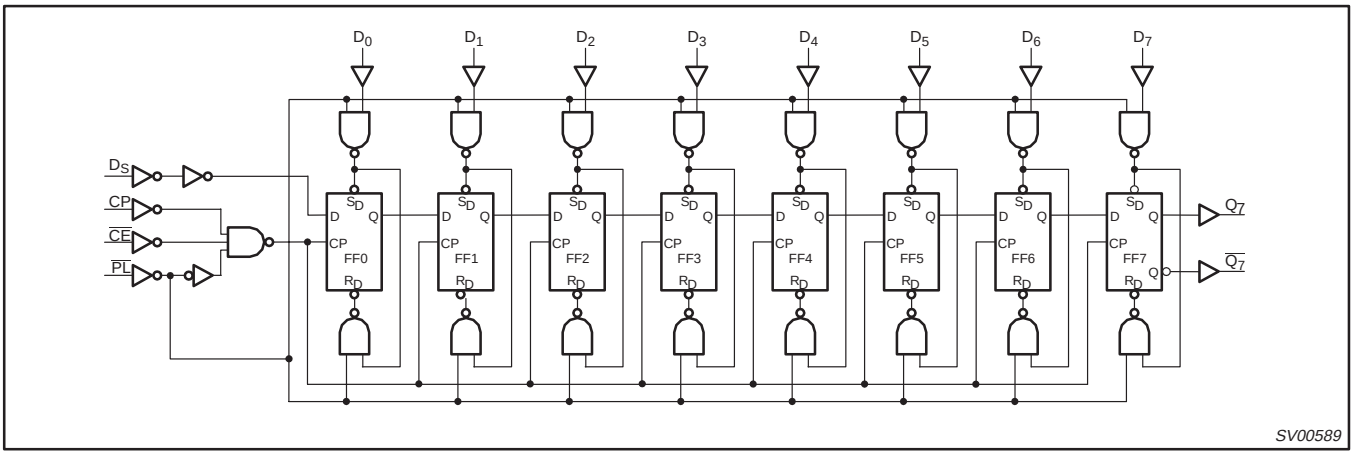
FUNCTIONAL DIAGRAM



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS					Qn REGISTERS		OUTPUTS	
	$\overline{PL}$	$\overline{CE}$	CP	D_S	D_0–D_7	Q_0	Q_1–Q_6	Q_7	$\overline{Q}_7$
Parallel load	L	X	X	X	L	L	L–L	L	H
	L	X	X	X	H	H	H–H	H	L
Serial Shift	H	L	↑	l	X	L	q_0–q_5	q_6	$\overline{q}_6$
	H	L	↑	h	X	H	q_0–q_5	q_6	$\overline{q}_6$
Hold “do nothing”	H	H	X	X	X	q_0	q_1–q_6	q_7	q_7

NOTES:
H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level level one set-up time prior to the LOW-to-HIGH clock transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition
X = don’t care
↑ = LOW-to-HIGH clock transition

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics per device	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times except for Schmitt-trigger inputs	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < –0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < –0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs – bus driver outputs	$–0.5V < V_O < V_{CC} + 0.5V$	 25 35	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs – bus driver outputs		 50 70	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V	0.9			0.9		V
		V_{CC} = 2.0 V	1.4			1.4		
		V_{CC} = 2.7 to 3.6 V	2.0			2.0		
		V_{CC} = 4.5 to 5.5 V	0.7 ∗ V_{CC}			0.7 ∗ V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V			0.3		0.3	V
		V_{CC} = 2.0 V			0.6		0.6	
		V_{CC} = 2.7 to 3.6 V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3 ∗ V_{CC}		0.3 ∗ V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2 V; V_I = V_{IH} or $V_{IL;}$ $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0 V; V_I = V_{IH} or $V_{IL;}$ $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7 V; V_I = V_{IH} or $V_{IL;}$ $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0 V; V_I = V_{IH} or $V_{IL;}$ $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5 V; V_I = V_{IH} or $V_{IL;}$ $-I_O$ = 100µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0 V; V_I = V_{IH} or $V_{IL;}$ $-I_O$ = 6mA	2.40	2.82		2.20		V
		V_{CC} = 4.5 V; V_I = V_{IH} or $V_{IL;}$ $-I_O$ = 12mA	3.60	4.20		3.50		
V_{OH}	HIGH level output voltage; BUS driver outputs	V_{CC} = 3.0 V; V_I = V_{IH} or $V_{IL;}$ $-I_O$ = 8mA	2.40	2.82		2.20		V
		V_{CC} = 4.5 V; V_I = V_{IH} or $V_{IL;}$ $-I_O$ = 16mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2 V; V_I = V_{IH} or $V_{IL;}$ I_O = 100µA		0				V
		V_{CC} = 2.0 V; V_I = V_{IH} or $V_{IL;}$ I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7 V; V_I = V_{IH} or $V_{IL;}$ I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0 V; V_I = V_{IH} or $V_{IL;}$ I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5 V; V_I = V_{IH} or $V_{IL;}$ I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0 V; V_I = V_{IH} or $V_{IL;}$ I_O = 6mA		0.25	0.40		0.50	V
		V_{CC} = 4.5 V; V_I = V_{IH} or $V_{IL;}$ I_O = 12mA		0.35	0.55		0.65	
V_{OL}	LOW level output voltage; BUS driver outputs	V_{CC} = 3.0 V; V_I = V_{IH} or $V_{IL;}$ I_O = 8mA		0.20	0.40		0.50	V
		V_{CC} = 4.5 V; V_I = V_{IH} or $V_{IL;}$ I_O = 16mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5 V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 5.5 V; V_I = V_{IH} or $V_{IL;}$ V_O = V_{CC} or GND			5		10	µA
I_{CC}	Quiescent supply current; SSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		40	µA
	Quiescent supply current; flip-flops	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		80	
	Quiescent supply current; MSI	V_{CC} = 5.5 V; V_I = V_{CC} or GND; I_O = 0			20.0		160	µA
	Quiescent supply current; LSI	V_{CC} = 5.5 V; V_I = V_{CC} or GND; I_O = 0			500		1000	
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 V to 3.6 V; V_I = V_{CC} – 0.6 V			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PLH}/t_{PHL}	Propagation delay $\overline{CE}$, CP to Q_7, $\overline{Q}_7$	Figures 1, 6	1.2	–	115		–		ns
			2.0	–	39	75	–	90	
			2.7	–	29	55	–	66	
			3.0 to 3.6	–	22[2]	44	–	53	
t_{PLH}/t_{PHL}	Propagation delay $\overline{PL}$ to Q_7, $\overline{Q}_7$	Figures 1, 6	1.2	–	110		–		ns
			2.0	–	37	70	–	85	
			2.7	–	28	51	–	63	
			3.0 to 3.6	–	21[2]	41	–	50	
t_{PLH}/t_{PHL}	Propagation delay D_7 to Q_7, $\overline{Q}_7$	Figures 4, 6	1.2	–	90		–		ns
			2.0	–	31	58	–	70	
			2.7	–	23	43	–	51	
			3.0 to 3.6	–	17[2]	34	–	41	
t_w	Clock Pulse width HIGH or LOW	Figures 4, 6	2.0	34	10	–	41	–	ns
			2.7	25	8	–	30	–	
			3.0 to 3.6	20	6[2]	–	24	–	
t_w	Parallel load pulse width LOW	Figures 4, 6	2.0	34	9	–	41	–	ns
			2.7	25	6	–	30	–	
			3.0 to 3.6	20	5[2]	–	24	–	
t_{rem}	Removal time $\overline{PL}$ to CP, $\overline{CE}$	Figures 4, 6	1.2	–	40	–	–	–	ns
			2.0	26	14	–	31	–	
			2.7	19	10	–	23	–	
			3.0 to 3.6	15	8[2]	–	18	–	
t_{su}	Set-up time D_S to CP, $\overline{CE}$	Figures 4, 6	1.2	–	20	–	–	–	ns
			2.0	22	7	–	26	–	
			2.7	16	5	–	19	–	
			3.0 to 3.6	13	4[2]	–	15	–	
t_{su}	Set-up time $\overline{CE}$ to CP; CP to $\overline{CE}$	Figures 4, 6	1.2	–	30	–	–	–	ns
			2.0	22	10	–	26	–	
			2.7	16	8	–	19	–	
			3.0 to 3.6	13	6[2]	–	15	–	
t_{su}	Set-up time D_n to $\overline{PL}$	Figures 4, 6	1.2	–	40	–	–	–	ns
			2.0	26	14	–	31	–	
			2.7	19	10	–	23	–	
			3.0 to 3.6	15	8[2]	–	18	–	

AC CHARACTERISTICS (*Continued*)

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_h	Hold time D_s to CP, $\overline{CE}$ D_n to $\overline{PL}$	Figures 4, 6	1.2	–	20	10	–	–	ns
			2.0	22	8	4	8	–	
			2.7	16	8	3	8	–	
			3.0 to 3.6	13	8	2[2]	8	–	
t_h	Hold time $\overline{CE}$ to CP, CP to $\overline{CE}$	Figures 4, 6	1.2	–	–30	–	–	–	ns
			2.0	5	–10	–	5	–	
			2.7	5	–8	–	5	–	
			3.0 to 3.6	5	–6[2]	–	5	–	
f_{max}	Maximum clock pulse frequency	Figures 4, 6	2.0	14	40	–	12	–	MHz
			2.7	19	58	–	16	–	
			3.0 to 3.6	24	70[2]	–	20	–	

NOTES:
1. Unless otherwise stated, all typical values are measured at $T_{amb} = 25°C$
2. Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V.
$V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7$ V;
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

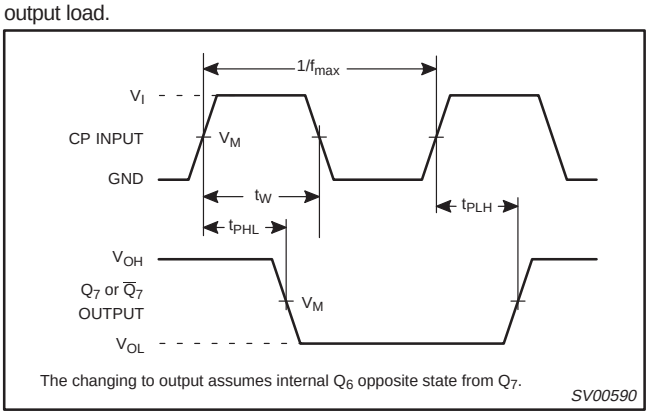


Figure 1. Clock (CP) to output (Q_7 or $\overline{Q}_7$) propagation delays, the clock pulse width and the maximum clock frequency.

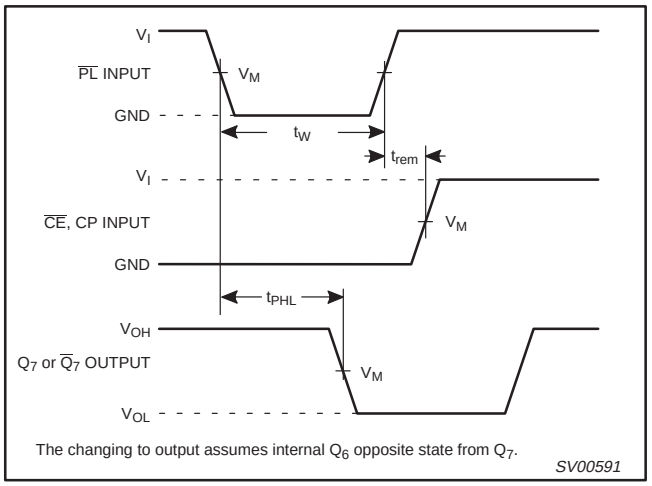


Figure 2. Parallel load ($\overline{PL}$) pulse width, the parallel load to output (Q_7 or $\overline{Q}_7$) propagation delays, the parallel load to clock (CP) and clock enable ($\overline{CE}$) removal time.

Note to Figures 1 and 2

The changing to output assumes internal Q_6 opposite state from Q_7.

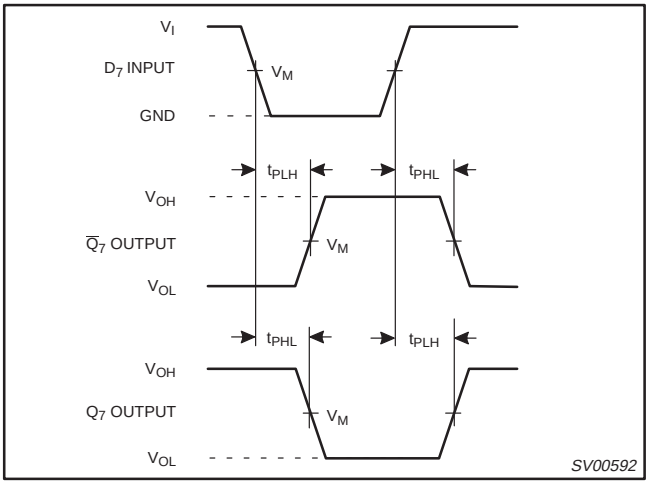


Figure 3. Data input (D_n) to output (Q_7 or $\overline{Q}_7$) propagation delays when $\overline{PL}$ is LOW.

Note to Figure 4

$\overline{CE}$ may change only from HIGH-to-LOW while CP is LOW. The shaded areas indicate when the input is permitted to change for predictable output performance.

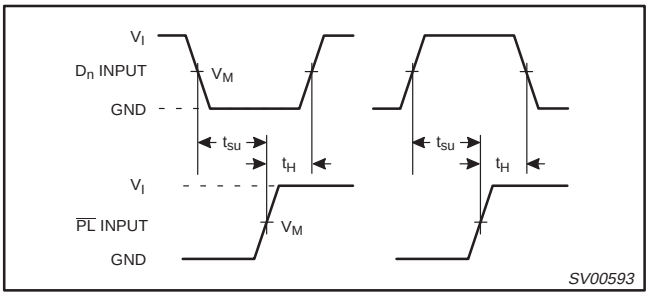


Figure 5. Set-up and hold times from the data inputs (D_n) to the parallel load input ($\overline{PL}$).

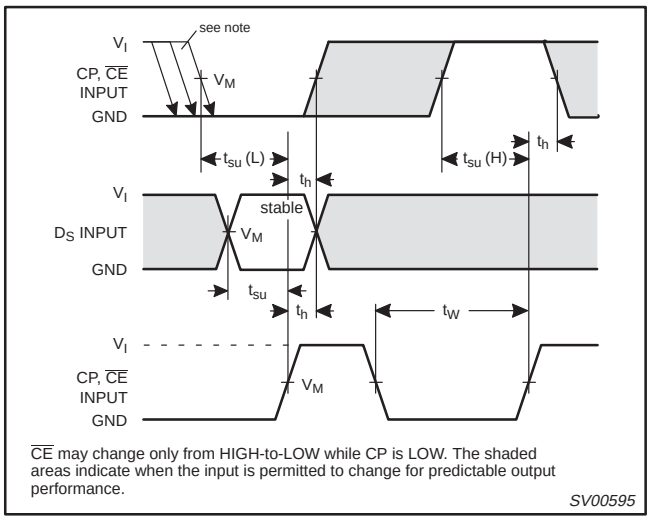
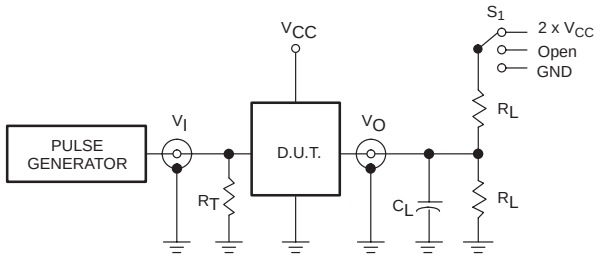


Figure 4. Set-up and hold times from the serial data input (D_S) to the clock (CP) and the clock enable ($\overline{CE}$) inputs, from the clock enable input ($\overline{CE}$) to the clock input (CP) and from the clock input (CP) to the clock enable input ($\overline{CE}$).

TEST CIRCUIT



Test Circuit for switching times

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V
≥ 4.5V	V_{CC}

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

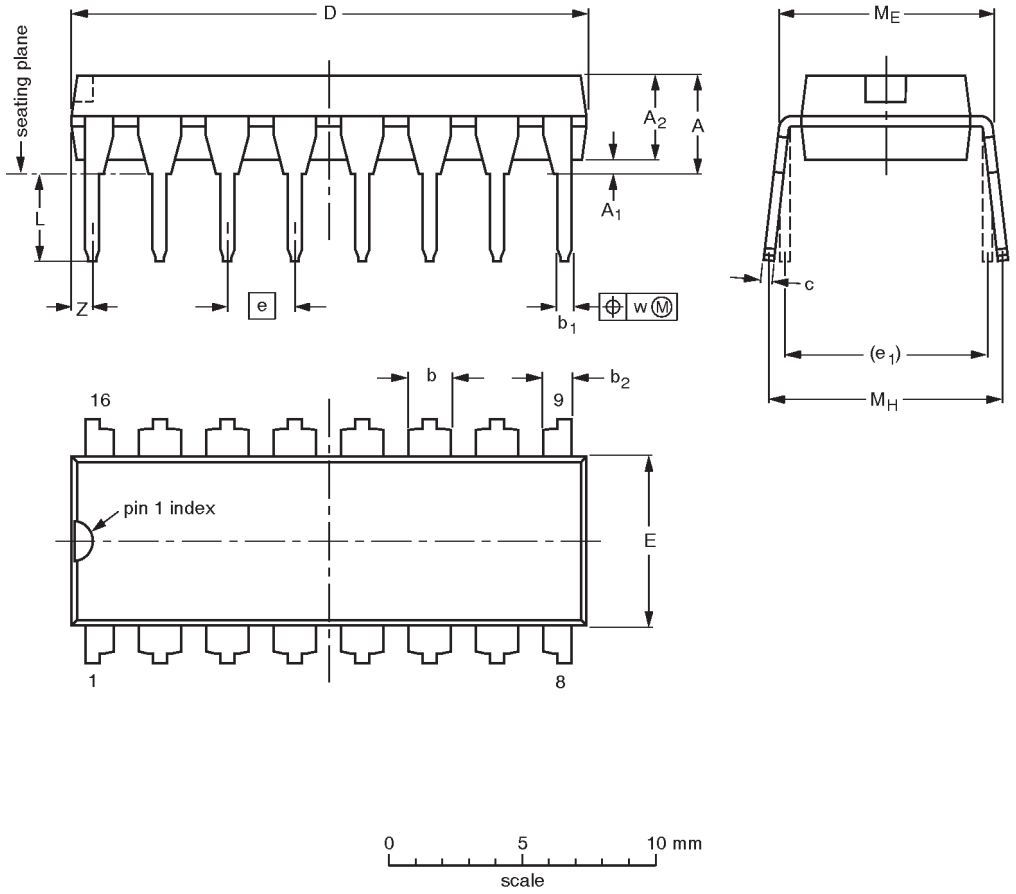
C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SV00755

Figure 6. Load circuitry for switching times.

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

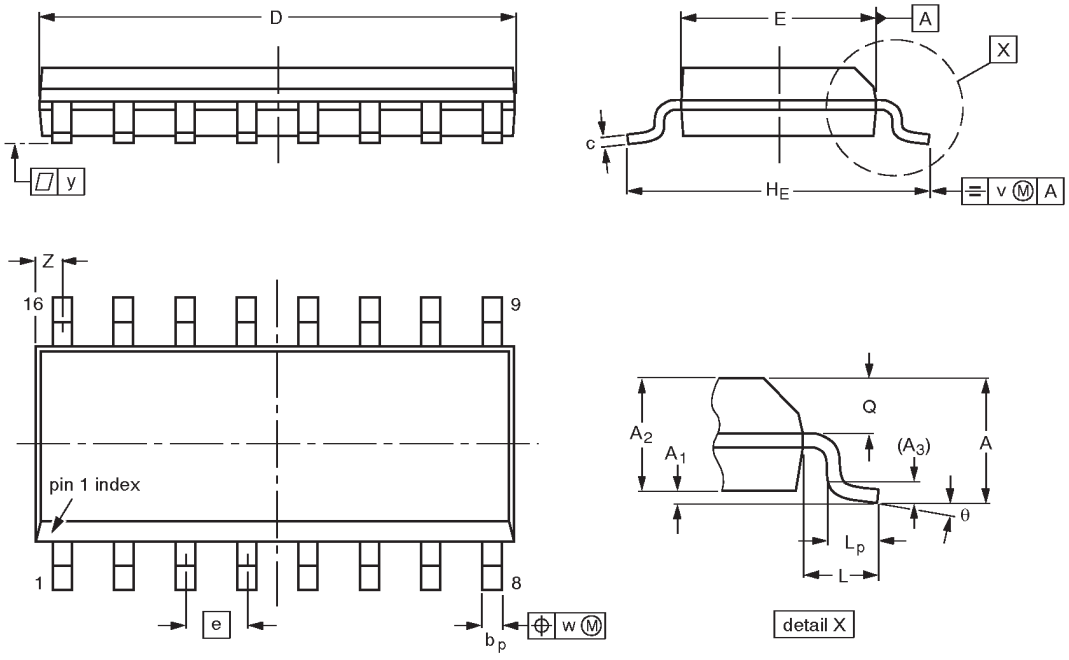
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

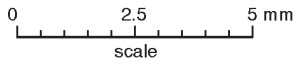
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

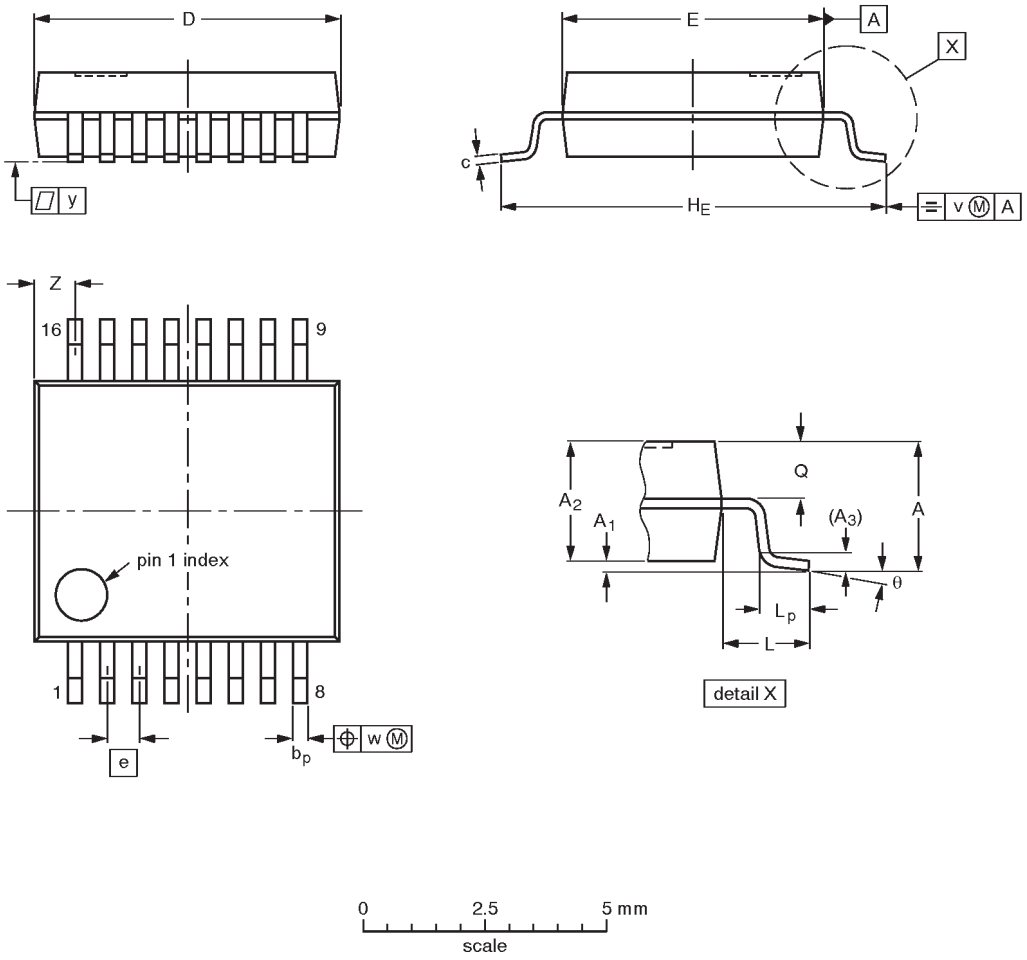
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~91-08-13~~ 95-01-23

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

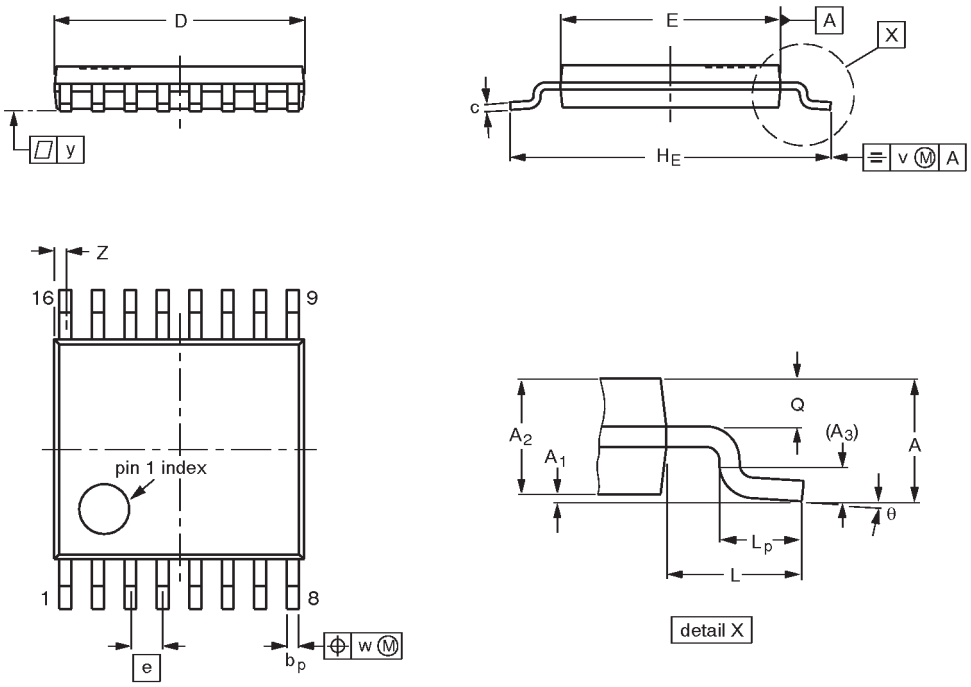
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

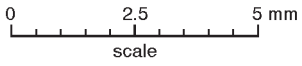
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				~~94-01-14~~ 95-02-04

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm SOT403-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~94-07-12~~ 95-04-04

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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