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Recommended Usage of Microchip SPI Serial SRAM Devices

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INTRODUCTION

Many embedded systems require some amount of volatile storage for temporary data. This is increasingly true with internet enabled devices. Because of their small footprint, low I/O pin requirement, low-power consumption and low cost, serial SRAMs are a popular choice for volatile storage. Microchip Technology has addressed this need by offering a line of serial SRAMs using the industry standard SPI communication. Serial SRAM devices are available in a number of density offerings, operational voltage ranges and packaging options. The serial SRAM products offer an alternative to the traditional parallel architecture that saves both board area and also I/O count on the MCU.

In order to achieve a highly robust application when utilizing serial SRAMs, the designer must consider more than just the data sheet specifications.

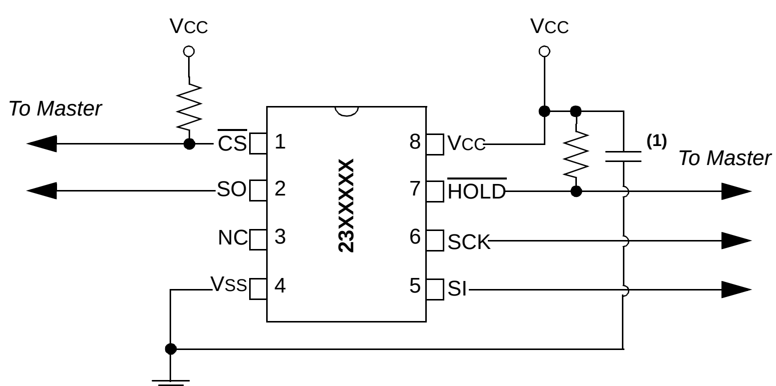
There are a number of conditions which could potentially result in non-standard operation. The most important of them are discussed in this application note.

This application note provides assistance and guidance with the use of Microchip SPI serial SRAMs. These recommendations are not meant as requirements; however, their adoption will lead to a more robust overall design. The following topics are discussed:

- Input Considerations
- Power Supply
- STATUS Register
- Operating Modes

Figure 1 shows the suggested connections for using Microchip SPI serial SRAMs. The basis for these connections will be explained in the sections which follow.

FIGURE 1: RECOMMENDED CONNECTIONS FOR 23XXXX SERIES DEVICES



Note 1: A decoupling capacitor (typically 0.1 μF) should be used on VCC.

INPUT CONSIDERATIONS

It is never good practice to leave an input pin floating. This can cause high standby current as well as undesired functionality. If a pin is left floating, it can either float low or high. Which direction the signal goes is dependent upon a number of factors, including noise in the system and capacitive coupling. Because of this, the level seen by the input circuitry is relatively random and likely to change during operation.

Such unpredictable input levels can have devastating effects on device operation. For example, Microchip's SPI serial SRAMs feature a $\overline{\text{HOLD}}$ pin which allows the user to suspend the clock mid-stream. If this pin were to float low (active), the device would no longer react to any clock pulses received, communication would be disrupted and data potentially lost or corrupted.

Therefore, any unused input pins should always be tied to a proper level, such as high for an active-low input. Moreover, it is recommended that, if the microcontroller has extra, tri-state I/O pins available, connections be made to these unused inputs along with a pull-down/pull-up resistor, as shown in Figure 1. This will allow for the inputs to be used at a later date simply by modifying firmware.

Although the $\overline{\text{CS}}$ pin should always be driven by the microcontroller during normal operation, it has potential for floating during power-down/power-up. As such, this pin should also have a pull-up resistor to avoid undesired commands due to noise during these conditions.

POWER SUPPLY

Microchip SPI serial SRAMs feature a robust serial communication protocol that helps to prevent unintentional writes and data corruption while power is within normal operating levels. But, certain considerations should be made regarding power-up and power-down conditions to ensure the same level of protection during those times when power is not within normal operating levels.

As shown in Figure 1, a decoupling capacitor (typically 0.1 μF) should be used to help filter out small ripples on V_{CC}.

Power-Up

On power-up, V_{CC} should always begin at 0V and rise straight to its normal operating level to ensure a proper Power-on Reset. V_{CC} should not linger at an ambiguous level (i.e., below the minimum operating voltage).

However, if V_{CC} happens to fall below the minimum retention voltage for the device (see data sheet DC characteristics), it is recommended that V_{CC} be brought down fully to 0V before returning to normal operating level. This will help to ensure that the device is reset properly.

Furthermore, if the microcontroller features a Brown-out Reset with a threshold higher than that of the serial SRAM, bringing V_{CC} down to 0V will allow both devices to be reset together. Otherwise, the microcontroller may reset during communication while the SRAM is still in an operational condition.

Power Failure During a Write

During the time that data is being written to the SRAM V_{DD} should remain above the minimum operating voltage. If at any time V_{DD} drops below this minimum voltage but remains above the retention voltage, (as specified in the product data sheet) care should be taken to ensure that the data written to the device is free from errors.

STATUS REGISTER

Microchip SPI serial SRAMs feature a STATUS register. The STATUS register is used to control features of the device and is a read/write register. Bits within the STATUS register are used to control the following functions:

- HOLD Feature
- Operating modes:
- Byte mode
- Page mode
- Sequential mode

The STATUS register is accessed through the Read Status Register (RDSR) and Write Status Register (WRSR) commands.

For the 23XX256, bits 1 through 5 should always be set to '0'. For the 23XX640, bits 2 through 5 should always be set to '0'. Bit 1 will read back as a '1' but this bit must always be written back as '0' to ensure correct operation.

HOLD FEATURE

The HOLD bit (bit 0) in the STATUS register is used to enable and disable the hardware HOLD feature. To enable the HOLD pin, bit 0 must be cleared before the pin can be toggled. Setting this bit to 1 will disable the hardware pin.

OPERATING MODES

The Microchip serial SRAM has three operating modes.

Byte Mode

Byte Mode is selected when bits 7:6 in the STATUS register are set to 00. In this mode, all read and write operations are limited to the byte that is addressed with the 16-bit address clocked into the device after the instruction. The user can read or write to the same byte continuously until the CS line is brought high, terminating the command. The internal Address Pointer is not incremented.

Page Mode

Page mode is selected when bits 7:6 in the STATUS register are set to 10. In this mode, read and write operations are limited to the current page that is addressed with the 16-bit address following the instruction.

The serial SRAM has a page size of 32 bytes, with either 1024 pages (23XX256) or 256 pages (23XX640). In Page mode the user can either read data from or write data to the current page. As the internal Address Pointer is incremented at the end of the page boundary it will roll over to the beginning of the current page. If a write is being executed the data at the beginning of the page will be overwritten. The address sent after the instruction does not have to be aligned to a page boundary.

Sequential Mode

Sequential mode is selected when bits 7:6 in the STATUS register are set to 01. In this mode, read and write operations can be performed on the whole array.

The address sent after the instruction is the first array location that will be read from or written to. With each subsequent data byte, the internal Address Pointer is incremented. At any point, the read or write sequence can be terminated by raising CS. At the end of the SRAM array, the internal Address Pointer will roll-over to 0x0000.

SUMMARY

This application note illustrates recommended techniques for increasing design robustness when using Microchip SPI serial SRAMs. These recommendations fall directly in line with how Microchip designs, manufactures, qualifies and tests its serial SRAMs and will allow the devices to operate within the data sheet parameters. It also serves to explain in detail some of the features of the device and makes the user aware of any potential pitfalls that they may fall into.

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